

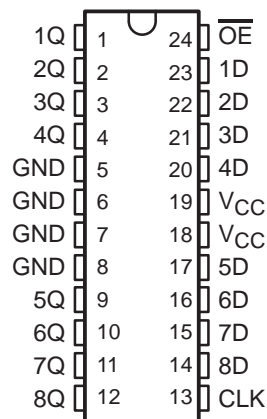
74ACT11374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS217A – JULY 1987 – REVISED APRIL 1996

- Eight D-Type Flip-Flops in a Single Package
- 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (NT)

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 74ACT11374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

An output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state provides the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

\overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT11374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
L	H	X	Q_0
L	\downarrow	X	Q_0
H	X	X	Z



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**TEXAS
INSTRUMENTS**

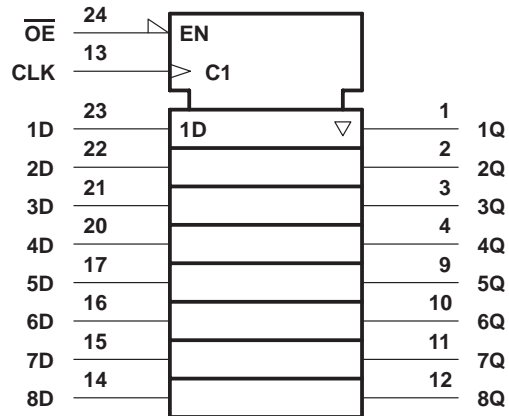
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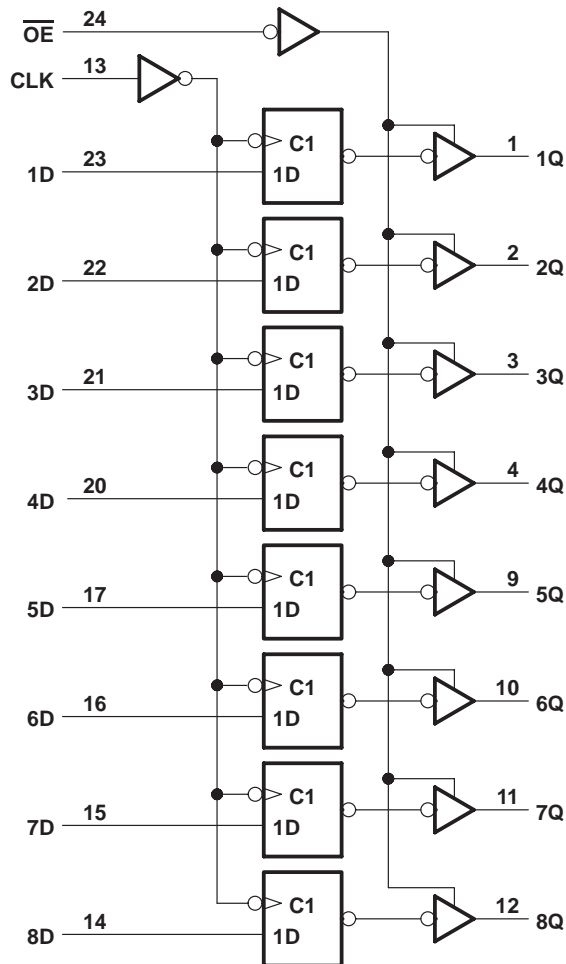
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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WITH 3-STATE OUTPUTS

SCAS217A – JULY 1987 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V	
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V	
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA	
Continuous current through V_{CC} or GND	±200 mA	
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	DB package	0.65 W
	DW package	1.7 W
	NT package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	V
I_{OH} High-level output current		–24	mA
I_{OL} Low-level output current		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
T_A Operating free-air temperature	–40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I _{OH} = -75 mA†	5.5 V				3.85		
V _{OL}	I _{OL} = 50 μA	4.5 V	0.1			0.1		V
		5.5 V	0.1			0.1		
	I _{OL} = 24 mA	4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
	I _{OL} = 75 mA†	5.5 V				1.65		
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±0.5			±5		μA
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	8			80		μA
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V	0.9			1		mA
C _i	V _I = V _{CC} or GND	5 V	4					pF
C _o	V _O = V _{CC} or GND	5 V	10					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f _{clock}	Clock frequency	0	55	0	55	MHz
t _w	Pulse duration, CLK low or CLK high	9		9		ns
t _{su}	Setup time, data before CLK↑	3		3		ns
t _h	Hold time, data after CLK↑	5.5		5.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

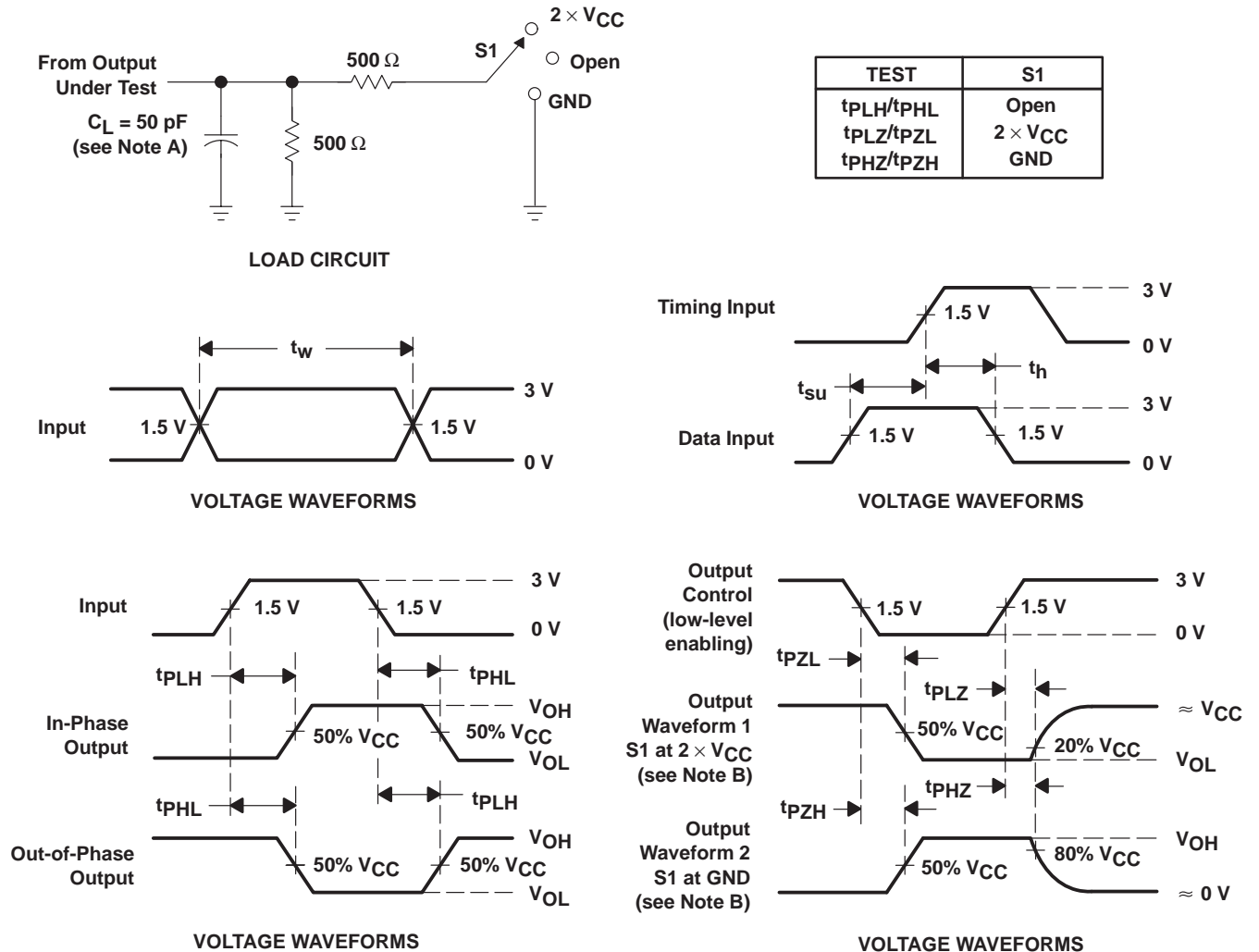
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f _{max}			55	70		55		MHz
t _{PLH}	CLK	Any Q	1.5	8.5	10.7	1.5	12.4	ns
t _{PHL}			1.5	8.5	11.3	1.5	13	
t _{PZH}	OE	Any Q	1.5	7.5	11	1.5	12.3	ns
t _{PZL}			1.5	7.5	11	1.5	12.3	
t _{PHZ}	OE	Any Q	1.5	11	12.7	1.5	13.2	ns
t _{PLZ}			1.5	8	10	1.5	10.8	



operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	107	pF
		Outputs disabled	96	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT11374DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
74ACT11374DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11374NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
74ACT11374NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

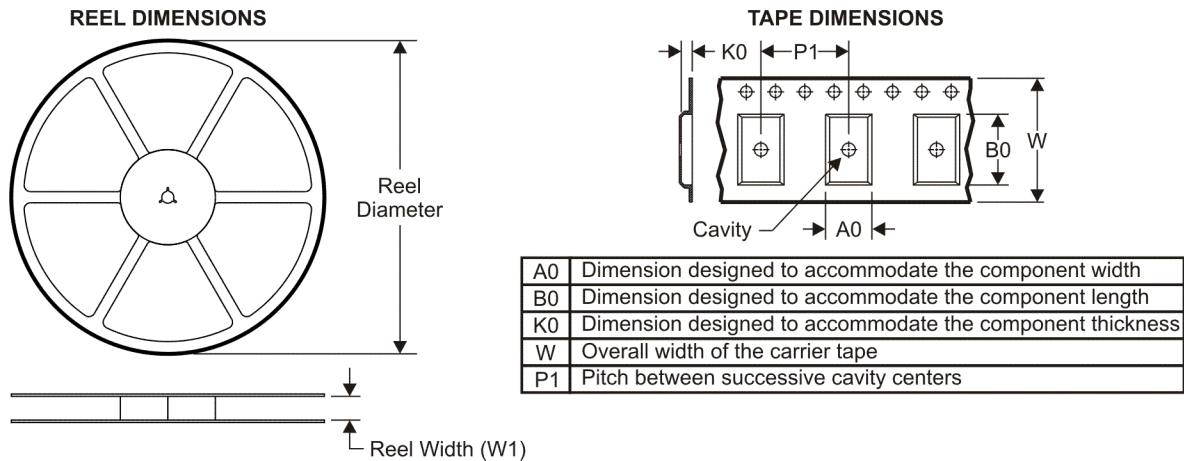
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

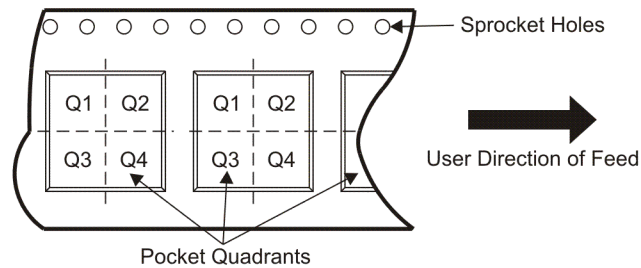
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11374DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



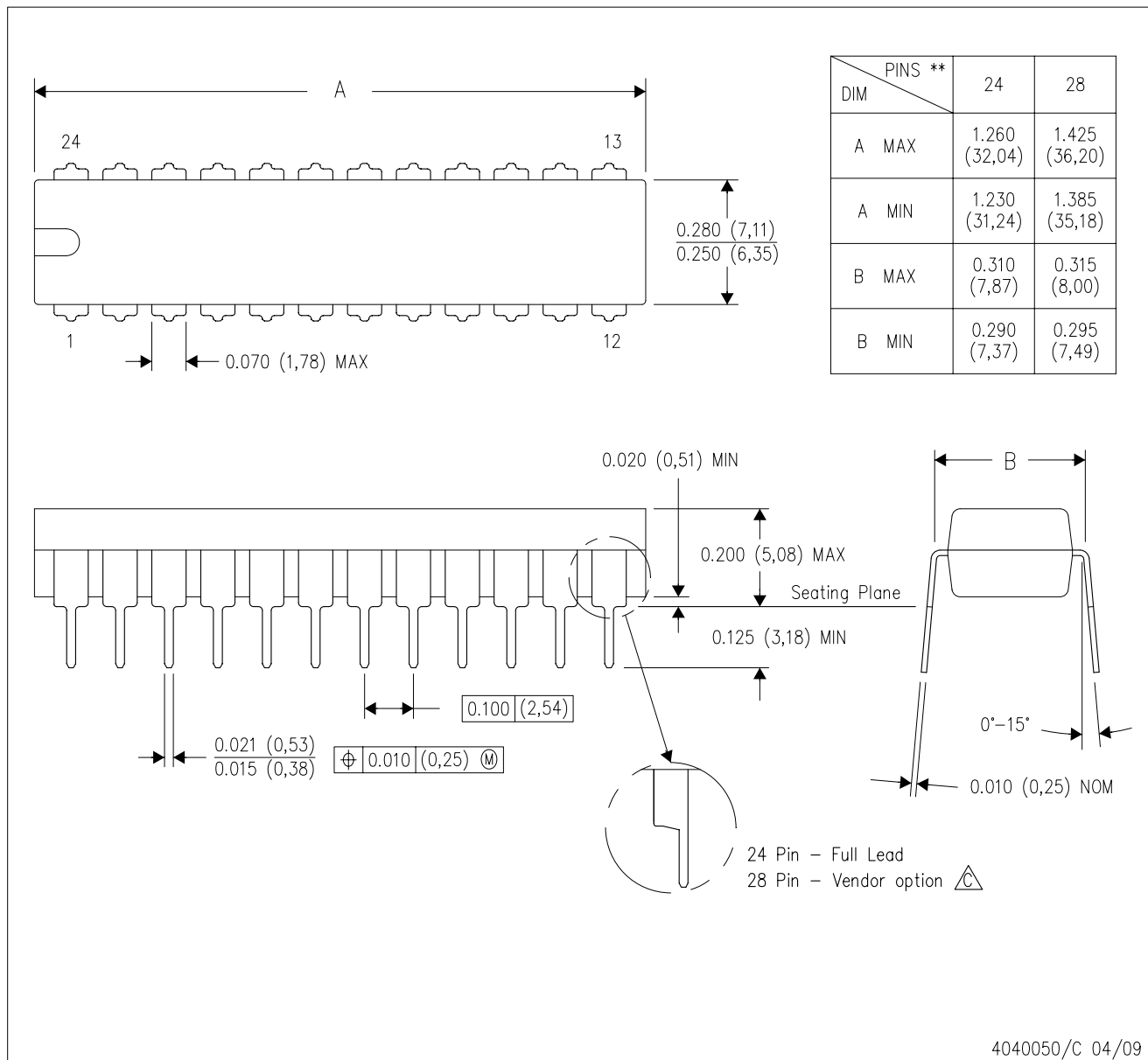
*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11374DWR	SOIC	DW	24	2000	346.0	346.0	41.0

MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ACT11374DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11374	Samples
74ACT11374DWG4	ACTIVE	SOIC	DW	24	25	TBD	Call TI	Call TI	-40 to 85		Samples
74ACT11374DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11374	Samples

(1) The marketing status values are defined as follows:

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OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

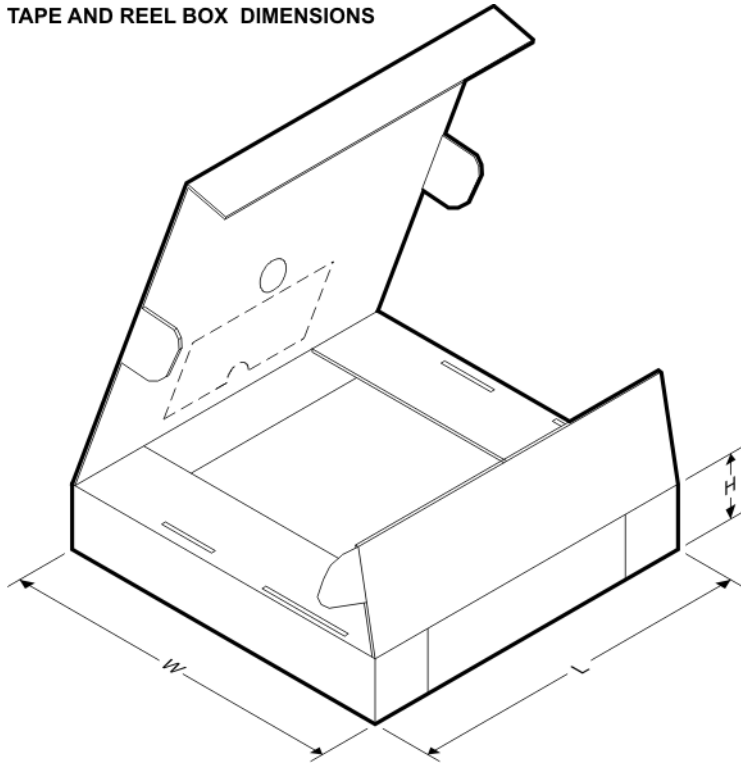


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



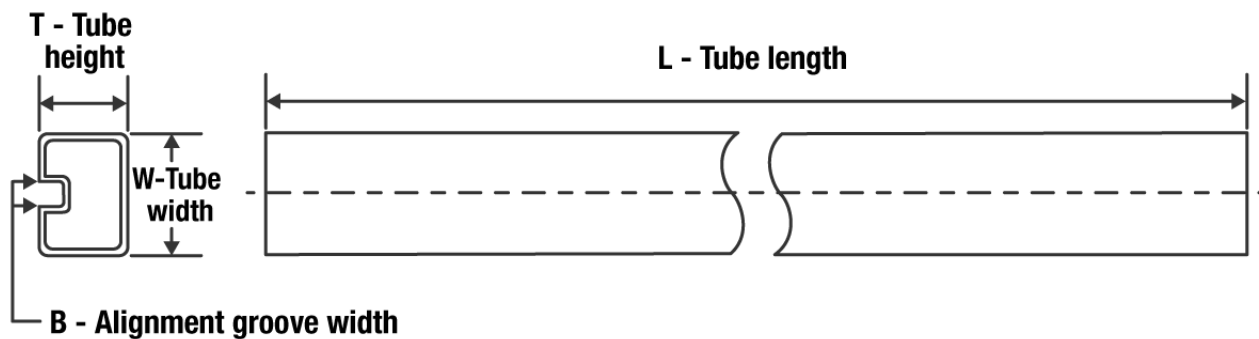
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11374DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11374DWR	SOIC	DW	24	2000	350.0	350.0	43.0

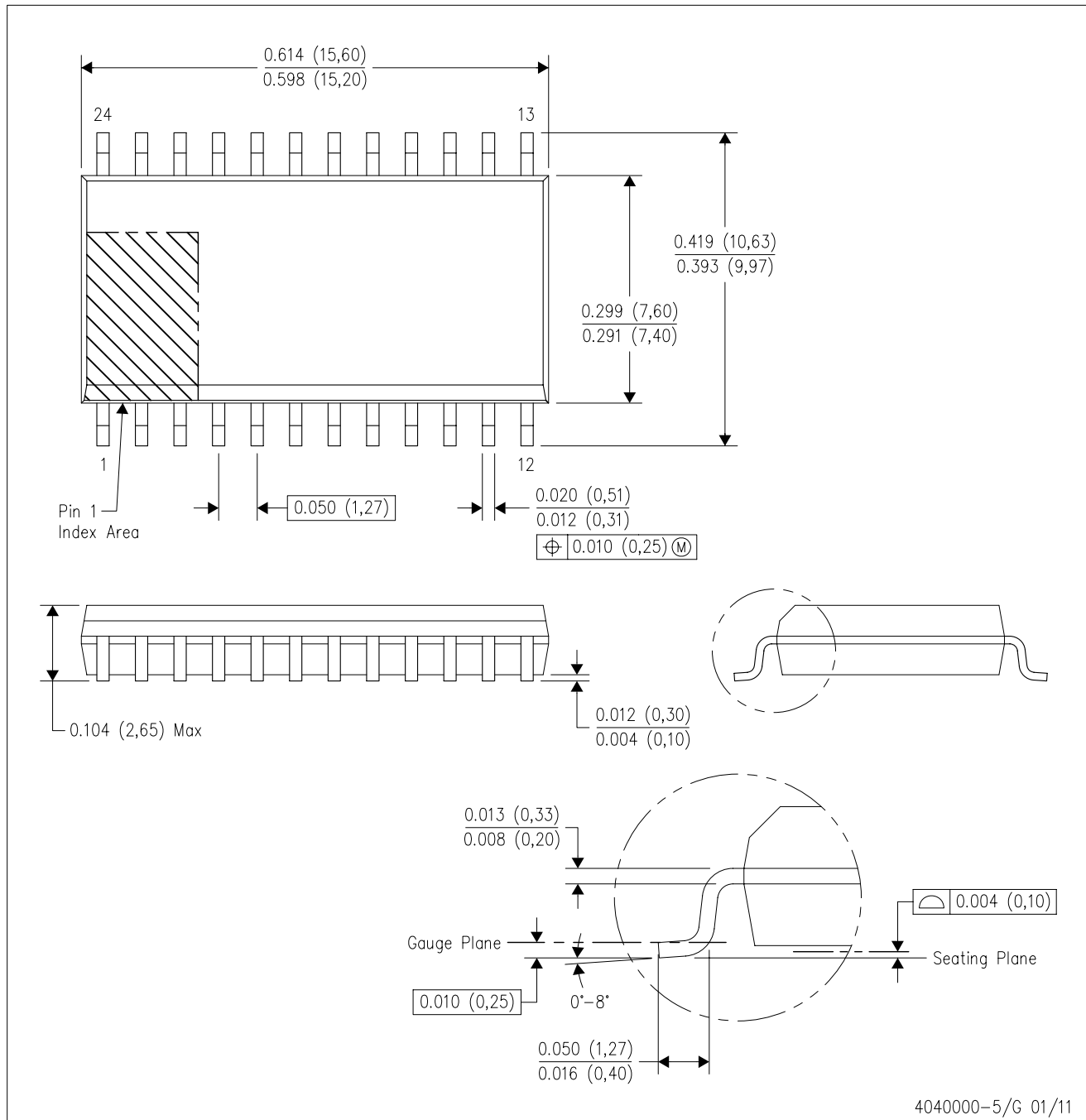
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74ACT11374DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
74ACT11374DWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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