Dual Picoampere Input Current Bipolar Op Amp

Data Sheet **AD706**

FEATURES

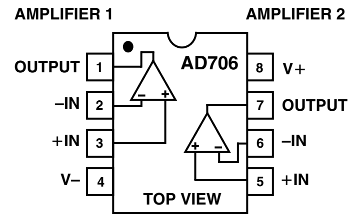
High DC Precision
100 µV Max Offset Voltage
1.5 µV/°C Max Offset Drift
200 pA Max Input Bias Current
0.5 µV p-p Voltage Noise, 0.1 Hz to 10 Hz
750 µA Supply Current
Available in 8-Lead Plastic Mini-DIP and Surface-Mount (SOIC) Packages
Available in Tape and Reel in Accordance with EIA-481A Standard
Quad Version: AD704

APPLICATIONS

Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

CONNECTION DIAGRAM

Plastic Mini-DIP (N) and Plastic SOIC (R) Packages



GENERAL DESCRIPTION

The AD706 is a dual, low power, bipolar op amp that has the low input bias current of a JFET amplifier, but which offers a significantly lower I_B drift over temperature. It utilizes superbeta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically only increases by 5× at 125°C (unlike a JFET amp, for which I_B doubles every 10°C for a 1000× increase at 125°C). The AD706 also achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has < 200 pA of bias current, the AD706 does not require the commonly used "balancing" resistor. Furthermore, the current noise is only 50 fA/$\sqrt{Hz}$, which makes this amplifier usable with very high source impedances. At 600 µA max supply current (per amplifier), the AD706 is well suited for today's high density boards.

The AD706 is an excellent choice for use in low frequency active filters in 12-bit and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD706 is internally compensated for unity gain and is available in five performance grades. The AD706J is rated over the commercial temperature range of 0°C to +70°C. The AD706A is rated for the extended industrial temperature range of –40°C to +85°C.

The AD706 is offered in two varieties of an 8-lead package: plastic mini-DIP and surface-mount (SOIC).

PRODUCT HIGHLIGHTS

1. The AD706 is a dual low drift op amp that offers JFET level input bias currents, yet has the low I_B drift of a bipolar amplifier. It may be used in circuits using dual op amps such as the LT1024.
2. The AD706 provides both low drift and high dc precision.
3. The AD706 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise.

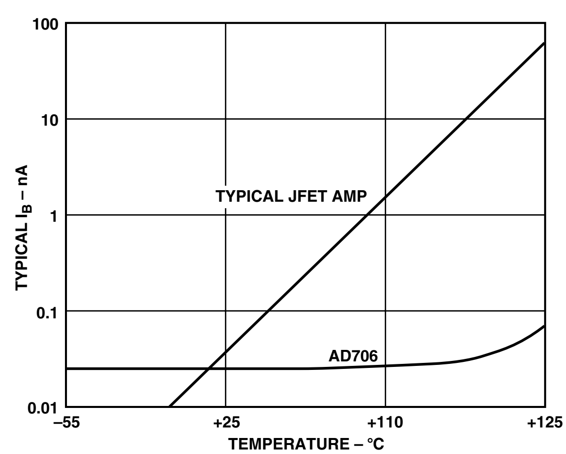


Figure 1. Input Bias Current vs. Temperature

Rev. F

Document Feedback

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Technical Support
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AD706* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- EVAL-OPAMP-2 Evaluation Board

DOCUMENTATION

Data Sheet

- AD706: Dual Picoampere Input Current Bipolar Op Amp Data Sheet

TOOLS AND SIMULATIONS

- Analog Filter Wizard
- Analog Photodiode Wizard
- AD706 SPICE Macro Models

DESIGN RESOURCES

- AD706 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD706–SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V and ±15 V dc, unless otherwise noted.)

Parameter	Conditions	AD706J/A Min	Typ	Max	Unit
INPUT OFFSET VOLTAGE					
Initial Offset			30	100	µV
Offset	T_{MIN} to T_{MAX}		40	150	µV
vs. Temperature, Average TC			0.2	1.5	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	110	132		dB
T_{MIN} to T_{MAX}	V_S = ±2.5 V to ±18 V	106	126		dB
Long Term Stability			0.3		µV/Month
INPUT BIAS CURRENT[1]	V_{CM} = 0 V		50	200	pA
	V_{CM} = ±13.5 V			250	pA
vs. Temperature, Average TC			0.3		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V			300	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V			400	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		30	150	pA
	V_{CM} = ±13.5 V			250	pA
vs. Temperature, Average TC			0.6		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V		80	250	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V		80	350	pA
MATCHING CHARACTERISTICS					
Offset Voltage				150	µV
	T_{MIN} to T_{MAX}			250	µV
Input Bias Current[2]				300	pA
	T_{MIN} to T_{MAX}			500	pA
Common-Mode Rejection		106			dB
	T_{MIN} to T_{MAX}	106			dB
Power Supply Rejection		106			dB
	T_{MIN} to T_{MAX}	104			dB
Crosstalk (Figure 2a)	@ f = 10 Hz				
	R_L = 2 kΩ		150		dB
FREQUENCY RESPONSE					
Unity Gain Crossover Frequency			0.8		MHz
Slew Rate	G = –1		0.15		V/µs
	T_{MIN} to T_{MAX}		0.15		V/µs
INPUT IMPEDANCE					
Differential			40‖2		MΩ‖pF
Common Mode			300‖2		GΩ‖pF
INPUT VOLTAGE RANGE					
Common-Mode Voltage		±13.5	±14		V
Common-Mode Rejection Ratio	V_{CM} = ±13.5 V	110	132		dB
	T_{MIN} to T_{MAX}	108	128		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		3		pA p-p
	f = 10 Hz		50		fA/$\sqrt{Hz}$
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5		µV p-p
	f = 10 Hz		17		nV/$\sqrt{Hz}$
	f = 1 kHz		15	22	nV/$\sqrt{Hz}$
OPEN-LOOP GAIN	V_O = ±12 V				
	R_{LOAD} = 10 kΩ	200	2000		V/mV
	T_{MIN} to T_{MAX}	150	1500		V/mV
	V_O = ±10 V				
	R_{LOAD} = 2 kΩ	200	1000		V/mV
	T_{MIN} to T_{MAX}	150	1000		V/mV
OUTPUT CHARACTERISTICS					
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		V
	T_{MIN} to T_{MAX}	±13	±14		V
Current	Short Circuit		±15		mA
Capacitive Load Drive Capability	Gain = +1		10,000		pF

SPECIFICATIONS (continued)

Parameter	Conditions	AD706J/A Min	Typ	Max	Unit
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±2.0		±18	V
Quiescent Current, Total			0.75	1.2	mA
	T_{MIN} to T_{MAX}		0.8	1.4	mA
TRANSISTOR COUNT	Number of Transistors		90		

NOTES

[1]Bias current specifications are guaranteed maximum at either input.

[2]Input bias current match is the difference between corresponding inputs (I_B of –IN of Amplifier 1 minus I_B of –IN of Amplifier 2).

CMRR match is the difference between $\frac{\Delta V_{OS1}}{\Delta V_{CM}}$ for Amplifier 1 and $\frac{\Delta V_{OS2}}{\Delta V_{CM}}$ for Amplifier 2, expressed in dB.

PSRR match is the difference between $\frac{\Delta V_{OS1}}{\Delta V_{SUPPLY}}$ for Amplifier 1 and $\frac{\Delta V_{OS2}}{\Delta V_{SUPPLY}}$ for Amplifier 2, expressed in dB.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation
(Total: Both Amplifiers)[2] . . . . 650 mW
Input Voltage . . . . $\pm V_S$
Differential Input Voltage[3] . . . . +0.7 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
AD706J . . . . 0°C to +70°C
AD706A . . . .–40°C to +85°C
Lead Temperature (Soldering 10 secs) . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 100°C/W
8-Lead Small Outline Package: θ_{JA} = 155°C/W

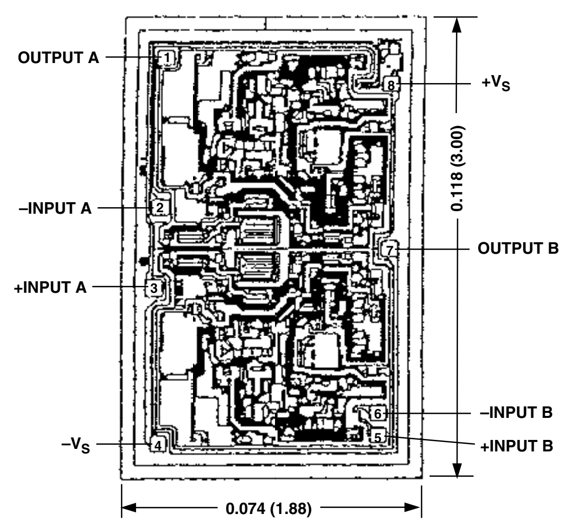
[3]The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 V, external series protection resistors should be added to limit the input current to less than 25 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

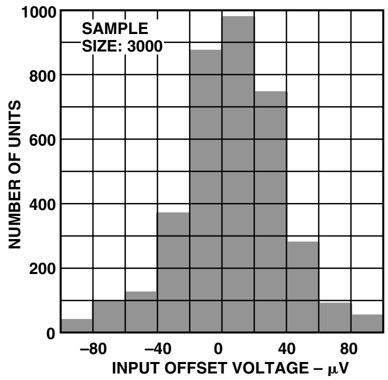
METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.

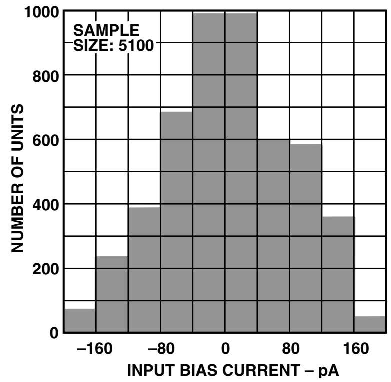


AD706–Typical Performance Characteristics

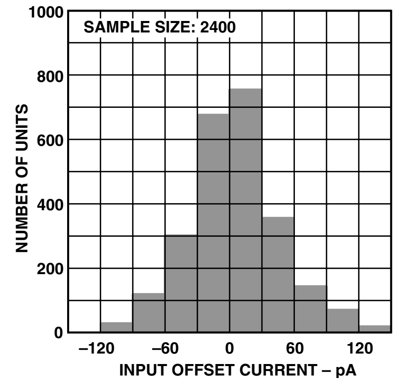
(Default Conditions: ±5 V, C_L = 5 pF, G = 2, R_g = R_f = 1 kΩ, R_L = 2 kΩ, V_O = 2 V p-p, Frequency = 1 MHz, T_A = 25°C)



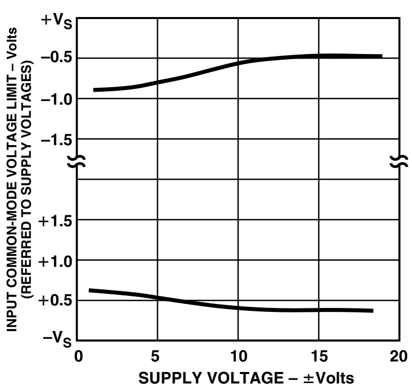
TPC 1. Typical Distribution of Input Offset Voltage



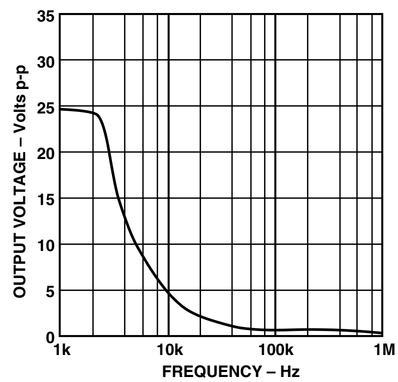
TPC 2. Typical Distribution of Input Bias Current



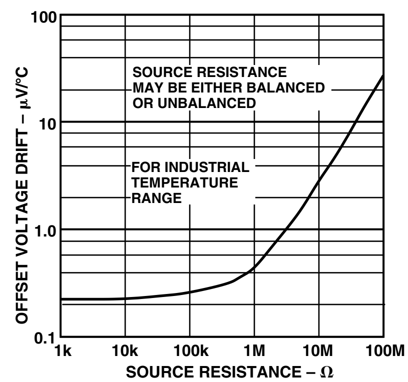
TPC 3. Typical Distribution of Input Offset Current



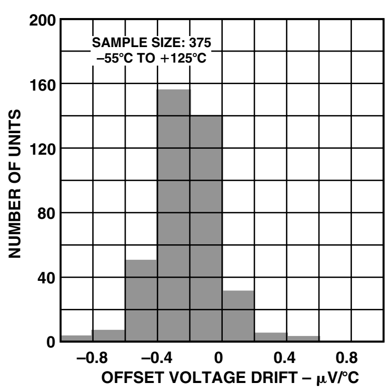
TPC 4. Input Common-Mode Voltage Range vs. Supply Voltage



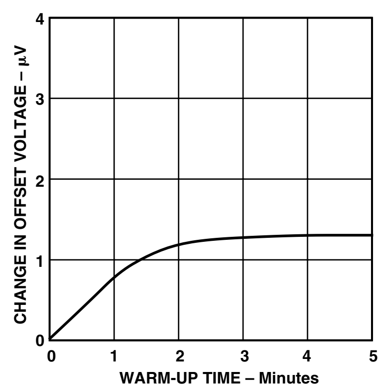
TPC 5. Large Signal Frequency Response



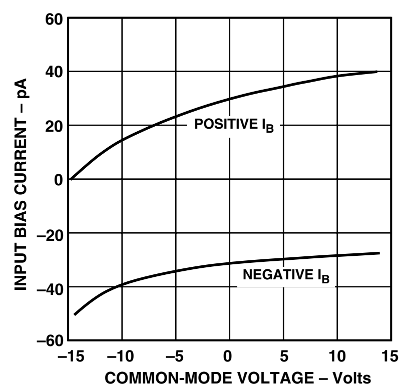
TPC 6. Offset Voltage Drift vs. Source Resistance



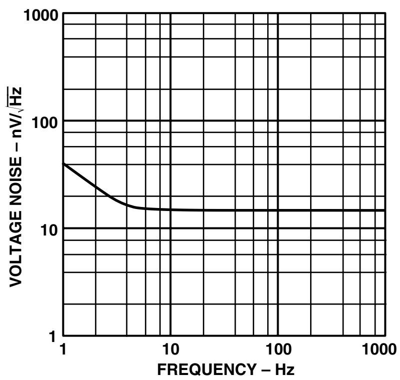
TPC 7. Typical Distribution of Offset Voltage Drift



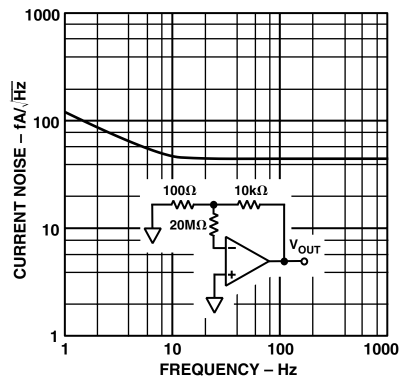
TPC 8. Change in Input Offset Voltage vs. Warm-Up Time



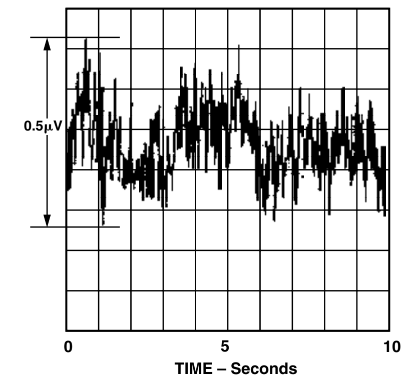
TPC 9. Input Bias Current vs. Common-Mode Voltage



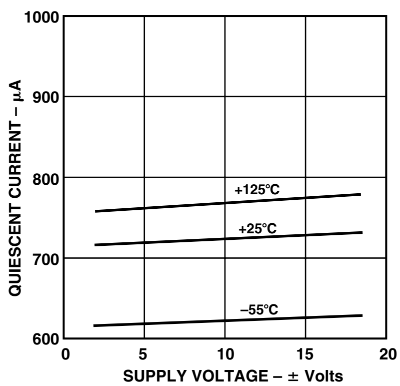
TPC 10. Input Noise Voltage Spectral Density



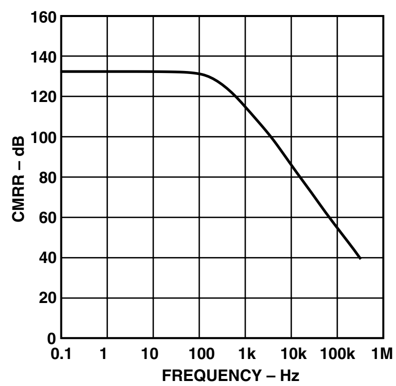
TPC 11. Input Noise Current Spectral Density



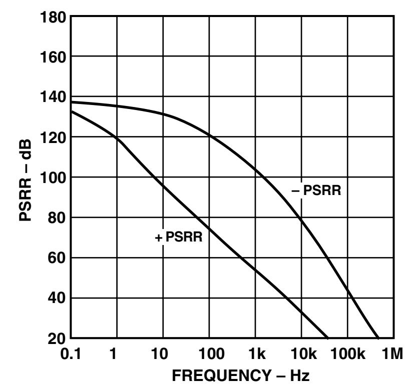
TPC 12. 0.1 Hz to 10 Hz Noise Voltage



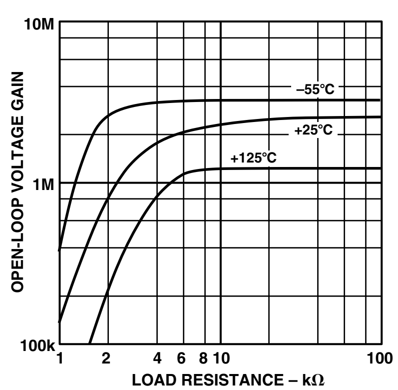
TPC 13. Quiescent Supply Current vs. Supply Voltage



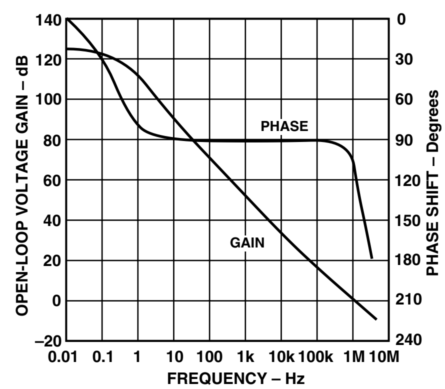
TPC 14. Common-Mode Rejection Ratio vs. Frequency



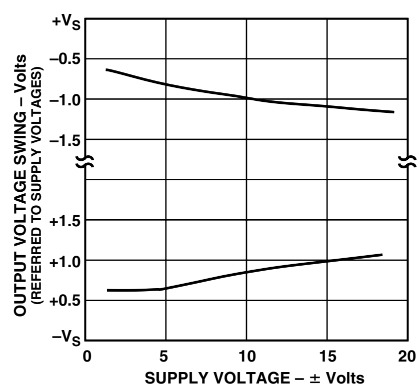
TPC 15. Power Supply Rejection Ratio vs. Frequency



TPC 16. Open-Loop Gain vs. Load Resistance vs. Load Resistance



TPC 17. Open-Loop Gain and Phase Shift vs. Frequency



TPC 18. Output Voltage Swing vs. Supply Voltage

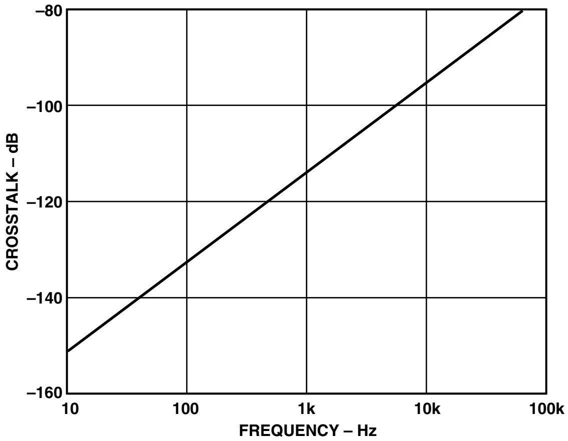


Figure 2a. Crosstalk vs. Frequency

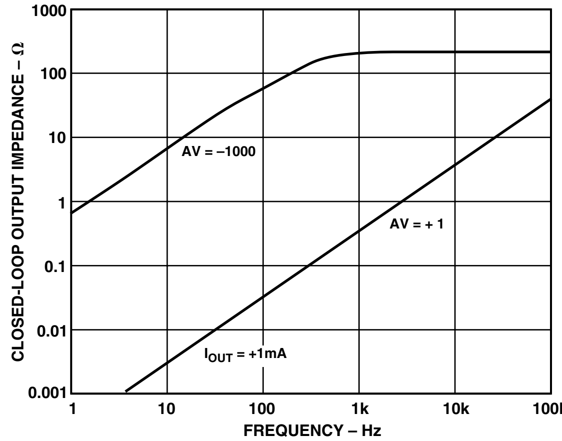


Figure 3. Magnitude of Closed-Loop Output Impedance vs. Frequency

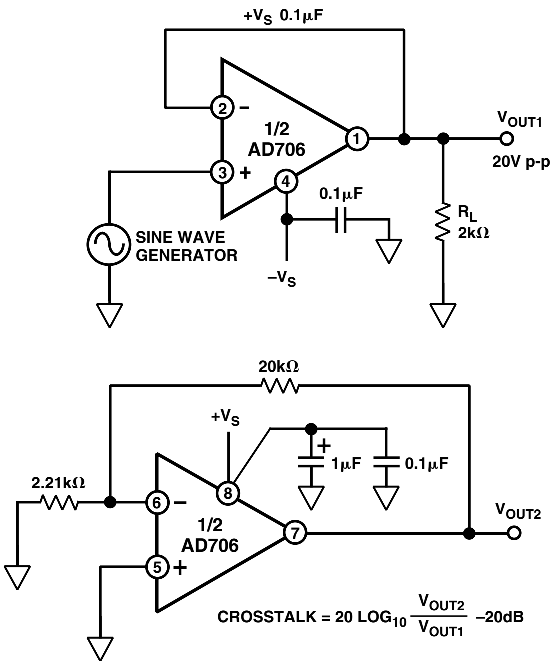


Figure 2b. Crosstalk Test Circuit

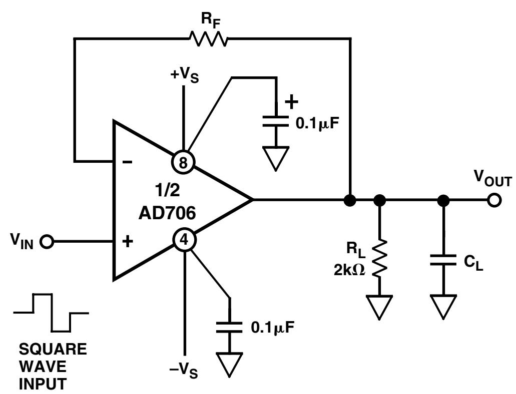


Figure 4a. Unity Gain Follower (For large signal applications, resistor R_F limits the current through the input protection diodes.)

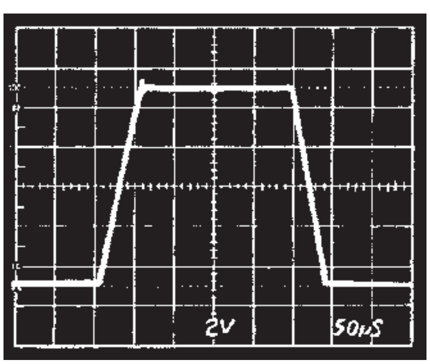


Figure 4b. Unity Gain Follower Large Signal Pulse Response, R_F = 10 kΩ, C_L = 1,000 pF

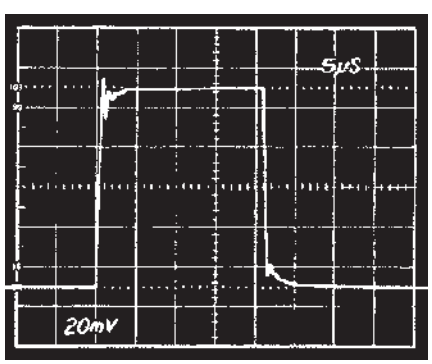


Figure 4c. Unity Gain Follower Small Signal Pulse Response, R_F = 0 Ω, C_L = 100 pF

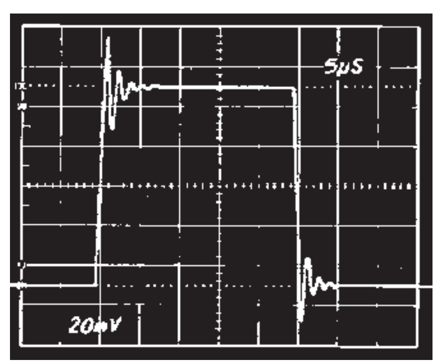


Figure 4d. Unity Gain Follower Small Signal Pulse Response, R_F = 0 Ω, C_L = 1000 pF

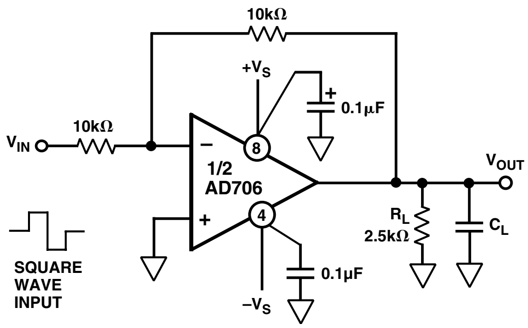


Figure 5a. Unity Gain Inverter Connection

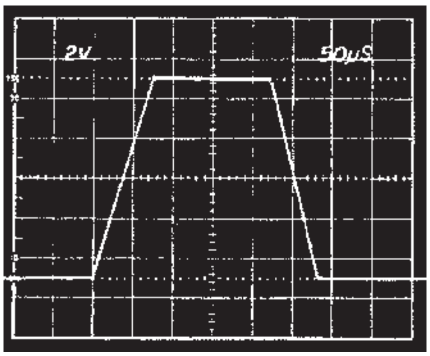


Figure 5b. Unity Gain Inverter Large Signal Pulse Response, C_L = 1,000 pF

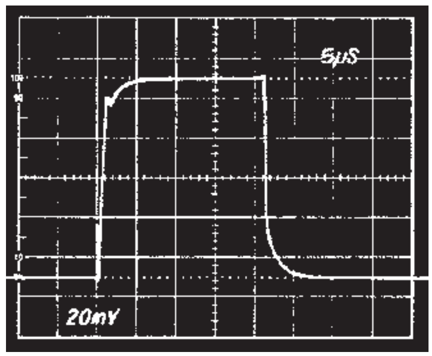


Figure 5c. Unity Gain Inverter Small Signal Pulse Response, C_L = 100 pF

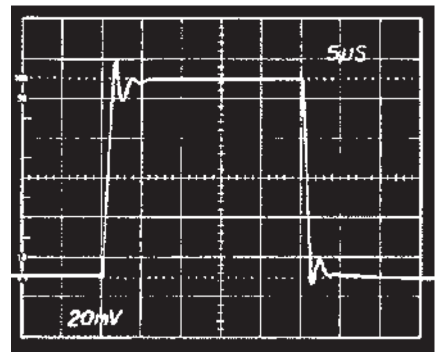


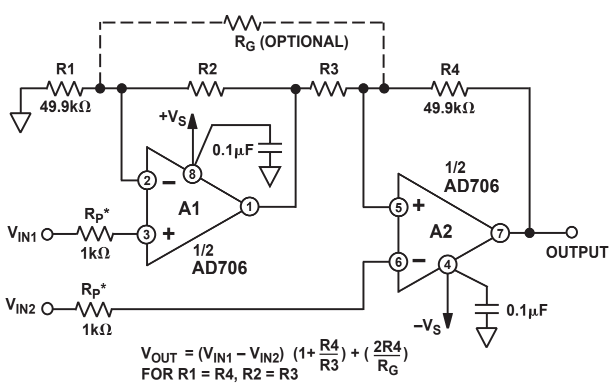
Figure 5d. Unity Gain Inverter Small Signal Pulse Response, C_L = 1000 pF

Figure 6 shows an in-amp circuit that has the obvious advantage of requiring only one AD706, rather than three op amps, with subsequent savings in cost and power consumption. The transfer function of this circuit (without R_G) is

$$V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{R4}{R3}\right)$$

for $R1 = R4$ and $R2 = R3$.

Input resistance is high, thus permitting the signal source to have an unbalanced output impedance.



*OPTIONAL INPUT PROTECTION RESISTOR FOR GAINS GREATER THAN 100 OR INPUT VOLTAGES EXCEEDING THE SUPPLY VOLTAGE.

Figure 6. Two Op Amp Instrumentation Amplifier

Furthermore, the circuit gain may be fine trimmed using an optional trim resistor, R_G. Like the three op amp circuit, CMR increases with gain, once initial trimming is accomplished—but CMR is still dependent upon the ratio matching of Resistors R1 through R4. Resistor values for this circuit, using the optional gain resistor, R_G, can be calculated using

$$R1 = R4 = 49.9\,k\Omega$$

$$R2 = R3 = \frac{49.9\,k\Omega}{0.9\,G - 1}$$

$$R_G = \frac{99.8\,k\Omega}{0.06\,G}$$

where G = The desired circuit gain.

Table I provides practical 1% resistance values. Note that without resistor R_G, R2 and R3 = 49.9 kΩ/G–1.

Table I. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 6

Circuit Gain	Gain of A1	Gain of A2	R2, R3	R1, R4
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	499 Ω	49.9 kΩ
1001	1.001	1001	49.9 Ω	49.9 kΩ

For a much more comprehensive discussion of in-amp applications, refer to the *Instrumentation Amplifier Applications Guide*—available free from Analog Devices, Inc.

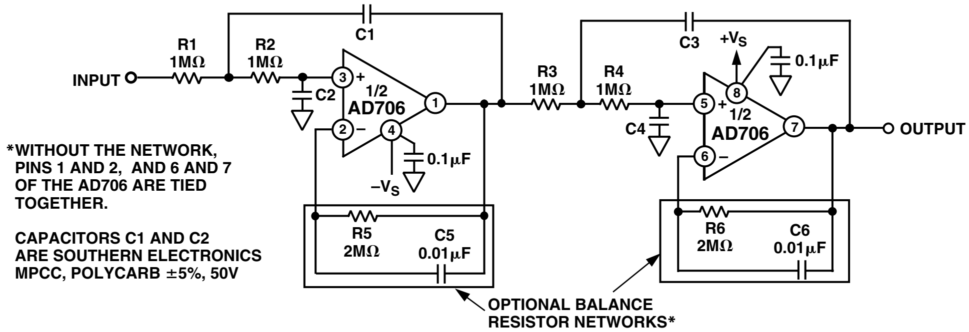


Figure 7. 1 Hz, 4-Pole Active Filter

1 Hz, 4-Pole, Active Filter

Figure 7 shows the AD706 in an active filter application. An important characteristic of the AD706 is that both the input bias current, input offset current, and their drift remain low over most of the op amp's rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor. Adding the balancing resistor enhances performance at high temperatures, as shown by Figure 8.

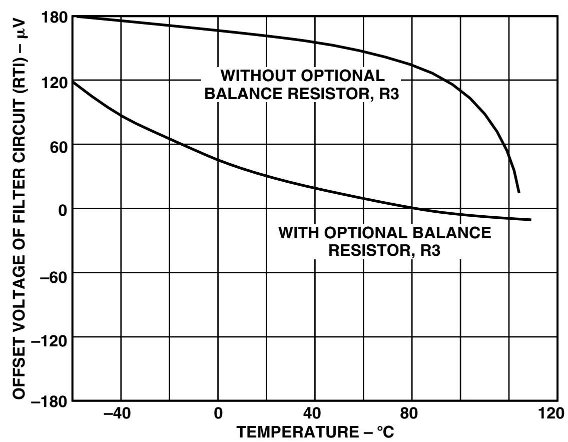


Figure 8. V_{OS} vs. Temperature Performance of the 1 Hz Filter

Table II. 1 Hz, 4-Pole, Low Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

NOTE
Specified Values are for a –3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly, i.e. for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

OUTLINE DIMENSIONS

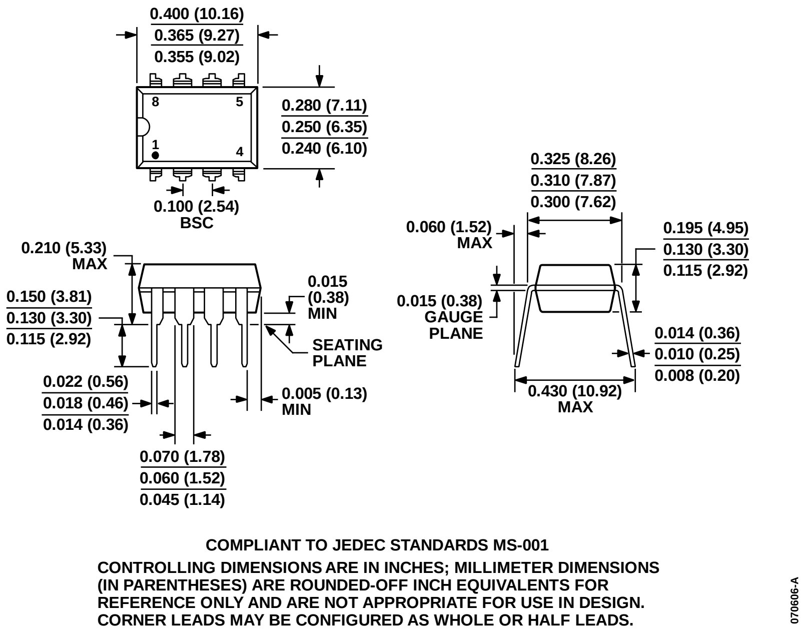


Figure 9. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

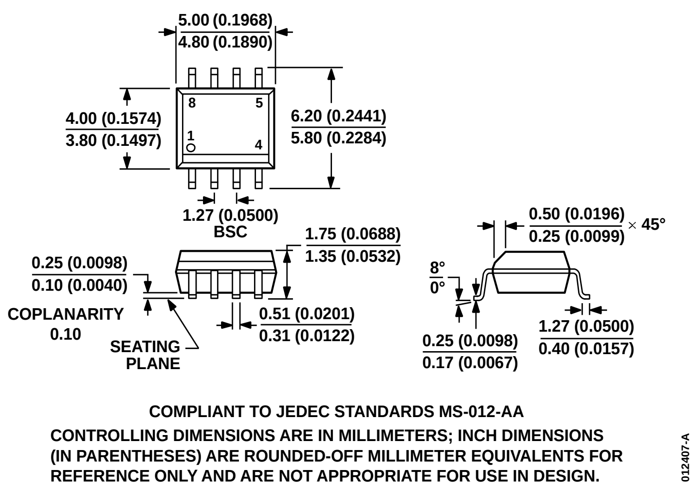


Figure 10. 8-Lead Plastic Dual-in-line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD706AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD706ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD706ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N, 13″Tape and Reel	R-8
AD706ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8
AD706JNZ	0°C to + 70°C	8-Lead PDIP	N-8
AD706JRZ	0°C to + 70°C	8-Lead SOIC_N	R-8
AD706JRZ-REEL	0°C to + 70°C	8-Lead SOIC_N, 13″Tape and Reel	R-8
AD706JRZ-REEL7	0°C to + 70°C	8-Lead SOIC_N, 7″Tape and Reel	R-8

REVISION HISTORY

8/2017—Rev. E to Rev. F

Changes to Figure 6 ... 6
Updated Outline Dimensions ... 10
Changes to Ordering Guide ... 10

10/2003—Rev. D to Rev. E

Removed K Version ... Universal
Changes to Features and Product Description ... 1
Renumbered TPC's ... 4
Renumbered Figured ... 6
Updated Outline Dimensions ... 9

10/2002—Rev. C to Rev. D

Deleted 8-Lead CERDIP (Q-8) Package ... Universal
Changes to Features and Product Description ... 1
Changes to Specifications Section ... 2
Changes to Absolute Maximum Ratings Section ... 3
Changes to Ordering Guide ... 3
Updated Outline Dimensions ... 15

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