ADC1175 8-Bit, 20MHz, 60mW A/D Converter

Check for Samples: ADC1175

FEATURES

- **Internal Sample-and-Hold Function**
- **Single +5V Operation**
- **Internal Reference Bias Resistors**
- **Industry Standard Pinout**
- **TRI-STATE Outputs**

APPLICATIONS

- **Video Digitization**
- **Digital Still Cameras**
- **Personal Computer Video Cameras**
- **CCD Imaging**
- **Electro-Optics**

KEY SPECIFICATIONS

- **Resolution 8Bits**
- **Maximum Sampling Frequency 20Msps (min)**
- **DNL 0.75 LSB (max)**
- **ENOB 7.5 Bits (typ)**
- **Power Consumption (excluding I_{REF}) 60mW (typ)**

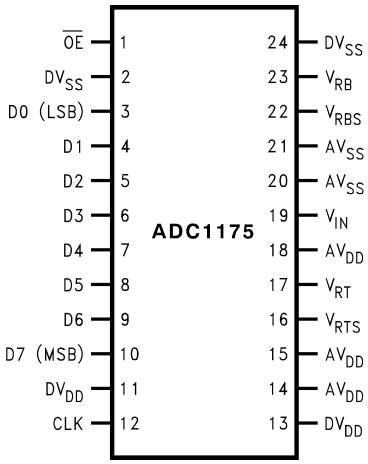
DESCRIPTION

The ADC1175 is a low power, 20 Msps analog-to-digital converter that digitizes signals to 8 bits while consuming just 60 mW of power (typ). The ADC1175 uses a unique architecture that achieves 7.5 Effective Bits. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video, imaging and communications applications, including use in portable equipment. Furthermore, the ADC1175 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC1175's reference ladder is available for connections, enabling a wide range of input possibilities.

The ADC1175 is offered in a TSSOP. It is designed to operate over the commercial temperature range of -20°C to +75°C.

PIN CONFIGURATION



ADC1175 Pin Configuration
TSSOP Package
See Package Number PW

BLOCK DIAGRAM

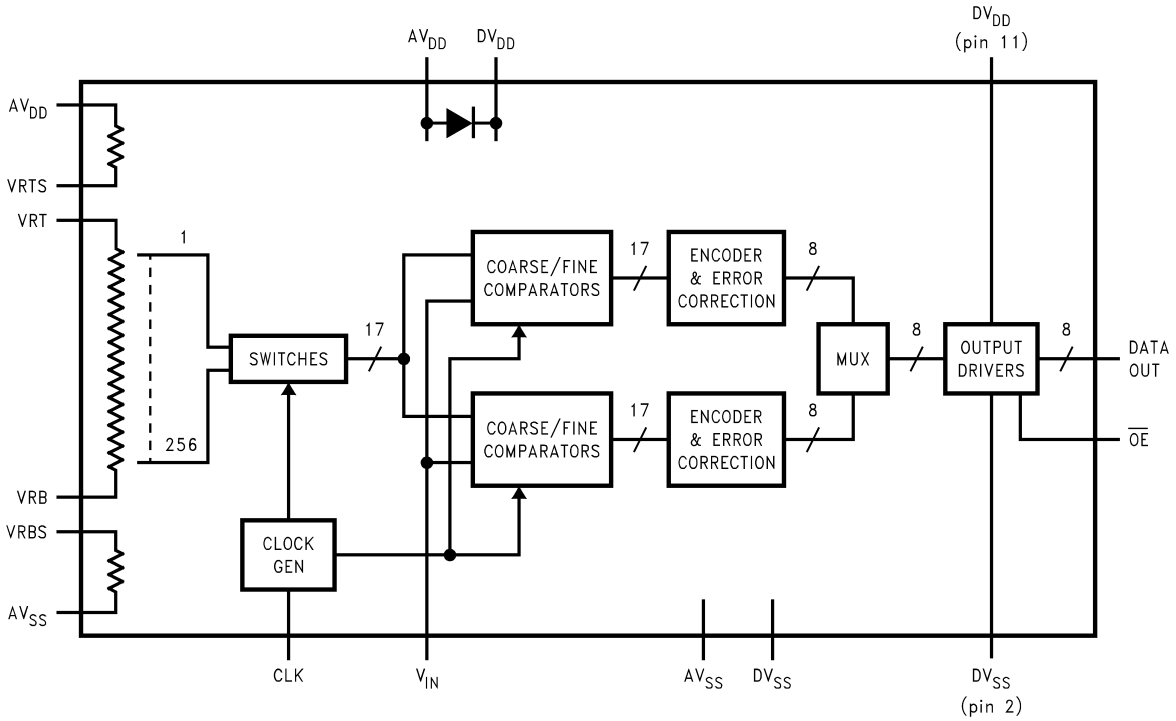
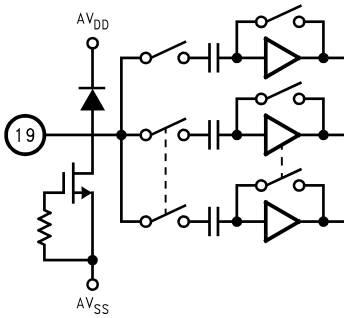
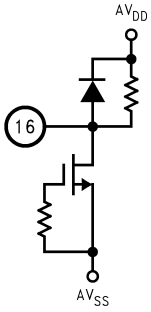
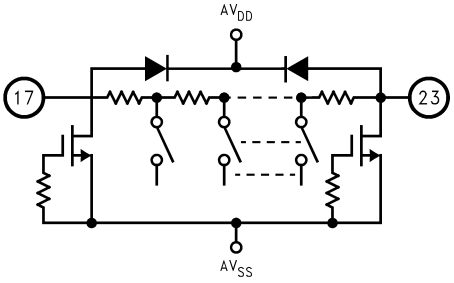
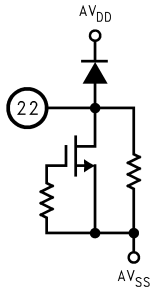
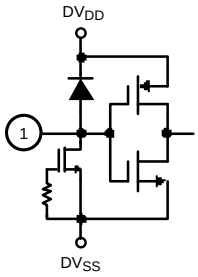


Figure 1.

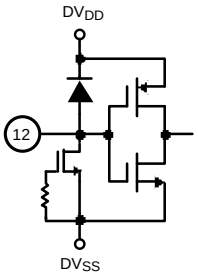
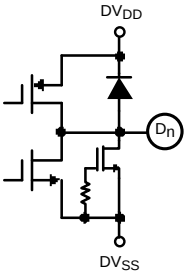
PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
19	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
16	V_{RTS}		Reference Top Bias with internal pull-up resistor. Short this pin to V_{RT} to self bias the reference ladder.

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
17	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to AV_{DD}. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See REFERENCE INPUTS for more information.
23	V_{RB}		Analog Input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0V to 4.0V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See REFERENCE INPUTS for more information.
22	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self bias the reference ladder.
1	$\overline{OE}$		CMOS/TTL compatible Digital input that, when low, enables the digital outputs of the ADC1175. When high, the outputs are in a high impedance state.

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
12	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
3 thru 10	D0-D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the $\overline{OE}$ pin low.
13	DV_{DD}		Positive digital supply pin. Connect to a clean voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10µF capacitor and a 0.1µF ceramic chip capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
11	DV_{DD}		This digital supply pin supplies power for the digital output drivers. This pin should be connected to a supply source in the range of 2.5V to the Pin 13 potential.
2, 24	DV_{SS}		The ground return for the digital supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175.
14, 15, 18	AV_{DD}		Positive analog supply pin. Connected to a quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
20, 21	AV_{SS}		The ground return for the analog supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175 package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

AV_{DD}, DV_{DD}		6.5V
Voltage on Any Pin		−0.3V to 6.5V
V_{RT}, V_{RB}		AV_{SS} to AV_{DD}
CLK, $\overline{OE}$ Voltage		−0.5 to (AV_{DD} + 0.5V)
Digital Output Voltage		DV_{SS} to DV_{DD}
Input Current (4)		±25mA
Package Input Current (4)		±50mA
Package Dissipation at 25°C		See (5)
ESD Susceptibility (6)	Human Body Model	2000V
	Machine Model	200V
Soldering Temp., Infrared, 10 sec.		300°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see CONVERTER ELECTRICAL CHARACTERISTICS. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AV_{SS} = DV_{SS} = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, less than AV_{SS} or DV_{SS}, or greater than AV_{DD} or DV_{DD}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperatures ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature, T_A, and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC1175 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220 pF discharged through ZERO Ω.

OPERATING RATINGS(1)(2)

Operating Temperature Range	−20°C ≤ T_A ≤ +75°C
Supply voltage (AV_{DD}, DV_{DD})	+4.75V to +5.25V
AV_{DD} − DV_{DD}	<0.5V
$\lvert AV_{SS} - DV_{SS} \rvert$	0V to 100 mV
Pin 13 - Pin 11 Voltage	<0.5V
V_{RT}	1.0V to V_{DD}
V_{RB}	0V to 4.0V
V_{RT} - V_{RB}	1V to 2.8V
V_{IN} Voltage Range	V_{RB} to V_{RT}

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see CONVERTER ELECTRICAL CHARACTERISTICS. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AV_{SS} = DV_{SS} = 0V, unless otherwise specified.

PACKAGE THERMAL RESISTANCE

Package	θ_{JA}
TSSOP-24	92°C / W

CONVERTER ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{DD} = DV_{DD} = +5.0V_{DC}, $\overline{OE}$ = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 20MHz at 50% duty cycle. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C (1)(2)

Symbol	Parameter	Conditions		Typical(3)	Limits(3)	Units
DC Accuracy						
INL	Integral Non Linearity	f_{CLK} = 20 MHz		±0.5	**±1.3**	LSB (max)
INL	Integral Non Linearity	f_{CLK} = 30 MHz		±1.0		LSB (max)
DNL	Differential Non Linearity	f_{CLK} = 20 MHz		±0.35	**±0.75**	LSB (max)
DNL	Differential Non Linearity	f_{CLK} = 30 MHz		±1.0		LSB (max)
	Missing Codes				**0**	(max)
E_{OT}	Top Offset			−24		mV
E_{OB}	Bottom Offset			+37		mV
Video Accuracy						
DP	Differential Phase Error	f_{in} = 4.43 MHz sine wave f_{CLK} = 17.7 MHz		0.5		Degree
DG	Differential Gain Error	f_{in} = 4.43 MHz sine wave f_{CLK} = 17.7 MHz		0.4		%
Analog Input and Reference Characteristics						
V_{IN}	Input Range			2.0	**V_{RB}** **V_{RT}**	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 1.5V + 0.7Vrms	(CLK LOW)	4		pF
			(CLK HIGH)	11		
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Analog Input Bandwidth			120		MHz
R_{RT}	Top Reference Resistor			360		Ω
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		300	200 400	Ω (min) Ω (max)
R_{RB}	Bottom Reference Resistor			90		Ω
I_{REF}	Reference Ladder Current	V_{RT} =V_{RTS}, V_{RB} =V_{RBS}		7	**4.8** **9.3**	mA (min) mA (max)
		V_{RT} =V_{RTS},V_{RB} =AV_{SS}		8	**5.4** **10.5**	mA (min) mA (max)
V_{RT}	Reference Top Self Bias Voltage	V_{RT} connected to V_{RTS} V_{RB} connected to V_{RBS}		2.6		V
V_{RB}	Reference Bottom Self Bias Voltage	V_{RT} connected to V_{RTS} V_{RB} connected to V_{RBS}		0.6	**0.55** **0.65**	V (min) V (max)
V_{RTS} - V_{RBS}	Self Bias Voltage Delta	V_{RT} connected to V_{RTS} V_{RB} connected to V_{RBS}		2	**1.89** **2.15**	V (min) V (max)
		V_{RT} connected to V_{RTS} V_{RB} connected to AV_{SS}		2.3		V
V_{RT} - V_{RB}	Reference Voltage Delta			2	**1.0** **2.8**	V (min) V (max)

(1) The analog inputs are protected as shown below. Input voltage magnitudes up to 6.5V or to 500 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DD} or below GND by more than 50 mV. As an example, if AV_{DD} is 4.75V_{DC}, the full-scale input voltage must be ≤4.80V_{DC} to ensure accurate conversions. See Figure 2.

(2) To ensure accuracy, it is required that AV_{DD} and DV_{DD} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for AV_{DD} = DV_{DD} = +5.0V_{DC}, $\overline{OE}$ = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 20MHz at 50% duty cycle. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C (1)(2)

Symbol	Parameter	Conditions	Typical(3)	Limits(3)	Units
Power Supply Characteristics					
IA_{DD}	Analog Supply Current	DV_{DD} = AV_{DD} =5.25V	9.5		mA
ID_{DD}	Digital Supply Current	DV_{DD} = AV_{DD} =5.25V	2.5		mA
IAV_{DD} + IDV_{DD}	Total Operating Current	DV_{DD} AV_{DD} =5.25V, f_{CLK} = 20 MHz	12	**17**	mA (max)
		DV_{DD} AV_{DD} =5.25V, f_{CLK} = 30 MHz	13		
		DV_{DD} = AV_{DD} =5.25V, CLK Low(4)	9.6		mA
	Power Consumption	DV_{DD} = AV_{DD} =5.25V, f_{CLK} = 20 MHz	60	**85**	mW (max)
		DV_{DD} = AV_{DD} =5.25V, f_{CLK} = 30 MHz	65		mW
CLK, $\overline{OE}$ Digital Input Characteristics					
V_{IH}	Logical High Input Voltage	DV_{DD} = AV_{DD} = +5.25V		**3.0**	V (min)
V_{IL}	Logical Low Input Voltage	DV_{DD} = AV_{DD} = +5.25V		**1.0**	V (max)
I_{IH}	Logical High Input Current	V_{IH} = DV_{DD} = AV_{DD} = +5.25V	5		µA
I_{IL}	Logic Low Input Current	V_{IL} = 0V, DV_{DD} = AV_{DD} = +5.25V	−5		µA
C_{IN}	Logic Input Capacitance		5		pF
Digital Output Characteristics					
I_{OH}	High Level Output Current	DV_{DD} = 4.75V, V_{OH} = 2.4V		**−1.1**	mA (max)
I_{OL}	Low Level Output Current	DV_{DD} = 4.75V, V_{OL} = 0.4V		**1.6**	mA (min)
I_{OZH}, I_{OZL}	Tri-State Leakage Current	DV_{DD} = 5.25V $\overline{OE}$ = DV_{DD}, V_{OL} = 0V or V_{OH} = DV_{DD}	±20		µA
AC Electrical Characteristics					
f_{C1}	Maximum Conversion Rate		30	**20**	MHz (min)
f_{C2}	Minimum Conversion Rate		1		MHz
t_{OD}	Output Delay	CLK rise to data rising	19.5		ns
		CLK rise to data falling	16		ns
	Pipeline Delay (Latency)		2.5		Clock Cycles
t_{DS}	Sampling (Aperture) Delay	CLK low to acquisition of data	3		ns
t_{AJ}	Aperture Jitter		30		ps rms
t_{OH}	Output Hold Time	CLK high to data invalid	10		ns
t_{EN}	$\overline{OE}$ Low to Data Valid	Loaded as in Figure 18	11		ns
t_{DIS}	$\overline{OE}$ High to High Z State	Loaded as in Figure 18	15		ns
ENOB	Effective Number of Bits	f_{IN} = 1.31 MHz, V_{IN} = FS - 2 LSB	7.5	**7.0**	Bits (min)
		f_{IN} = 4.43 MHz, V_{IN} = FS - 2 LSB	7.3		
		f_{IN} = 9.9 MHz, V_{IN} = FS - 2 LSB	7.2		
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	6.5		
SINAD	Signal-to- Noise & Distortion	f_{IN} = 1.31 MHz, V_{IN} = FS - 2 LSB	46.9	**43**	dB (min)
		f_{IN} = 4.43 MHz, V_{IN} = FS - 2 LSB	45.7		
		f_{IN} = 9.9 MHz, V_{IN} = FS - 2 LSB	45.1		
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	40.9		
SNR	Signal-to- Noise Ratio	f_{IN} = 1.31 MHz, V_{IN} = FS - 2 LSB	47.6	**44**	dB (min)
		f_{IN} = 4.43 MHz, V_{IN} = FS - 2 LSB	46		
		f_{IN} = 9.9 MHz, V_{IN} = FS - 2 LSB	46.1		
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	42.1		

(4) At least two clock cycles must be presented to the ADC1175 after power up. See THE ADC1175 CLOCK for details.

CONVERTER ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for AV_{DD} = DV_{DD} = +5.0V_{DC}, $\overline{OE}$ = 0V, V_{RT} = +2.6V, V_{RB} = 0.6V, C_L = 20 pF, f_{CLK} = 20MHz at 50% duty cycle. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C (1)(2)

Symbol	Parameter	Conditions	Typical(3)	Limits(3)	Units
SFDR	Spurious Free Dynamic Range	f_{IN} = 1.31 MHz, V_{IN} = FS - 2 LSB	56		dB
		f_{IN} = 4.43 MHz, V_{IN} = FS - 2 LSB	58		
		f_{IN} = 9.9 MHz, V_{IN} = FS - 2 LSB	53		
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	47		
THD	Total Harmonic Distortion	f_{IN} = 1.31 MHz, V_{IN} = FS - 2 LSB	−55		dB
		f_{IN} = 4.43 MHz, V_{IN} = FS - 2 LSB	−57		
		f_{IN} = 9.9 MHz, V_{IN} = FS - 2 LSB	−52		
		f_{IN} = 4.43 MHz, f_{CLK} = 30 MHz	−47		

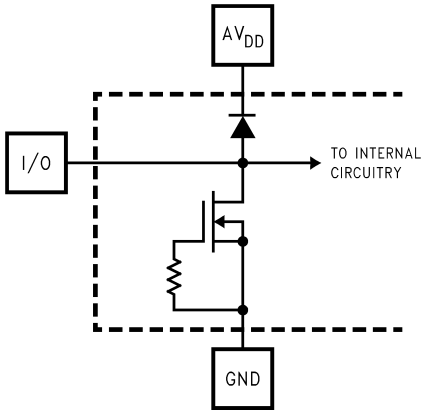


Figure 2.

TYPICAL PERFORMANCE CHARACTERISTICS

INL vs. Temp at f_{CLK}

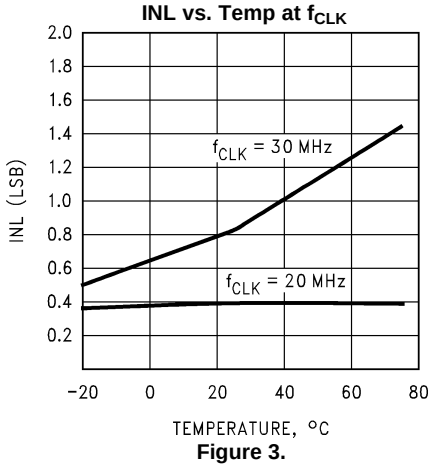


Figure 3.

DNL vs. Temp at f_{CLK}

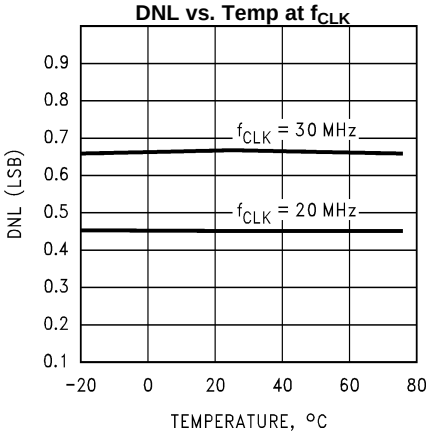


Figure 4.

SNR vs. Temp at f_{CLK}

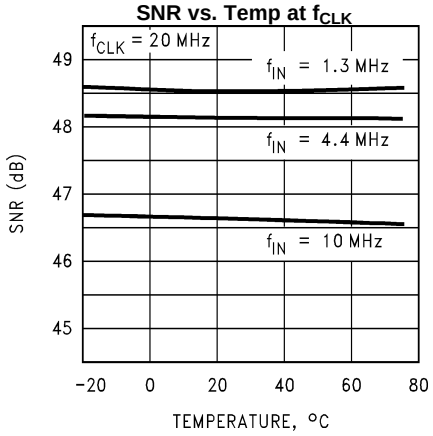


Figure 5.

SNR vs. Temp at f_{CLK}

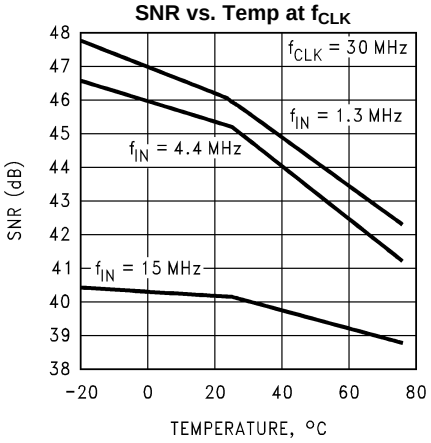


Figure 6.

THD vs. Temp

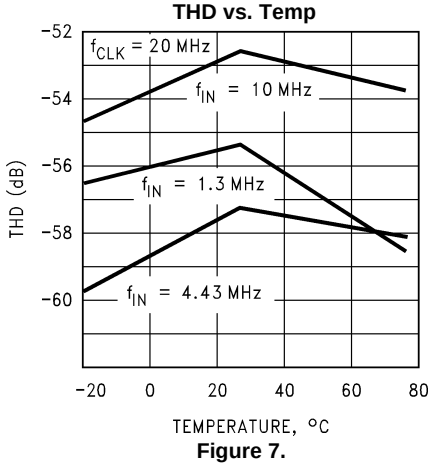


Figure 7.

THD vs. Temp

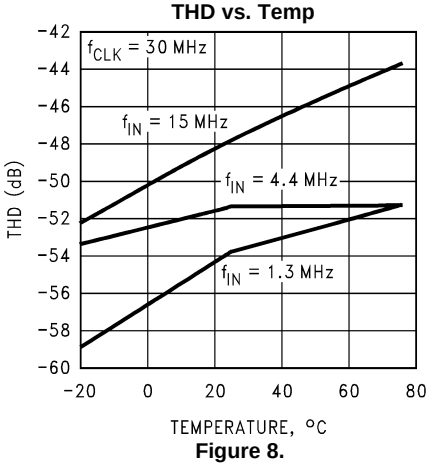


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SINAD/ENOB vs. Temp

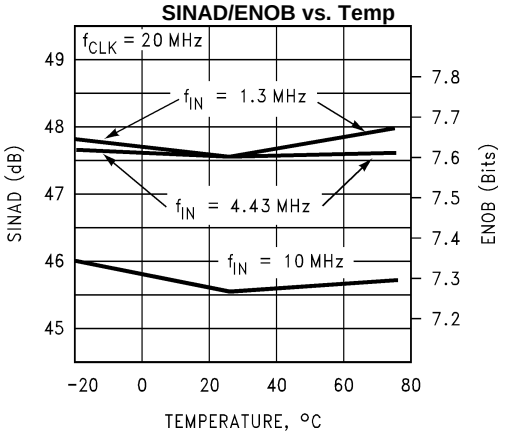


Figure 9.

SINAD/ENOB vs. Temp

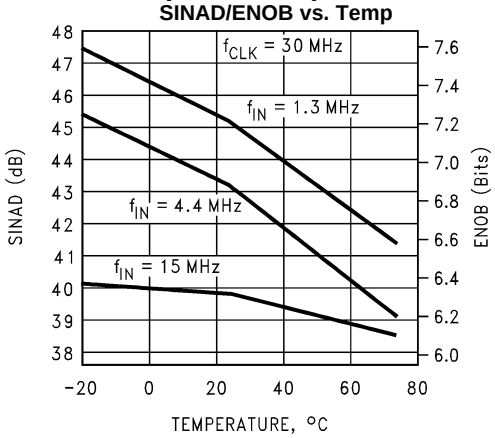


Figure 10.

SINAD and ENOB vs. Clock Duty Cycle

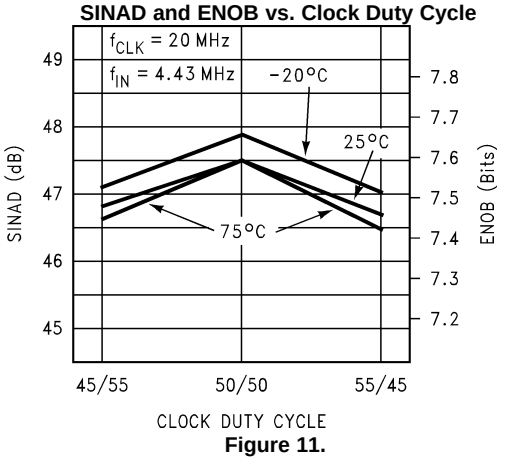


Figure 11.

SFDR vs. Temp and f_{IN}

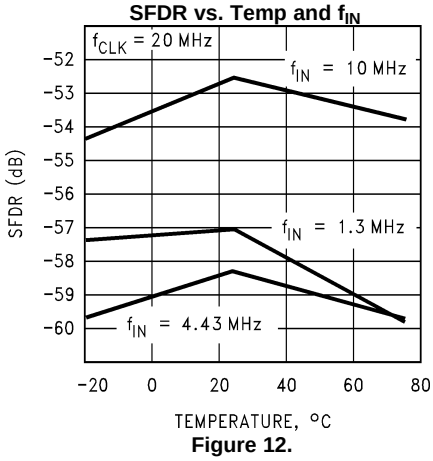


Figure 12.

SFDR vs. Temp and f_{IN}

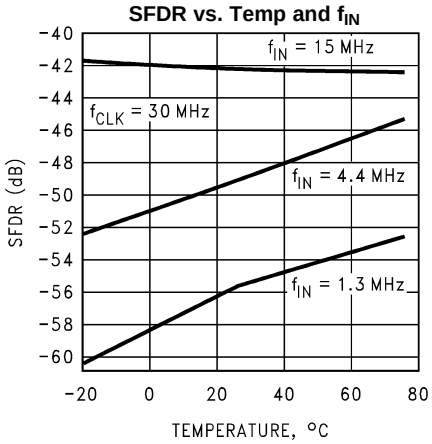


Figure 13.

Differential Gain vs. Temperature

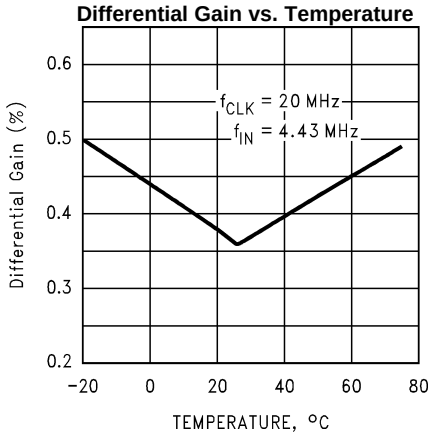


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Differential Phase vs. Temperature

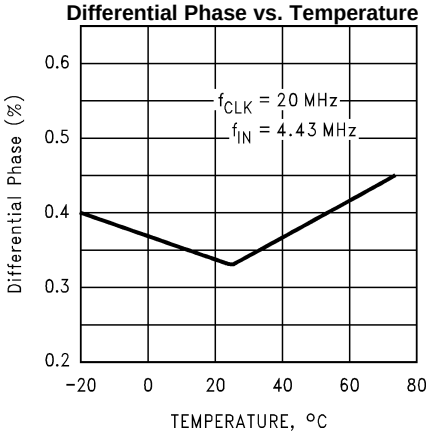


Figure 15.

Spectral Response at f_{CLK} = 20 MSPS

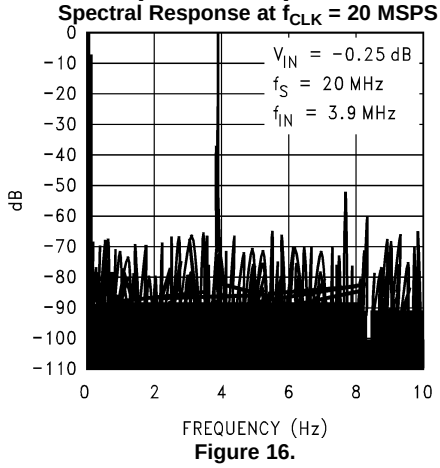


Figure 16.

SPECIFICATION DEFINITIONS

ANALOG INPUT BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

APERTURE JITTER is the time uncertainty of the sampling point (t_{DS}), or the range of variation in the sampling delay.

BOTTOM OFFSET is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom offset is defined as $E_{OB} = V_{ZT} - V_{RB}$, where V_{ZT} is the first code transition input voltage. Note that this is different from the normal Zero Scale Error.

DIFFERENTIAL GAIN ERROR is the percentage difference between the output amplitudes of a high frequency reconstructed sine wave at two different d.c. levels.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DIFFERENTIAL PHASE ERROR is the difference in the output phase of a reconstructed small signal sine wave at two different d.c. levels.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½LSB below the first code transition) through positive full scale (½LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any give sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

SAMPLING (APERTURE) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{DS} after the clock goes low.

SIGNAL TO NOISE RATIO (SNR) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOP OFFSET is the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale and is defined as $E_{OT} = V_{FT} - V_{RT}$. Where V_{FT} is the full scale transition input voltage. Note that this is different from the normal Full Scale Error.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first six harmonic components, to the rms value of the input signal.

TIMING DIAGRAM

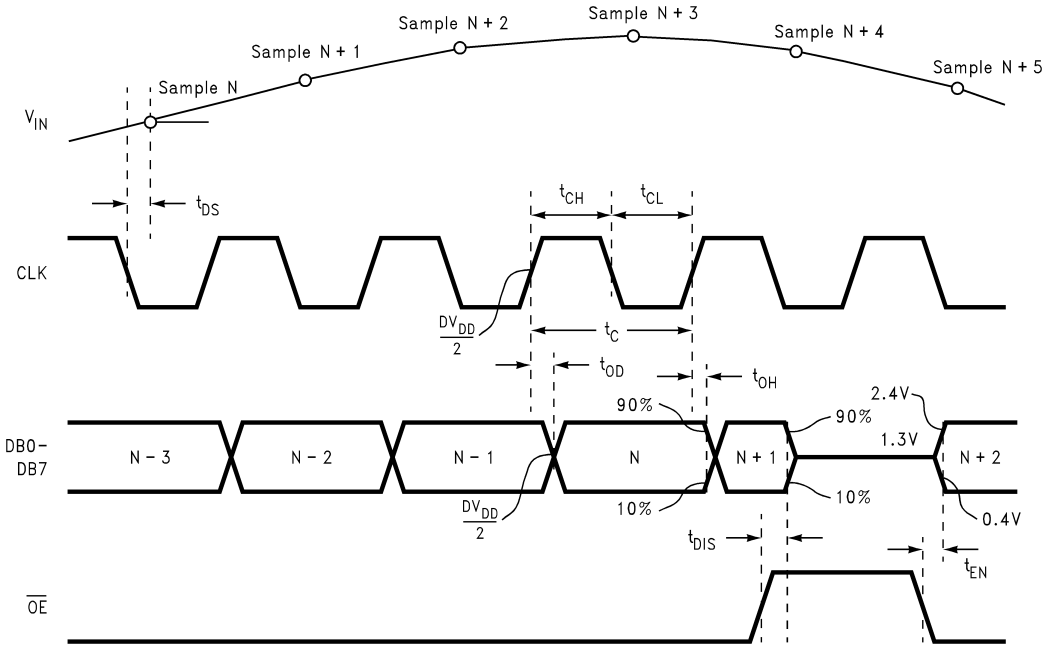


Figure 17. ADC1175 Timing Diagram

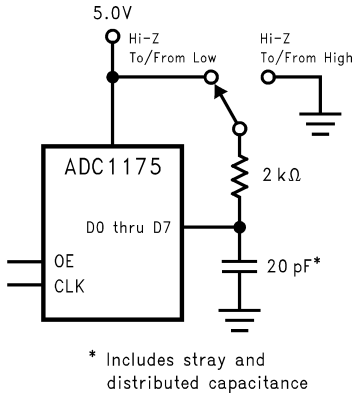


Figure 18. t_{EN} , t_{DIS} Test Circuit

FUNCTIONAL DESCRIPTION

The ADC1175 uses a new, unique architecture to achieve 7.2 effective bits at and maintains superior dynamic performance up to ½ the clock frequency.

The analog signal at V_{IN} that is within the voltage range set by V_{RT} and V_{RB} are digitized to eight bits at up to 30 MSPS. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones. V_{RT} has a range of 1.0 Volt to the analog supply voltage, AV_{DD}, while V_{RB} has a range of 0 to 4.0 Volts. V_{RT} should always be between 1.0 Volt and 2.8 Volts more positive than V_{RB}.

If V_{RT} and V_{RTS} are connected together and V_{RB} and V_{RBS} are connected together, the nominal values of V_{RT} and V_{RB} are 2.6V and 0.6V, respectively. If V_{RT} and V_{RTS} are connected together and V_{RB} is grounded, the nominal value of V_{RT} is 2.3V.

Data is acquired at the falling edge of the clock and the digital equivalent of the data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC1175 will convert as long as the clock signal is present at pin 12. The Output Enable pin $\overline{OE}$, when low, enables the output pins. The digital outputs are in the high impedance state when the $\overline{OE}$ pin is high.

APPLICATIONS INFORMATION

THE ANALOG INPUT

The analog input of the ADC1175 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 4 pF when the clock is low, and 11 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than a fixed capacitance, choose an amplifier that can drive this type of load. The LMH6702, LMH6609, LM6152, LM6154, LM6181 and LM6182 have been found to be excellent devices for driving the ADC1175. Do not drive the input beyond the supply rails. Figure 19 shows an example of an input circuit using the LMH6702.

Driving the analog input with input signals up to 2.8 V_{P-P} will result in normal behavior where signals above V_{RT} will result in a code of FFh and input voltages below V_{RB} will result in an output code of zero. Input signals above 2.8 V_{P-P} may result in odd behavior where the output code is not FFh when the input exceeds V_{RT}.

REFERENCE INPUTS

The reference inputs V_{RT} (Reference Top) and V_{RB} (Reference Bottom) are the top and bottom of the reference ladder. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in Operating Ratings (1.0V to AV_{DD} for V_{RT} and 0V to (AV_{DD} - 1.0V) for V_{RB}). Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin.

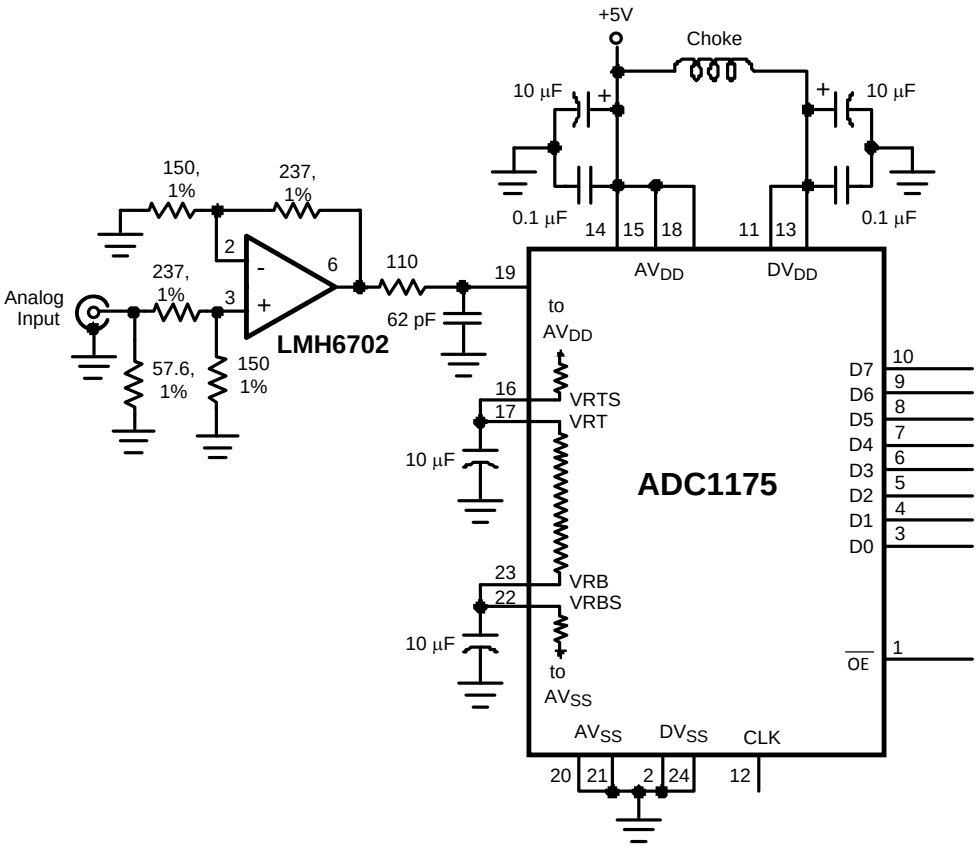
The reference ladder can be self-biased by connecting V_{RT} to V_{RTS} and connecting V_{RB} to V_{RBS} to provide top and bottom reference voltages of approximately 2.6V and 0.6V, respectively, with V_{CC} = 5.0V. This connection is shown in Figure 19. If V_{RT} and V_{RTS} are tied together, but V_{RB} is tied to analog ground, a top reference voltage of approximately 2.3V is generated. The top and bottom of the ladder should be bypassed with 10µF tantalum capacitors located close to the reference pins.

The reference self-bias circuit of Figure 19 is very simple and performance is adequate for many applications. Superior performance can generally be achieved by driving the reference pins with a low impedance source.

By forcing a little current into or out of the top and bottom of the ladder, as shown in Figure 20, the top and bottom reference voltages can be trimmed and performance improved over the self-bias method of Figure 19. The resistive divider at the amplifier inputs can be replaced with potentiometers. The LMC662 amplifier shown was chosen for its low offset voltage and low cost. Note that a negative power supply is needed for these amplifiers if their outputs are required to go slightly negative to force the required reference voltages.

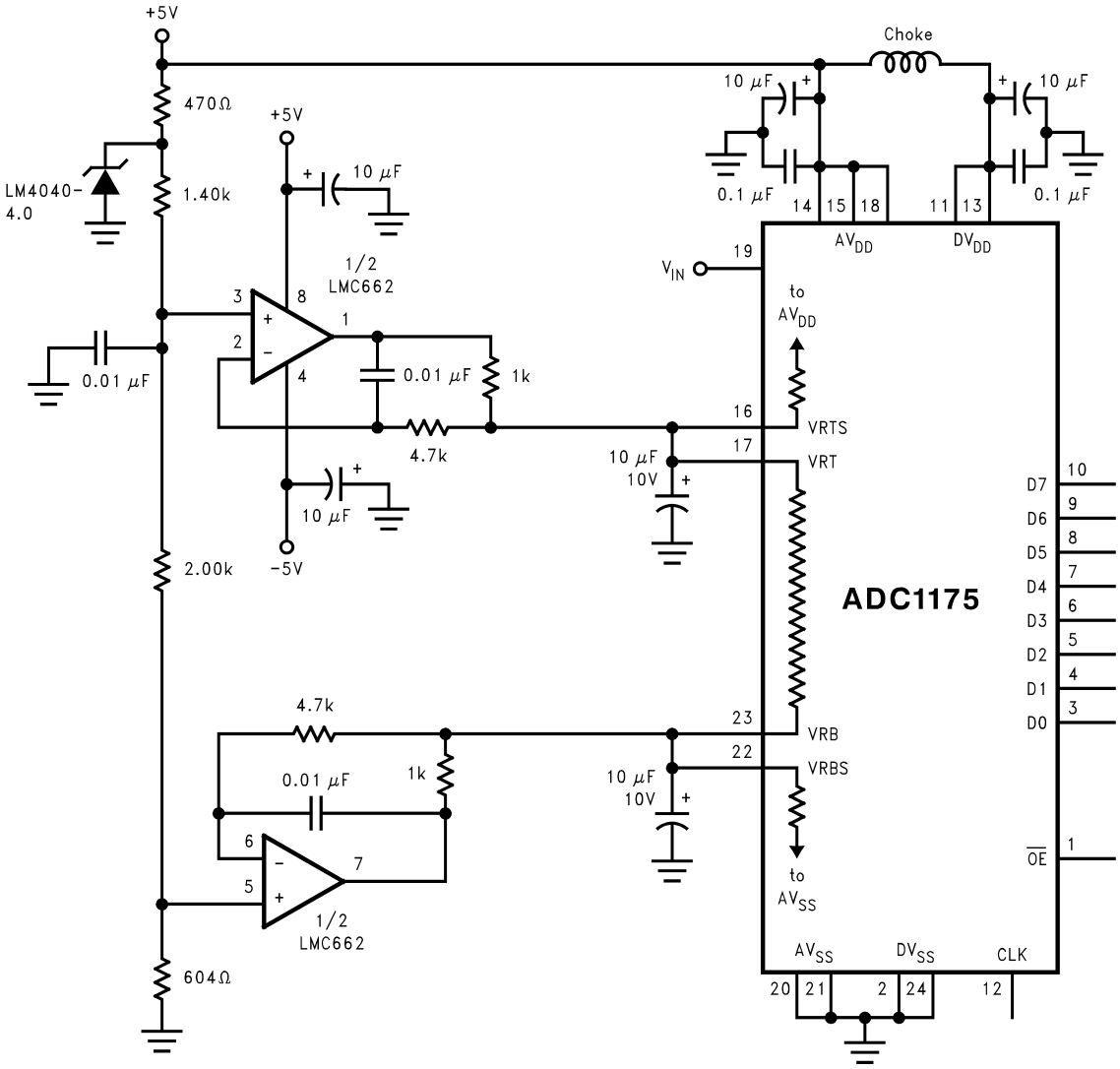
If reference voltages are desired that are more than a few tens of millivolts from the self-bias values, the circuit of Figure 21 will allow forcing the reference voltages to whatever levels are desired. This circuit provides the best performance because of the low source impedance of the transistors. Note that the V_{RTS} and V_{RBS} pins are left floating.

V_{RT} can be anywhere between V_{RB} + 1.0V and the analog supply voltage, and V_{RB} can be anywhere between ground and 1.0V below V_{RT}. To minimize noise effects and ensure accurate conversions, the total reference voltage range (V_{RT} - V_{RB}) should be a minimum of 1.0V and a maximum of about 2.8V. If V_{RB} is not required to be below about +700mV, the -5V points in Figure 21 can be returned to ground and the negative supply eliminated.



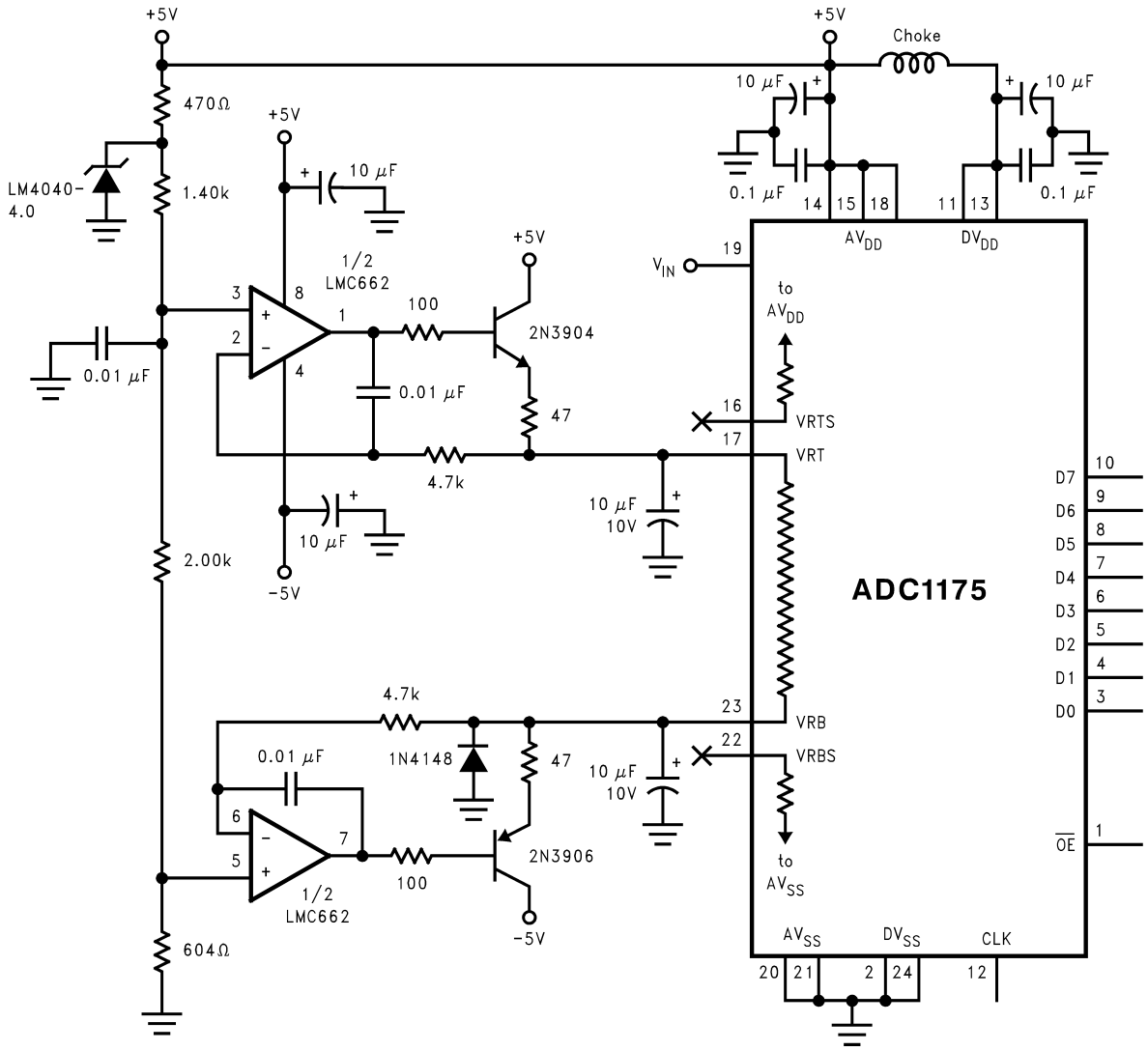
Because of resistor tolerances, the reference voltages can vary by as much as 6%. Choose an amplifier that can drive a dynamic capacitance (see text).

Figure 19. Simple, Low Component Count, Self-Bias Reference Application



Self-bias is still used, but the reference voltages are trimmed by providing a small trim current with the operational amplifiers.

Figure 20. Better Defining the ADC Reference Voltage



Driving the reference to force desired values requires driving with a low impedance source, provided by the transistors. Pins 16 and 22 are not connected.

Figure 21.

POWER SUPPLY CONSIDERATIONS

Many A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 centimeters) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed as close as possible to the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source should be used for the analog and digital supplies of the ADC1175, these supply pins should be well isolated from each other to prevent any digital noise from being coupled to the analog power pins. A wideband choke, such as the JW Miller FB20010-3B, is recommended between the analog and digital supply lines, with a ceramic capacitor close to the analog supply pin. Avoid inductive components in the analog supply line.

The converter digital supply should **not** be the supply that is used for other digital circuitry on the board. It should be the same supply used for the A/D analog supply.

As is the case with all high speed converters, the ADC1175 should be assumed to have little a.c. power supply rejection, especially when self-biasing is used by connecting V_{RT} and V_{RTS} together.

No pin should ever have a voltage on it that is in excess of the supply voltages or below ground, not even on a transient basis. This can be a problem upon application of power to a circuit. Be sure that the supplies to circuits driving the CLK, $\overline{OE}$, analog input and reference pins do not come up any faster than does the voltage at the ADC1175 power pins.

Pins 11 and 13 are both labeled DV_{DD}. Pin 11 is the supply point for the digital core of the ADC, where pin 13 is used only to provide power to the ADC output drivers. As such, pin 11 may be connected to a voltage source that is less than the +5V used for AV_{DD} and DV_{DD} to ease interfacing to low voltage devices. Pin 11 should never exceed the pin 13 potential by more than 0.5V.

THE ADC1175 CLOCK

Although the ADC1175 is tested and its performance is ensured with a 20MHz clock, it typically will function with clock frequencies from 1MHz to 30MHz.

If continuous conversions are not required, power consumption can be reduced somewhat by stopping the clock at a logic low when the ADC1175 is not being used. This reduces the current drain in the ADC1175's digital circuitry from a typical value of 2.5mA to about 100µA.

Note that powering up the ADC1175 without the clock running may not save power, as it will result in an increased current flow (by as much as 170%) in the reference ladder. In some cases, this may increase the ladder current above the specified limit. Toggling the clock twice at 1MHz or higher and returning it to the low state will eliminate the excess ladder current.

An alternative power-saving technique is to power up the ADC1175 with the clock active, then halt the clock in the low state after two or more clock cycles. Stopping the clock in the high state is not recommended as a power-saving technique.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC1175 may be used, but best EMI practices require a single ground plane. However, it is important to keep analog signal lines away from digital signal lines and away from power supply currents. This latter requirement requires the careful separation and placement of power planes. The use of power traces rather than one or more power planes is not recommended as higher frequencies are not well filtered with lumped capacitances. To filter higher frequency noise components it is necessary to have sufficient capacitance between the power and ground planes.

If separate analog and digital ground planes are used, the analog and digital grounds may be in the same layer, but should be separated from each other. If separate analog and digital ground layers are used, they should *never overlap* each other.

Capacitive coupling between a typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuity well separated from the digital circuitry.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families. In general, slower logic families will produce less high frequency noise than do high speed logic families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by using a single, solid ground plane, splitting the power plane into analog and digital areas and having power and ground planes in adjacent board layers. There should be no traces within either the power or the ground layers of the board. The analog and digital power planes should reside in the same board layer so that they can not overlap each other. The analog and digital power planes define the analog and digital areas of the board.

Generally, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog and digital. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies and at high resolution is obtained with a straight signal path.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, not even with just a small part of their bodies being beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground return.

DYNAMIC PERFORMANCE

The ADC1175 is a.c. tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 22.

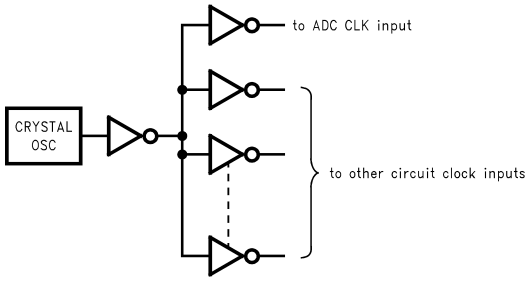


Figure 22. Isolating the ADC clock from Digital Circuitry.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal.

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 50mV below the ground pins or 50mV above the supply pins. Exceeding these limits on even a transient basis can cause faulty or erratic operation. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground due to improper line termination. A resistor of 50Ω to 100Ω in series with the offending digital input, located close to the signal source, will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC1175. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from DV_{DD} and DGND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with an 74AC541, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding 47Ω to 100Ω series resistors at each digital output, reducing the energy coupled back into the converter output pins.

Using an inadequate amplifier to drive the analog input. As explained in THE ANALOG INPUT, the capacitance seen at the input alternates between 4 pF and 11 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device. The LMH6702, LMH6609, LM6152, LM6154, LM6181 and LM6182 have been found to be excellent devices for driving the ADC1175 analog input.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in REFERENCE INPUTS, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. Simple gates with RC timing is generally inadequate as a clock source.

Input test signal contains harmonic distortion that interferes with the measurement of dynamic signal to noise ratio. Harmonic and other interfering signals can be removed by inserting a filter at the signal input. Suitable filters are shown in Figure 23 and Figure 24. The circuit of Figure 23 has cutoff of about 5.5 MHz and is suitable for input frequencies of 1 MHz to 5 MHz. The circuit of Figure 24 has a cutoff of about 11 MHz and is suitable for input frequencies of 5 MHz to 10 MHz. These filters should be driven by a generator of 75 Ohm source impedance and terminated with a 75 ohm resistor.

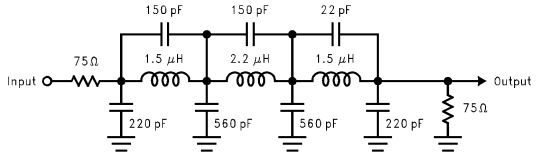
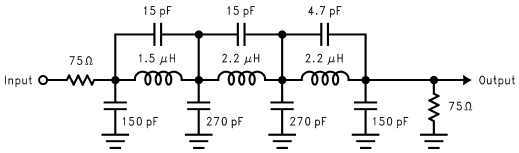


Figure 23. 5.5 MHz Low Pass Filter to Eliminate Harmonics at the Signal Input



Use at input frequencies of 5 MHz to 10 MHz.

Figure 24. 11 MHz Low Pass Filter to Eliminate Harmonics at the Signal Input

Not considering the effect on a driven CMOS digital circuit(s) when the ADC1175 is in the power down mode. Because the ADC1175 output goes into a high impedance state when in the power down mode, any CMOS device connected to these outputs will have their inputs floating when the ADC is in power down. Should the inputs of the circuit being driven by the ADC digital outputs float to a level near 2.5V, a CMOS device could exhibit relative large supply currents as the input stage toggles rapidly. The solution is to use pull-down resistors at the ADC outputs. The value of these resistors is not critical, as long as they do not cause excessive currents in the outputs of the ADC1175. Low pull-down resistor values could result in degraded SNR and SINAD performance of the ADC1175. Values between 5 kΩ and 100 kΩ should work well.

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC1175CIMTC/NOPB	ACTIVE	TSSOP	PW	24	61	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 70	ADC1175 CIMTC	Samples
ADC1175CIMTCX/NOPB	ACTIVE	TSSOP	PW	24	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 70	ADC1175 CIMTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

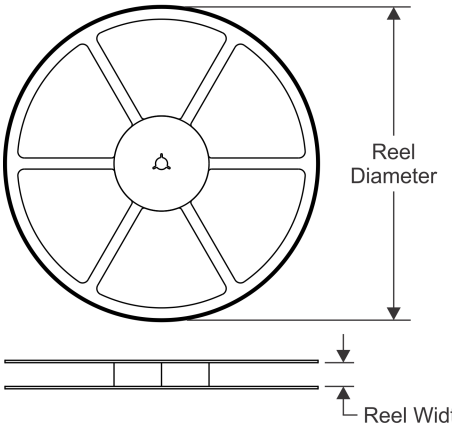
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

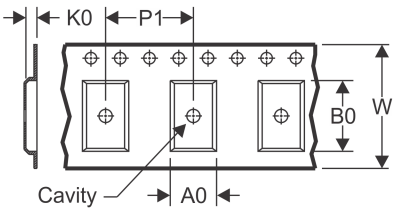
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

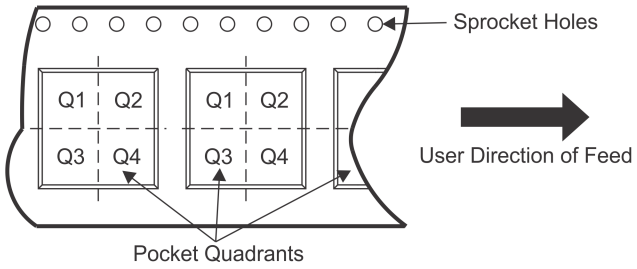


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

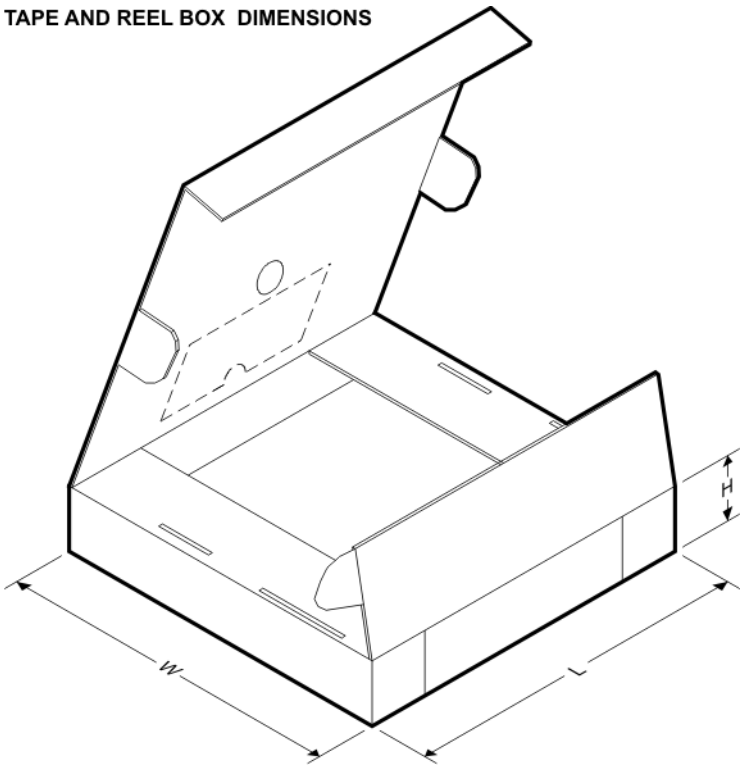
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC1175CIMTCX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

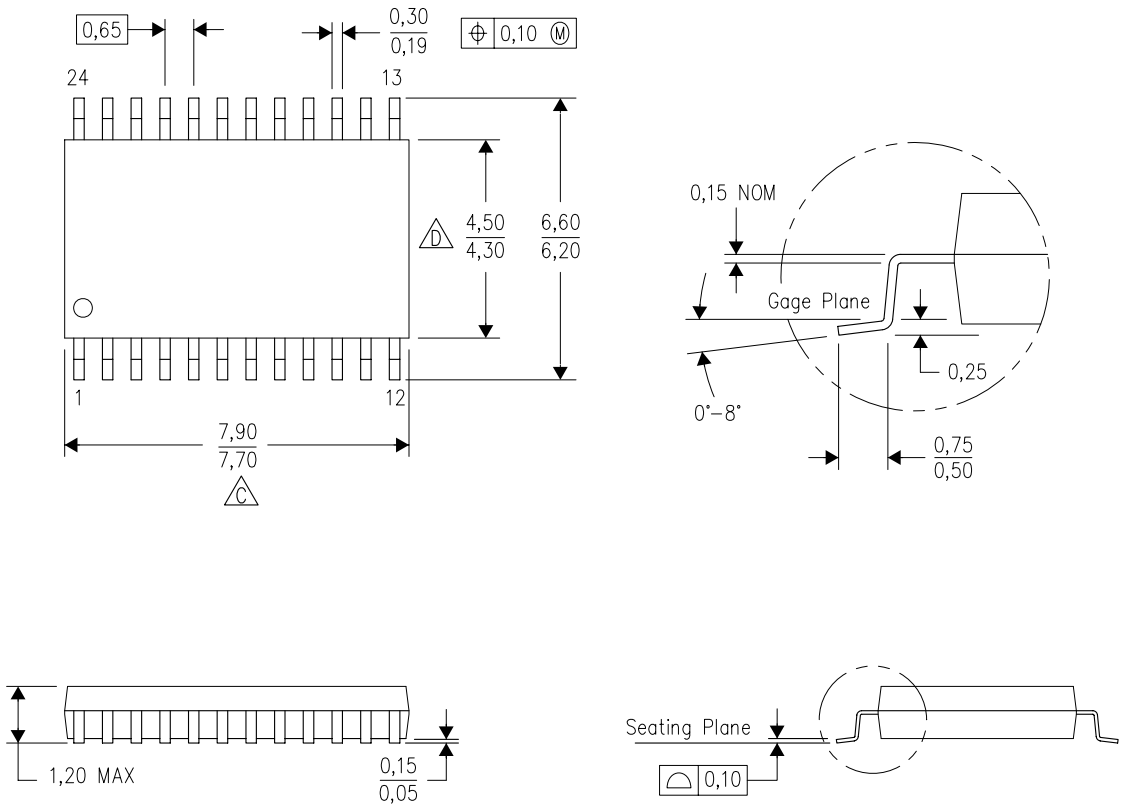
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC1175CIMTCX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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