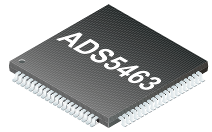


12-BIT, 500-MSPS ANALOG-TO-DIGITAL CONVERTER

Check for Samples : ADS5463-EP

FEATURES

- **500-MSPS Sample Rate**
- **12-Bit Resolution, 10.5-Bits Effective Number of Bits (ENOB)**
- **2-GHz Input Bandwidth**
- **SFDR = 75 dBc at 450 MHz and 500 MSPS**
- **SNR = 64.6 dBFS at 450 MHz and 500 MSPS**
- **2.2-Vpp Differential Input Voltage**
- **LVDS-Compatible Outputs**
- **Total Power Dissipation: 2.2 W**
- **Offset Binary Output Format**
- **Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock**
- **On-Chip Analog Buffer, Track and Hold, and Reference Circuit**
- **80-Pin TQFP PowerPAD™ Package (14 mm × 14 mm)**
- **Pin Similar to ADS5440/ADS5444**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

APPLICATIONS

- **Test and Measurement Instrumentation**
- **Software-Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Communication Instrumentation**
- **Radar**

(1) Additional temperature ranges available - contact factory

DESCRIPTION/ORDERING INFORMATION

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs. The ADS5463 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source while providing a high impedance input. An internal reference generator also is provided to simplify the system design.

Designed to optimize conversion of wide-bandwidth signals up to 500-MHz of input frequency at 500 MSPS, the ADS5463 has outstanding low noise and linearity over a large input frequency range. Input signals above 500 MHz also can be converted due to the large input bandwidth of the device.

The ADS5463 is available in an 80-pin TQFP PowerPAD™ package. The ADS5463 is built on state-of-the-art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full extended temperature range (–55°C to 125°C).

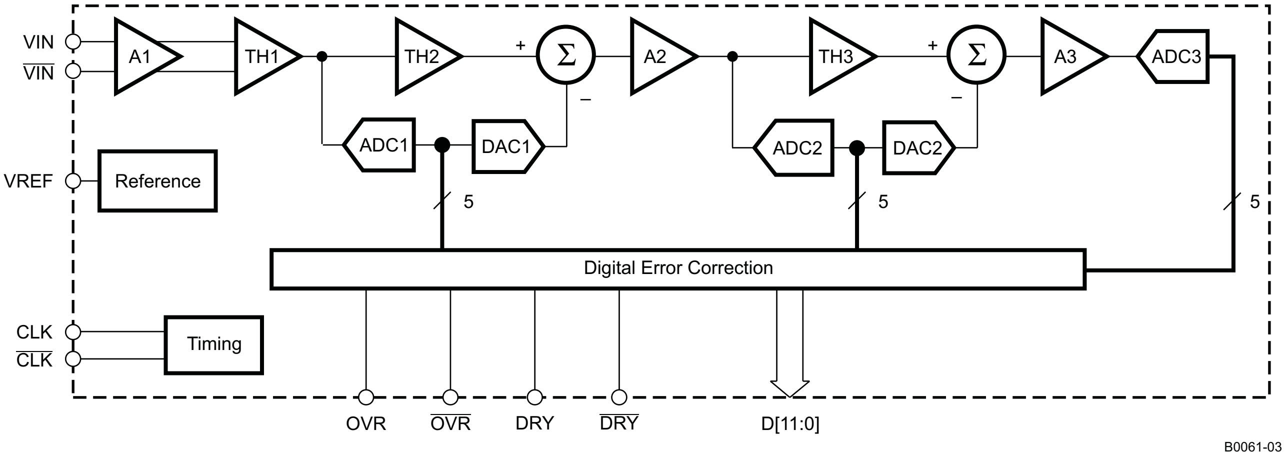


Figure 1. Analog-to-Digital Converter Functional Block Diagram

Table 1. PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR (2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5463-EP	HTQFP-80(3) PowerPAD	PFP	–55°C to 125°C	ADS5463MEP	ADS5463MPFPEP	Tray, 96

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Thermal pad size: 9.5 mm × 9.5 mm (minimum), 10 mm × 10 mm (maximum).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
Supply voltage	AVDD5 to GND		6	V
	AVDD3 to GND		5	
	DVDD3 to GND		5	
AIN, $\overline{AIN}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.4 to 4.4	
		DC signal, T_J = 125°C	1.0 to 3.8	
AIN to $\overline{AIN}$ (2)	Voltage difference between these pins	AC signal	–5.2 to 5.2	V
		DC signal, T_J = 105°C	–4 to 4	
		DC signal, T_J = 125°C	–2.8 to 2.8	
CLK, $\overline{CLK}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.1 to 4.7	
		DC signal, T_J = 125°C	1.1 to 3.7	
CLK to $\overline{CLK}$ (2)	Voltage difference between these pins	AC signal	–3.3 to 3.3	V
		DC signal, T_J = 105°C	–3.3 to 3.3	
		DC signal, T_J = 125°C	–2.6 to 2.6	
Data output to GND(2)	LVDS digital outputs		–0.3 to (DVDD3 + 0.3)	V
Characterized case operating temperature range			–55 to 125	°C
Maximum junction temperature			150	°C
Storage temperature range			–65 to 150	°C
ESD Human Body Model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Valid when supplies are within recommended operating range.

THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
(2)$R_{\theta JA}$	Soldered thermal pad, no airflow	23.7	°C/W
	Soldered thermal pad, 150 LFM airflow	17.8	
	Soldered thermal pad, 250 LFM airflow	16.4	
(3)$R_{\theta JP}$	Bottom of package (thermal pad)	2.99	°C/W

(1) Using 36 thermal vias (6 × 6 array). See *Application Information* section.
(2) $R_{\theta JA}$ is the thermal resistance from junction to ambient.
(3) $R_{\theta JP}$ is the thermal resistance from junction to the thermal pad.

Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Figure 2 for additional information on thermal derating. Electromigration failure mode applies to powered part. Kirkendall voiding failure mode is a function of temperature only.

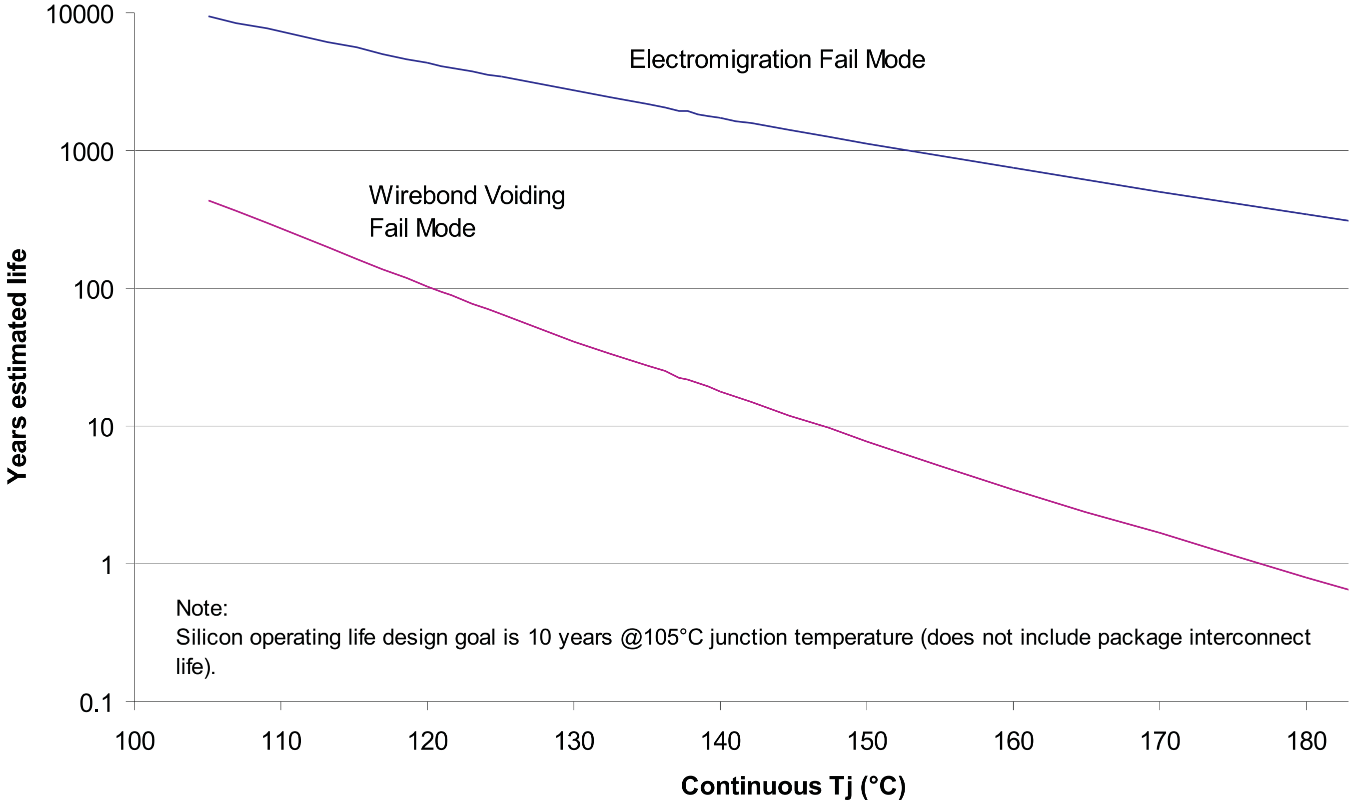


Figure 2. ADS5463-EP Operating Life Derating Chart

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{pp}
V_{CM}	Input common mode		2.4		V
DIGITAL OUTPUT (DRY, DATA, OVR)					
	Maximum differential output load		10		pF
CLOCK INPUT (CLK)					
	CLK input sample rate (sine wave)	20		500	MSPS
	Clock amplitude, differential sine wave		3		V_{pp}
	Clock duty cycle		50%		
T_A	Open free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –55°C to T_{MAX} = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		Bits
ANALOG INPUTS						
	Differential input range			2.2		Vpp
V_{CM}	Input common mode			2.4		V
	Input resistance (dc)	Each input to ground		500		Ω
	Input capacitance	Each input to ground		2.5		pF
	Analog input bandwidth (–3 dB)	Dependent on source impedance		2		GHz
CMRR	Common Mode Rejection Ratio	Common Mode Signal = 10MHz		80		dB
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
DYNAMIC ACCURACY						
	No missing codes			Assured		
DNL	Differential linearity error	f_{IN} = 10 MHz	–0.95	±0.25	0.95	LSB
INL	Integral linearity error	f_{IN} = 10 MHz	–2.5	+0.8/–0.3	2.5	LSB
	Offset error		–11		11	mV
	Offset temperature coefficient			0.0005		mV/°C
	Gain error		–5.2		5.2	%FS
	Gain temperature coefficient			–0.02		Δ%/°C
	PSRR	100kHz supply noise (see Figure 34)		85		dB
POWER SUPPLY						
I_{AVDD5}	5-V analog supply current	V_{IN} = full scale, f_{IN} = 10 MHz, f_S = 500 MSPS		300	365	mA
I_{AVDD3}	3.3-V analog supply current			125	145	mA
I_{DVDD3}	3.3-V digital supply current			82	92	mA
	Total Power dissipation			2.18	2.575	W
	Power-up time			200		µs
DYNAMIC AC CHARACTERISTICS						

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –55°C to T_{MAX} = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz			65.3		dBFS
		f_{IN} = 70 MHz			65.4		
		f_{IN} = 100 MHz	25C	63.5	65.3		
			Temp	63	65.3		
		f_{IN} = 230 MHz			65.1		
		f_{IN} = 300 MHz	25C	63.25	65		
			Temp	61.75	65		
		f_{IN} = 450 MHz			64.6		
		f_{IN} = 650 MHz			63.9		
		f_{IN} = 900 MHz			62.6		
		f_{IN} = 1.3 GHz			59.3		
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz			85		dBc
		f_{IN} = 70 MHz			82		
		f_{IN} = 100 MHz	25C	70	82		
			Temp	67	82		
		f_{IN} = 230 MHz			78		
		f_{IN} = 300 MHz	25C	64	77		
			Temp	62	77		
		f_{IN} = 450 MHz			75		
		f_{IN} = 650 MHz			65		
		f_{IN} = 900 MHz			56		
		f_{IN} = 1.3 GHz			45		
HD2	Second harmonic	f_{IN} = 10 MHz			87		dBc
		f_{IN} = 70 MHz			82		
		f_{IN} = 100 MHz		67	80		
		f_{IN} = 230 MHz			81		
		f_{IN} = 300 MHz		62.5	77		
		f_{IN} = 450 MHz			80		
		f_{IN} = 650 MHz			77		
		f_{IN} = 900 MHz			66		
		f_{IN} = 1.3 GHz			50		
HD3	Third harmonic	f_{IN} = 10 MHz			85		dBc
		f_{IN} = 70 MHz			90		
		f_{IN} = 100 MHz		67.5	87		
		f_{IN} = 230 MHz			90		
		f_{IN} = 300 MHz		63	80		
		f_{IN} = 450 MHz			75		
		f_{IN} = 650 MHz			65		
		f_{IN} = 900 MHz			56		
		f_{IN} = 1.3 GHz			45		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –55°C to T_{MAX} = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz		86		dBc
		f_{IN} = 70 MHz		86		
		f_{IN} = 100 MHz		86		
		f_{IN} = 230 MHz		77		
		f_{IN} = 300 MHz		81		
		f_{IN} = 450 MHz		86		
		f_{IN} = 650 MHz		85		
		f_{IN} = 900 MHz		78		
		f_{IN} = 1.3 GHz		67		
THD	Total Harmonic Distortion	f_{IN} = 10 MHz		80		dBc
		f_{IN} = 70 MHz		79		
		f_{IN} = 100 MHz		77		
		f_{IN} = 230 MHz		75		
		f_{IN} = 300 MHz		73		
		f_{IN} = 450 MHz		73		
		f_{IN} = 650 MHz		64		
		f_{IN} = 900 MHz		55		
		f_{IN} = 1.3 GHz		44		
SINAD	Signal-to-noise and distortion	f_{IN} = 10 MHz		65.2		dBc
		f_{IN} = 70 MHz		65.2		
		f_{IN} = 100 MHz	62	65.1		
		f_{IN} = 230 MHz		64.7		
		f_{IN} = 300 MHz	58.75	64.5		
		f_{IN} = 450 MHz		64.1		
		f_{IN} = 650 MHz		61.5		
		f_{IN} = 900 MHz		55.4		
		f_{IN} = 1.3 GHz		45.1		
	Two-Tone SFDR	f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, Each tone at –7 dBFS		90		dBc
		f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, Each tone at –16 dBFS		89		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, Each tone at –7 dBFS		82		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, Each tone at –16 dBFS		89		
ENOB	Effective number of bits	f_{IN} = 100 MHz	9.9	10.5		Bits
		f_{IN} = 300 MHz		10.4		
	RMS idle-channel noise	Inputs tied to common-mode		0.7		LSB
LVDS DIGITAL OUTPUTS						
V_{OD}	Differential output voltage (±)	T_A = 25°C	247	400	454	mV
V_{OC}	Common mode output voltage		1.125		1.375	V

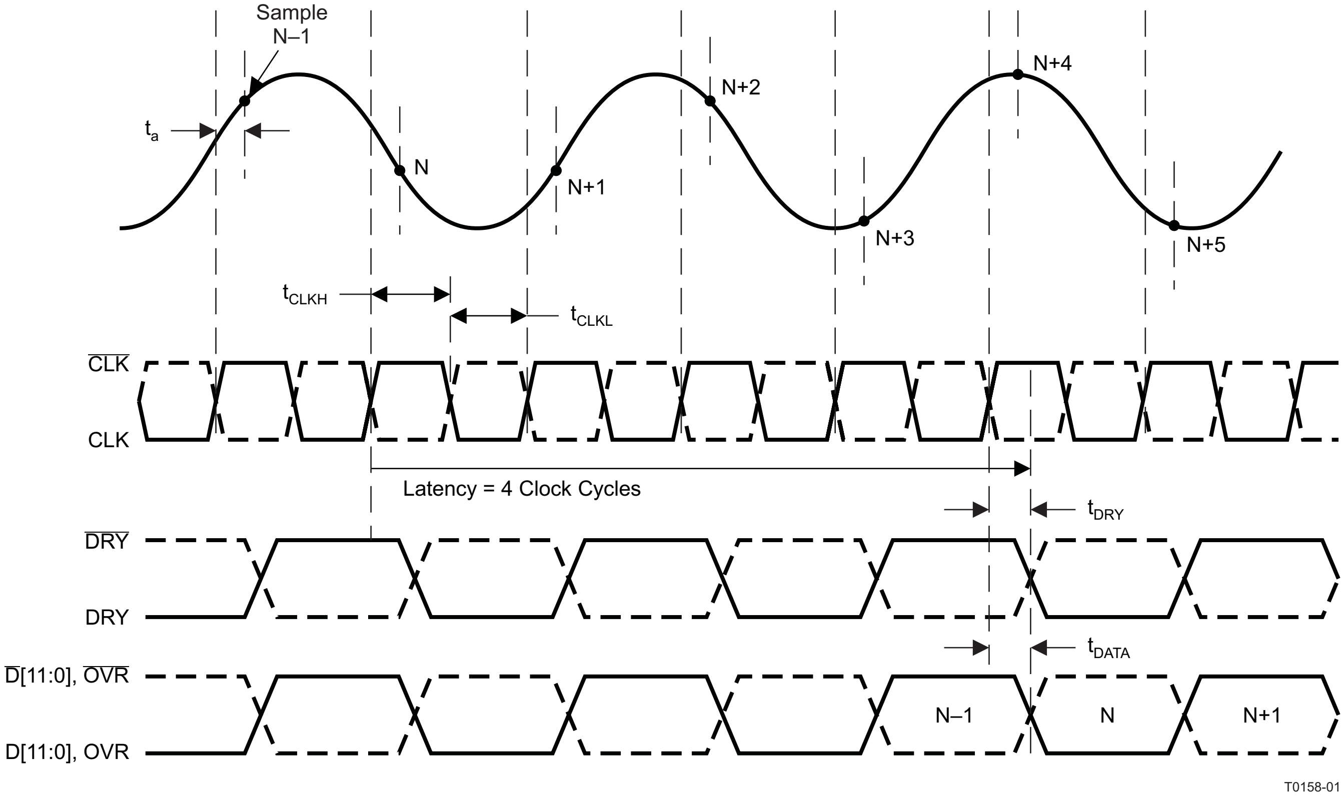


Figure 3. Timing Diagram

TIMING CHARACTERISTICS[1]

Typical values at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay			200		ps
	Aperture jitter, rms			160		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2			ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns
t_{DRY}	CLK to DRY delay[1]	Zero crossing, 7 pF diff loading		1100		ps
t_{DATA}	CLK to DATA/OVR delay [1]	Zero crossing, 7 pF diff loading		1100		ps
t_{SKEW}	DRY to DATA skew	$t_{DATA} – t_{DRY}$, 7 pF diff loading		0		ps
t_{RISE}	DRY/DATA/OVR rise time	7 pF differential loading		500		ps
t_{FALL}	DRY/DATA/OVR fall time	7 pF differential loading		500		ps

(1) DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the data propagation delay.

PFP PACKAGE
(TOP VIEW)

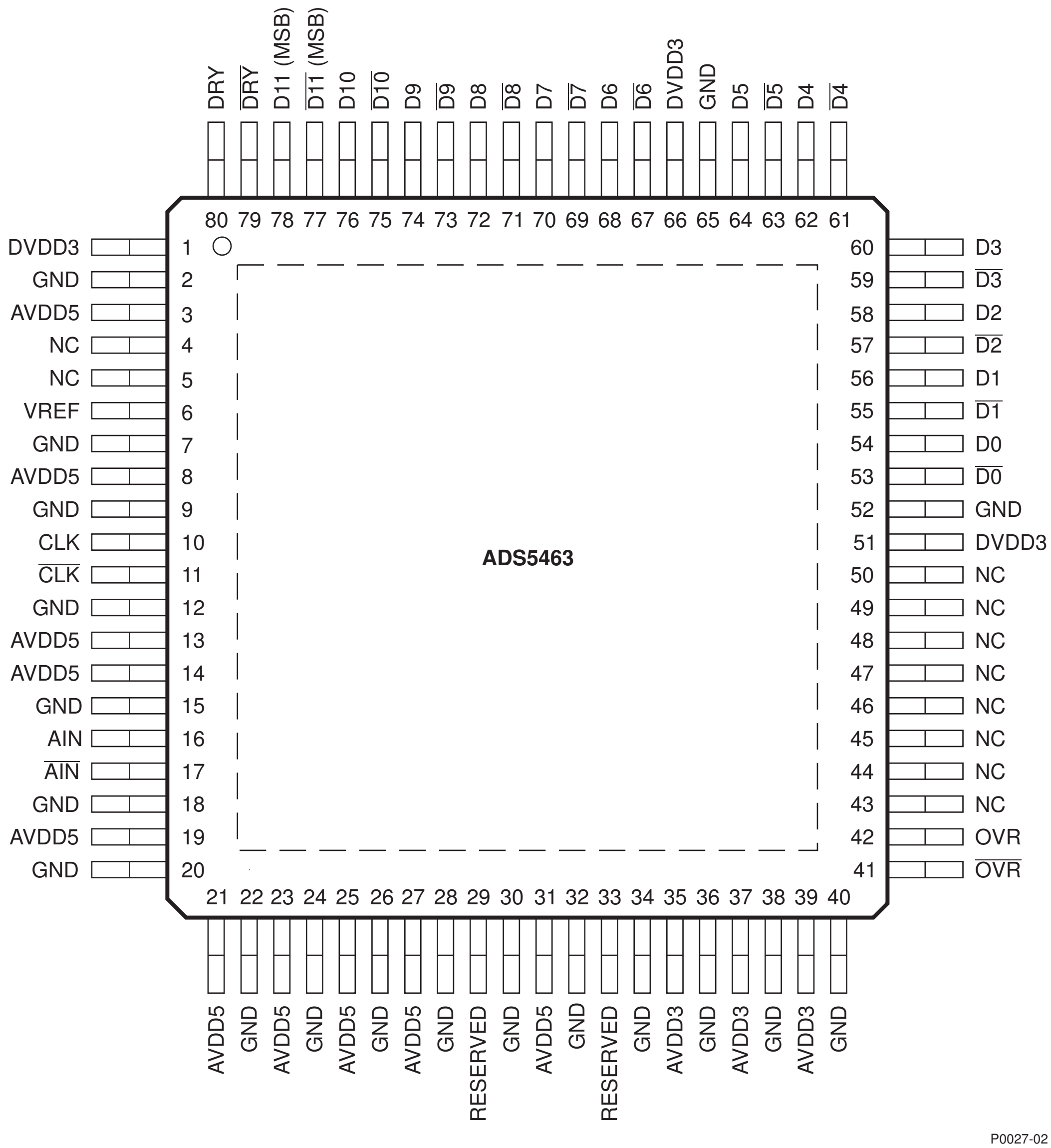


Table 2. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AIN	16	Differential input signal (positive)
$\overline{\text{AIN}}$	17	Differential input signal (negative)
AVDD5	3, 8, 13, 14, 19, 21, 23, 25, 27, 31	Analog power supply (5 V)
AVDD3	35, 37, 39	Analog power supply (3.3 V) (Suggestion for ≤250 MSPS: leave option to connect to 5 V for ADS5440/4 compatibility)
DVDD3	1, 51, 66	Output driver power supply (3.3 V)
GND	2, 7, 9, 12, 15, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 52, 65	Ground
CLK	10	Differential input clock (positive). Conversion is initiated on rising edge.
$\overline{\text{CLK}}$	11	Differential input clock (negative)
D0, $\overline{\text{D0}}$	54, 53	LVDS digital output pair, least-significant bit (LSB)
D1–D10, $\overline{\text{D1}}$–$\overline{\text{D10}}$	55–64, 67–76	LVDS digital output pairs
D11, $\overline{\text{D11}}$	78, 77	LVDS digital output pair, most-significant bit (MSB)
DRY, $\overline{\text{DRY}}$	80, 79	Data ready LVDS output pair
NC	4, 5, 43–50	No connect (4 and 5 should be left floating, 43–50 are possible future bit additions for this pinout and therefore can be connected to a digital bus or left floating)
OVR, $\overline{\text{OVR}}$	42, 41	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
RESERVED	29, 33	Pin 29 is reserved for possible future Vcm output for this pinout; pin 33 is reserved for possible future power-down control pin for this pinout.
VREF	6	Reference voltage

TYPICAL CHARACTERISTICS

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

SPECTRAL PERFORMANCE FFT FOR 30-MHz INPUT SIGNAL

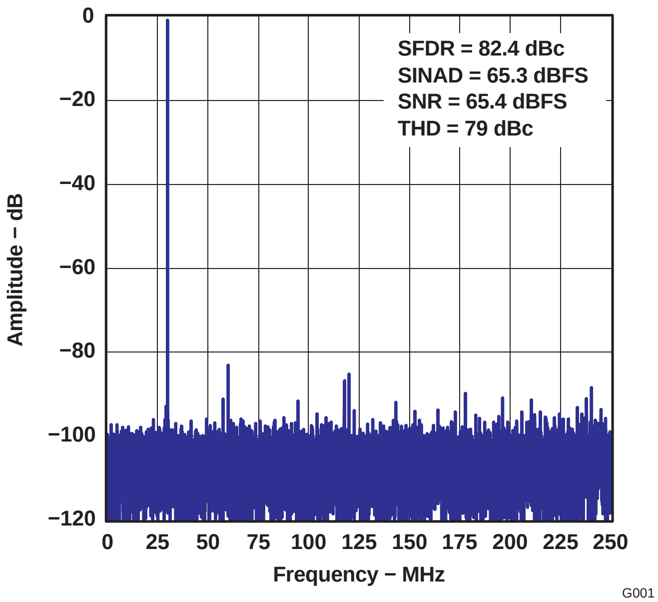


Figure 4.

SPECTRAL PERFORMANCE FFT FOR 100-MHz INPUT SIGNAL

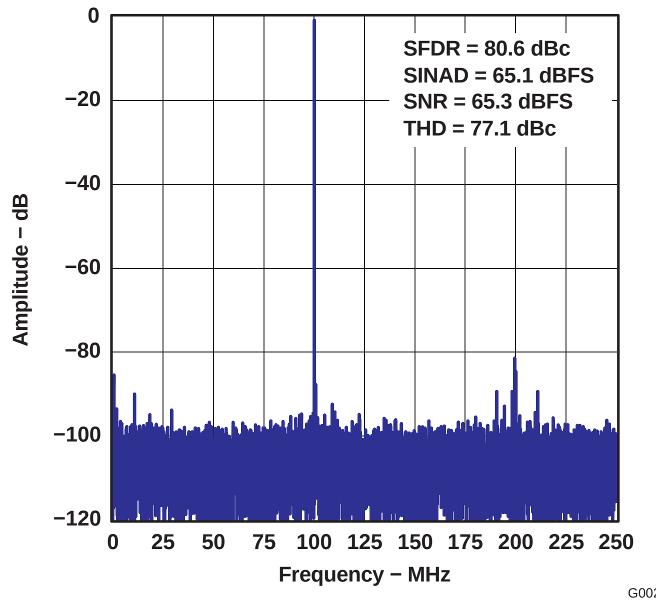


Figure 5.

SPECTRAL PERFORMANCE FFT FOR 230-MHz INPUT SIGNAL

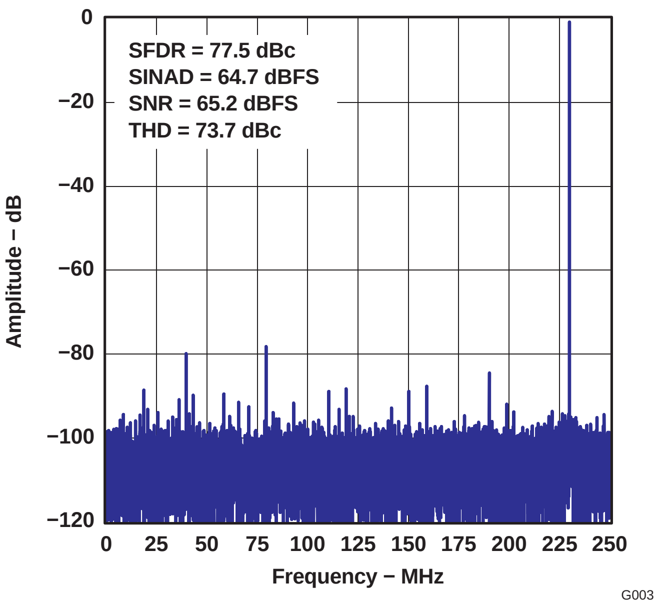


Figure 6.

SPECTRAL PERFORMANCE FFT FOR 300-MHz INPUT SIGNAL

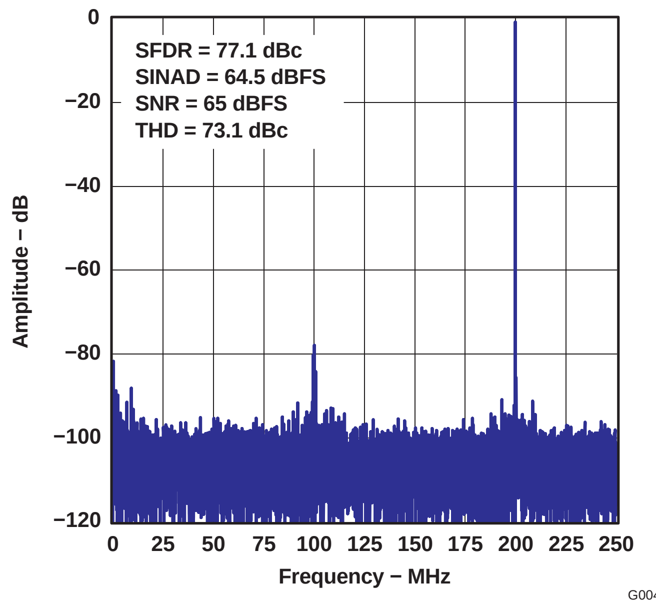


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

SPECTRAL PERFORMANCE
FFT FOR 450-MHz INPUT SIGNAL

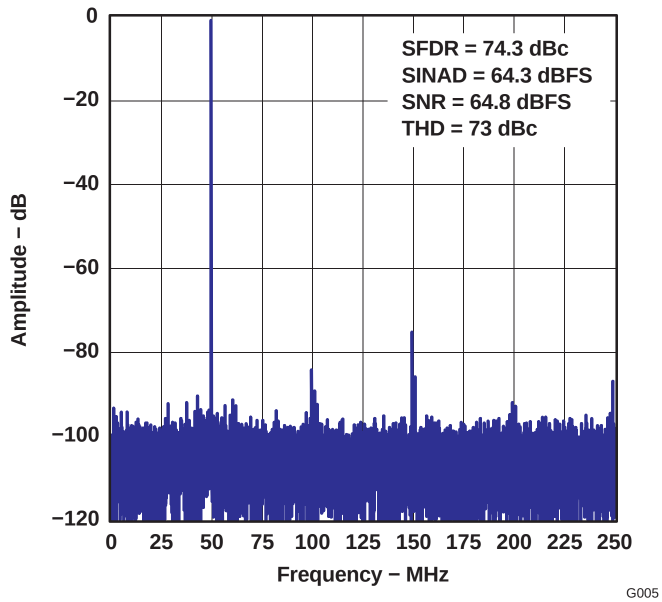


Figure 8.

SPECTRAL PERFORMANCE
FFT FOR 650-MHz INPUT SIGNAL

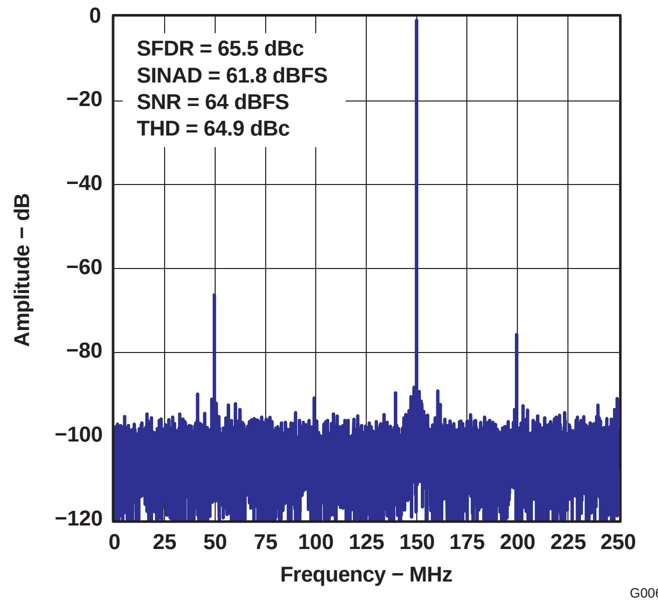


Figure 9.

SPECTRAL PERFORMANCE
FFT FOR 900-MHz INPUT SIGNAL

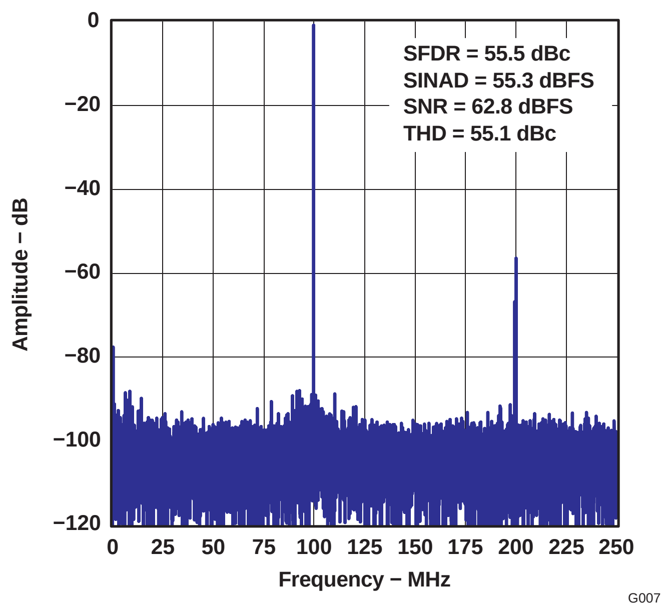


Figure 10.

SPECTRAL PERFORMANCE
FFT FOR 1,300-MHz INPUT SIGNAL

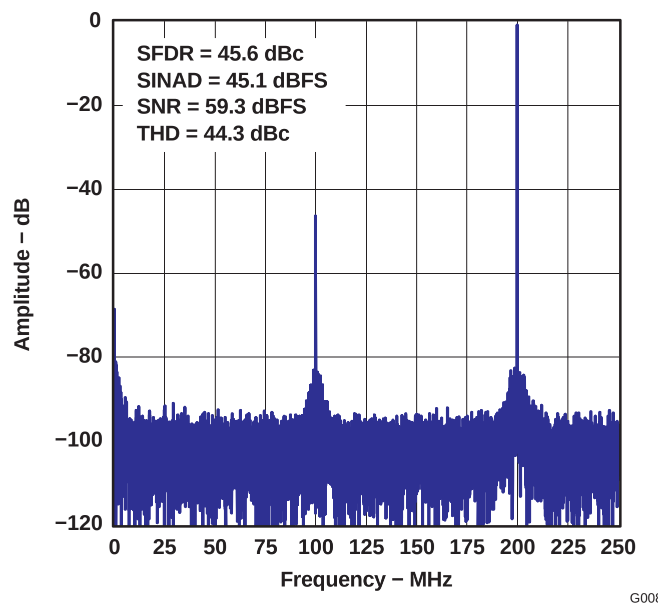


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

TWO-TONE INTERMODULATION DISTORTION (FFT FOR 65.1 MHz AND 70.1 MHz AT –7 dBFS)

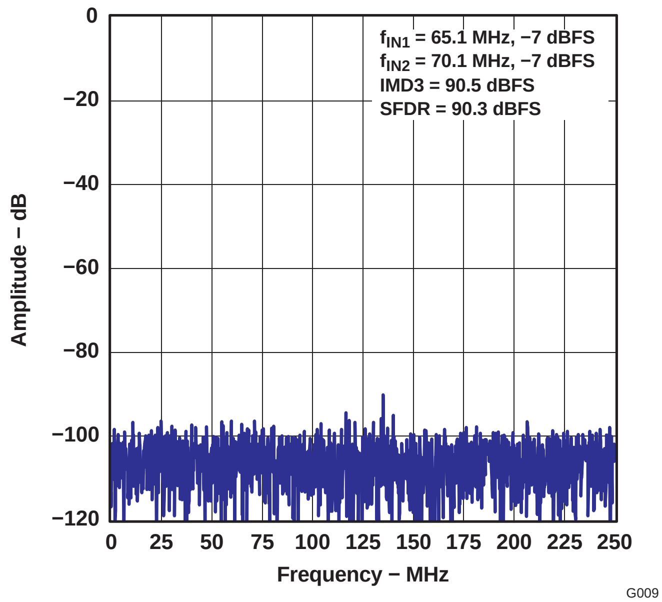


Figure 12.

TWO-TONE INTERMODULATION DISTORTION (FFT FOR 65.1 MHz AND 70.1 MHz AT –16 dBFS)

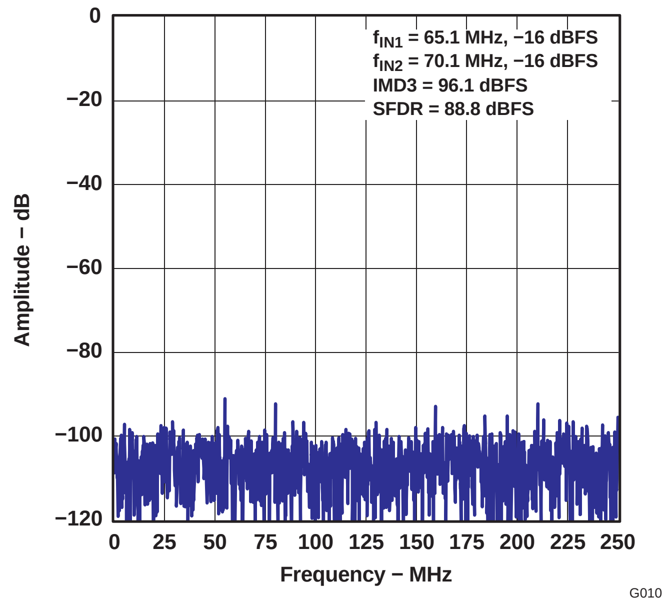


Figure 13.

TWO-TONE INTERMODULATION DISTORTION (FFT FOR 350 MHz AND 355 MHz AT –7 dBFS)

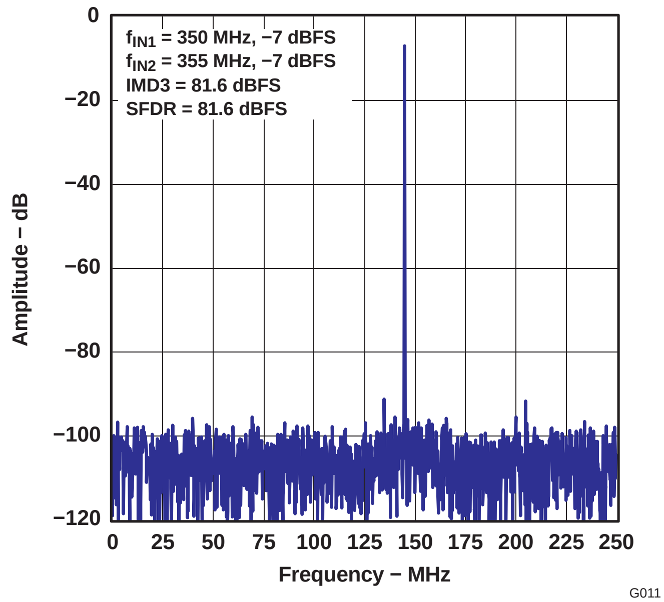


Figure 14.

TWO-TONE INTERMODULATION DISTORTION (FFT FOR 350 MHz AND 355 MHz AT –16 dBFS)

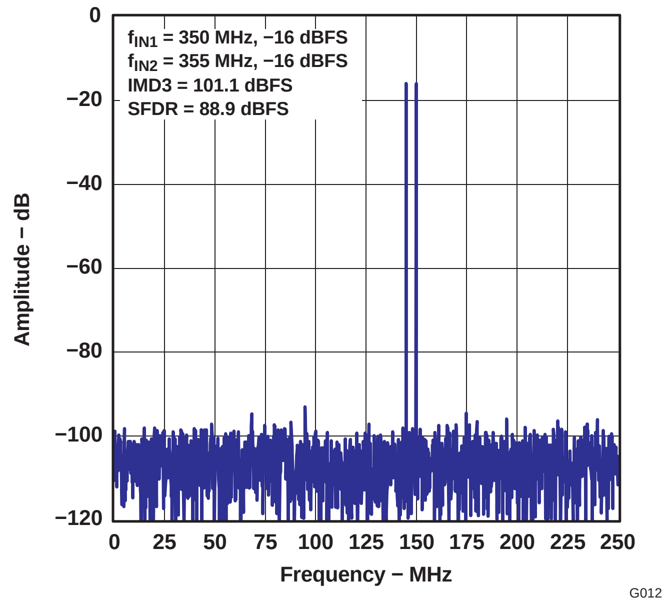


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

FULLSCALE GAIN RESPONSE vs INPUT FREQUENCY

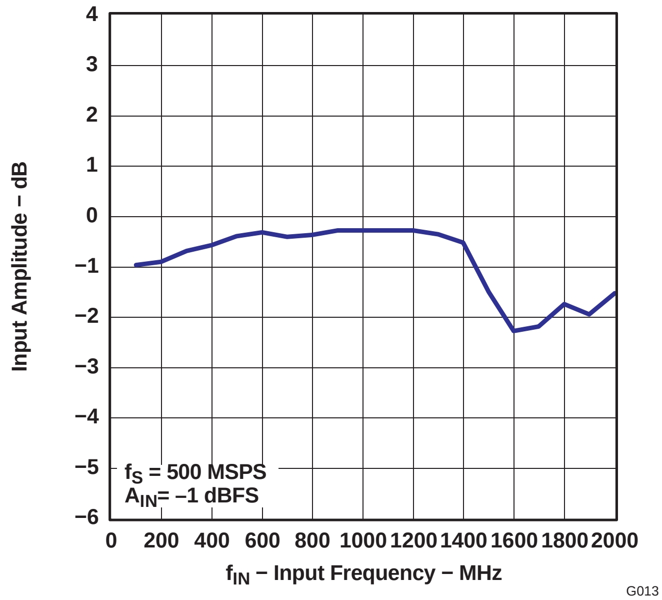


Figure 16.

DIFFERENTIAL NONLINEARITY

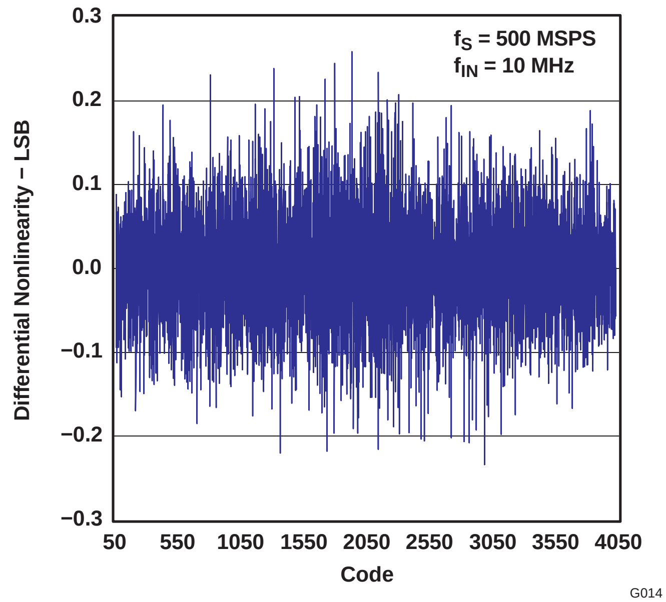


Figure 17.

INTEGRAL NONLINEARITY

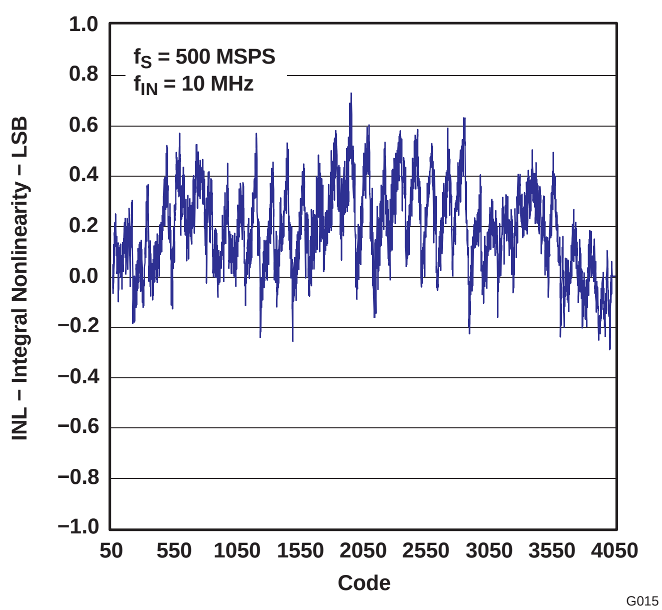


Figure 18.

NOISE HISTOGRAM WITH INPUTS SHORTED

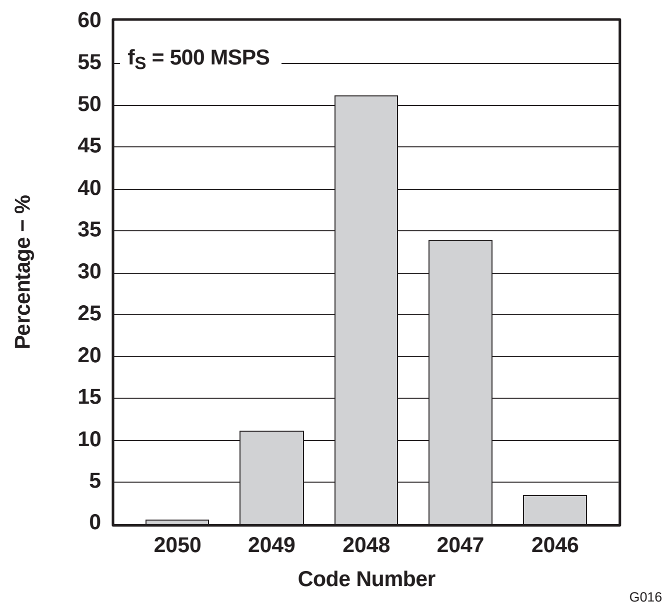


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

AC PERFORMANCE vs INPUT AMPLITUDE (100-MHz INPUT SIGNAL)

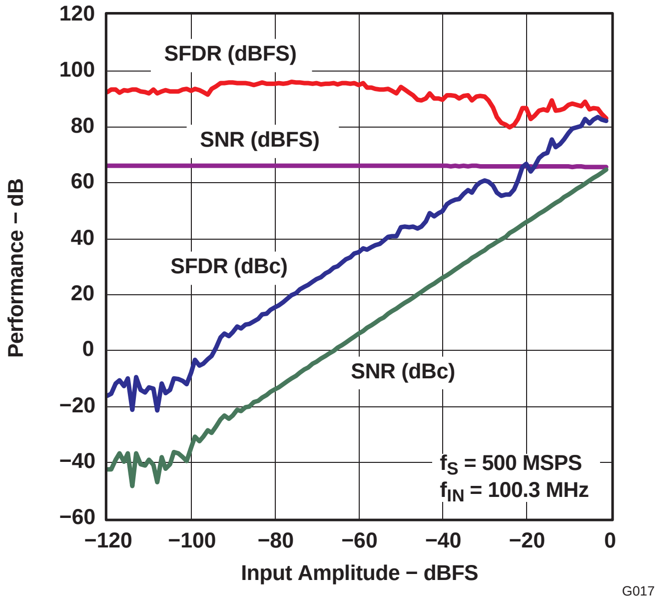


Figure 20.

AC PERFORMANCE vs INPUT AMPLITUDE (300-MHz INPUT SIGNAL)

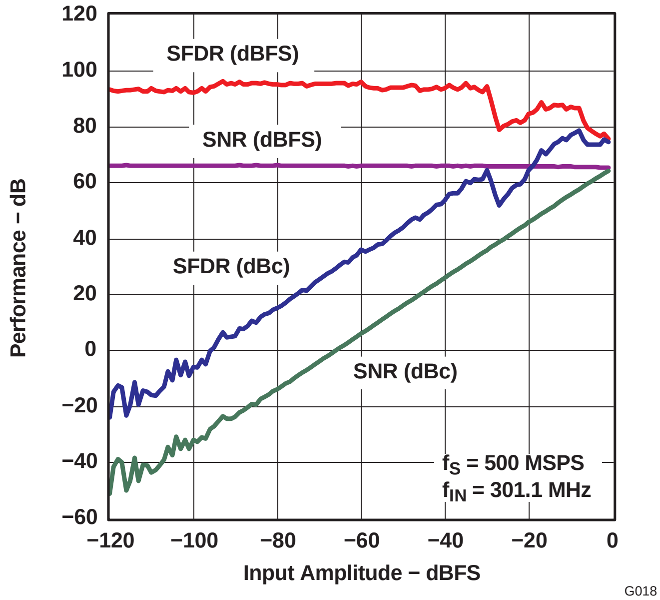


Figure 21.

AC PERFORMANCE vs INPUT AMPLITUDE (350-MHz AND 355-MHz TWO-TONE INPUT SIGNAL)

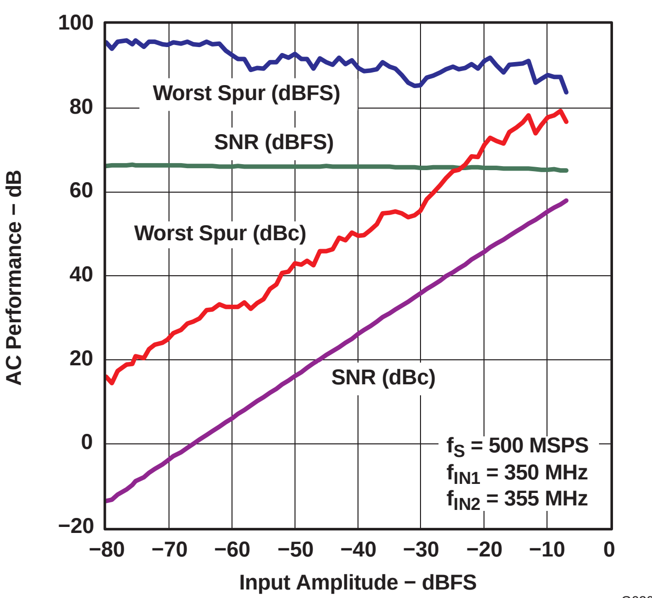


Figure 22.

SFDR vs CLOCK DUTY CYCLE

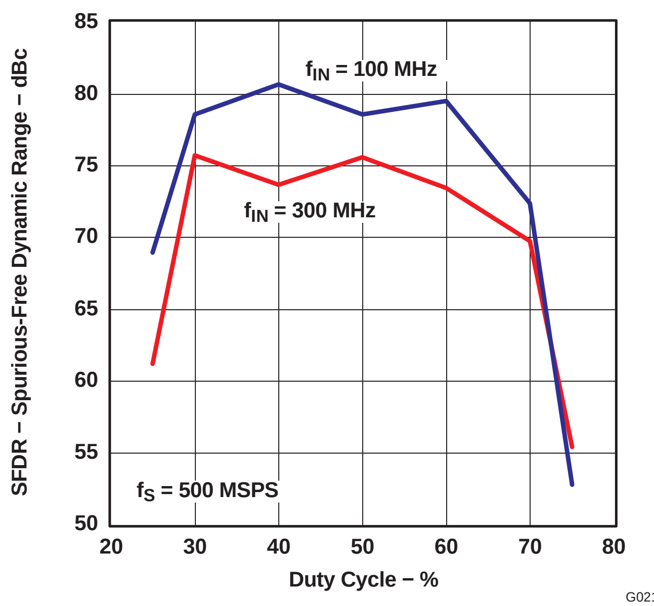


Figure 23.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

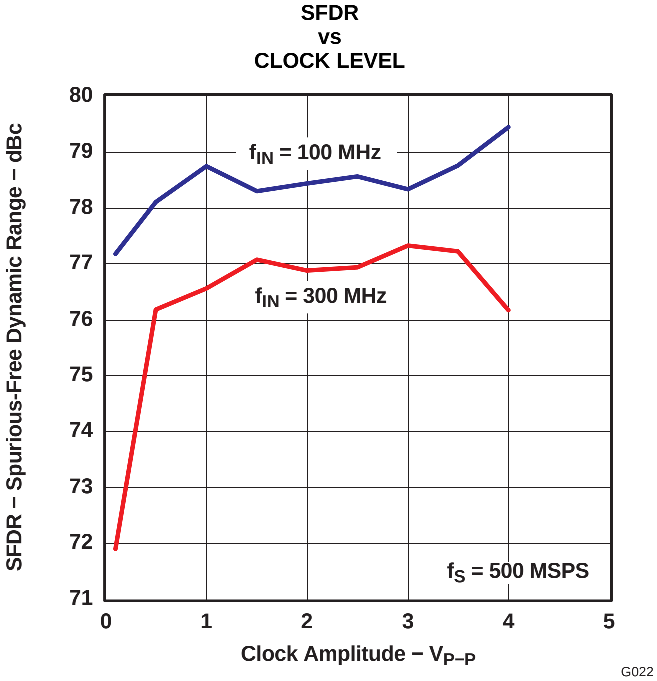


Figure 24.

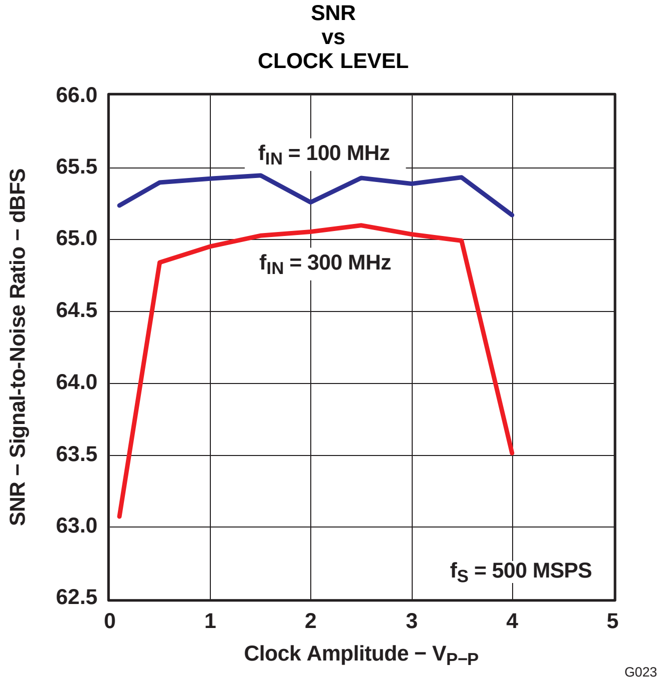


Figure 25.

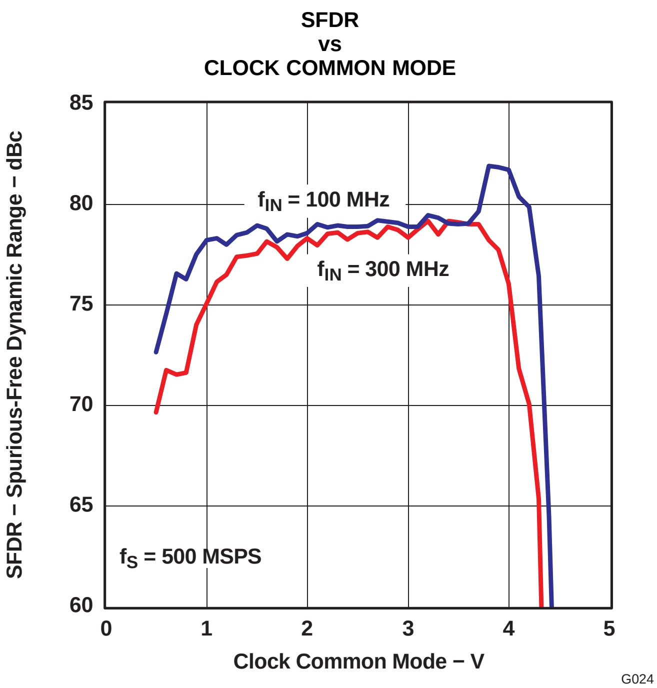


Figure 26.

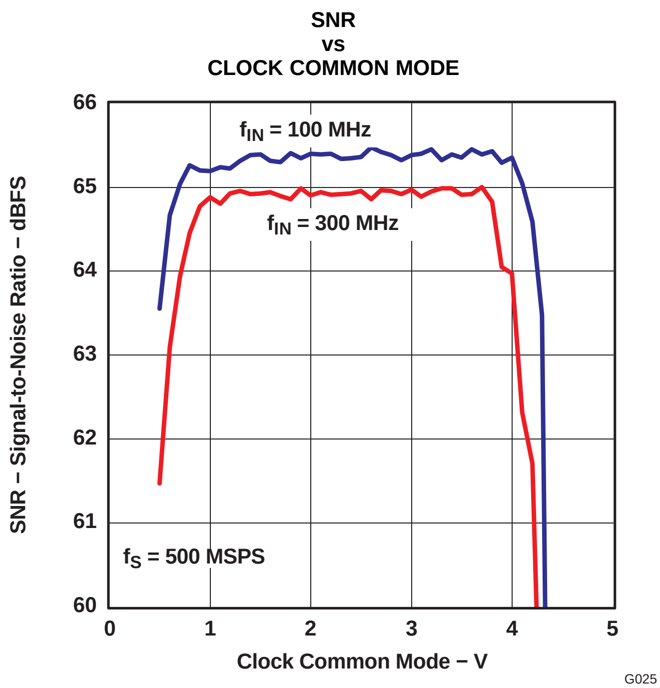


Figure 27.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

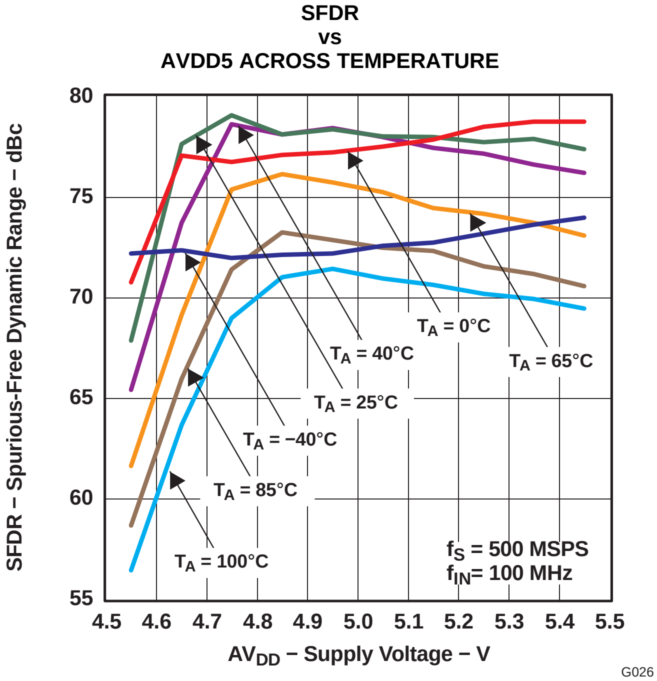


Figure 28.

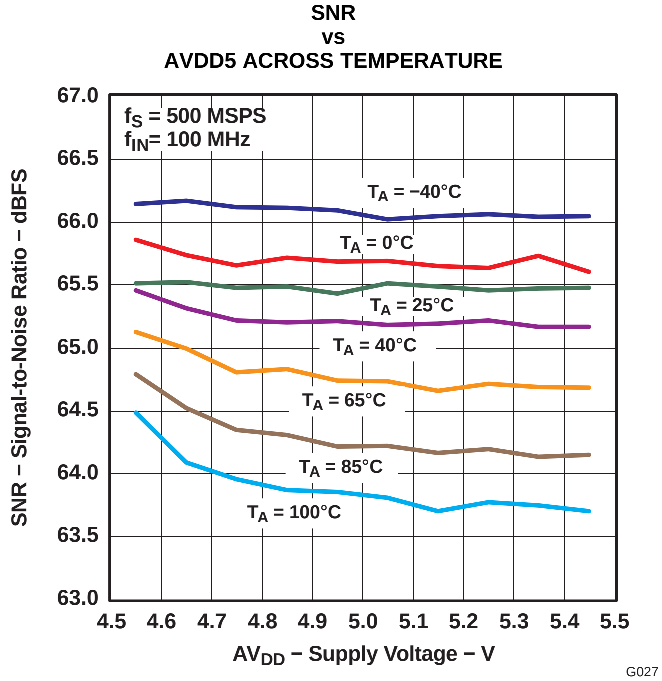


Figure 29.

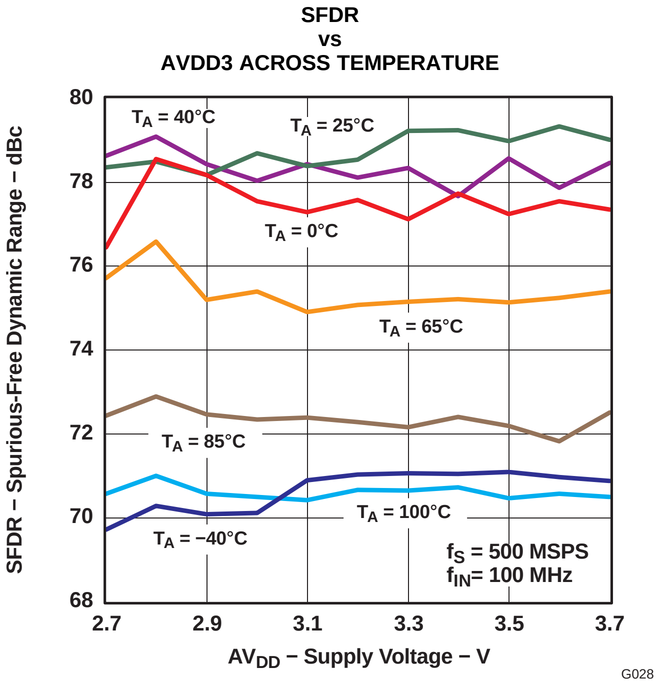


Figure 30.

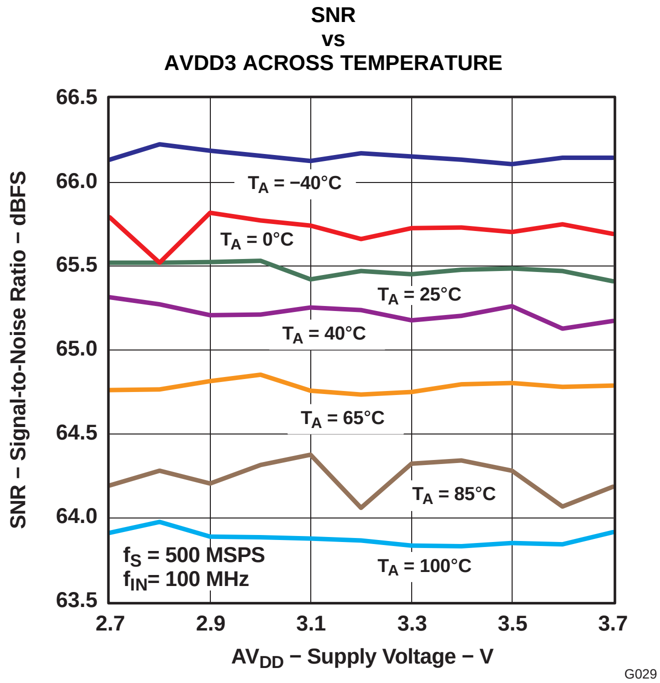


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

SFDR vs DVDD3 ACROSS TEMPERATURE

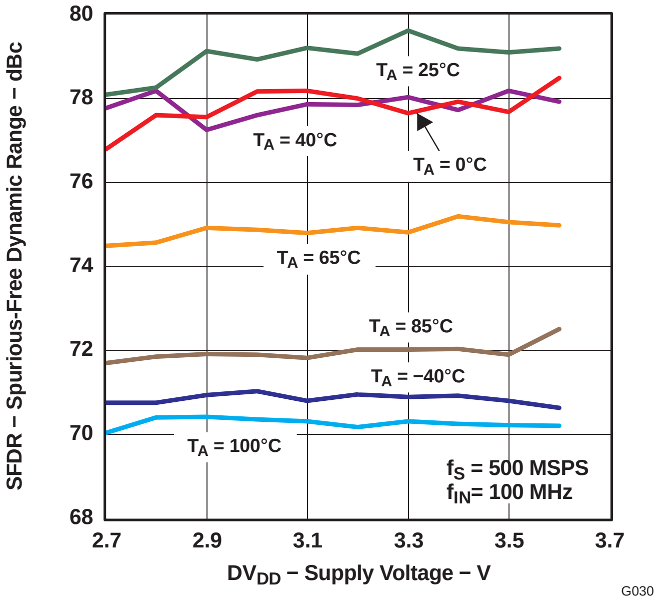


Figure 32.

SNR vs DVDD3 ACROSS TEMPERATURE

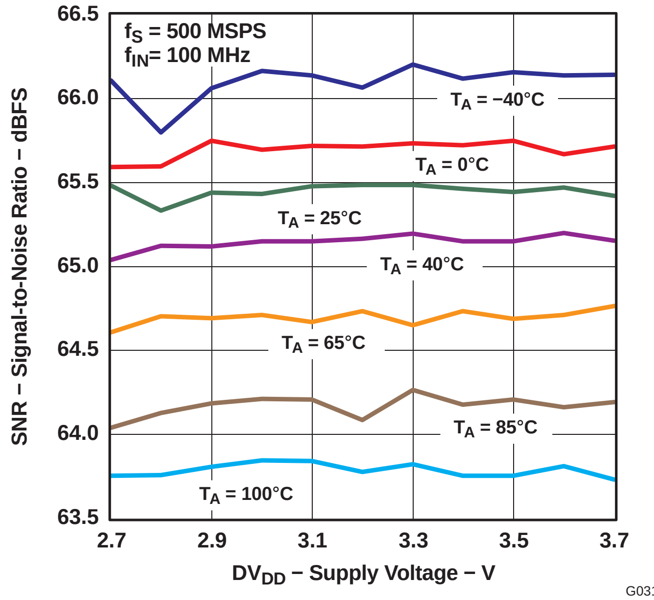


Figure 33.

PSRR vs SUPPLY INJECTED FREQUENCY

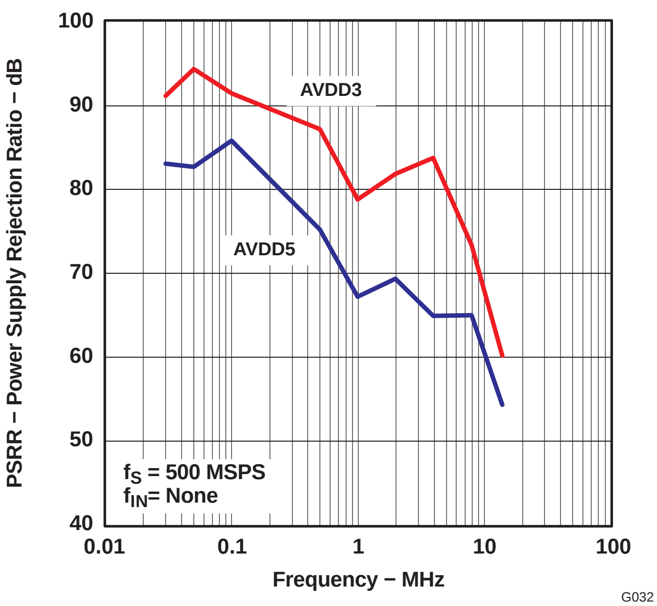


Figure 34.

CMRR vs COMMON-MODE INPUT FREQUENCY

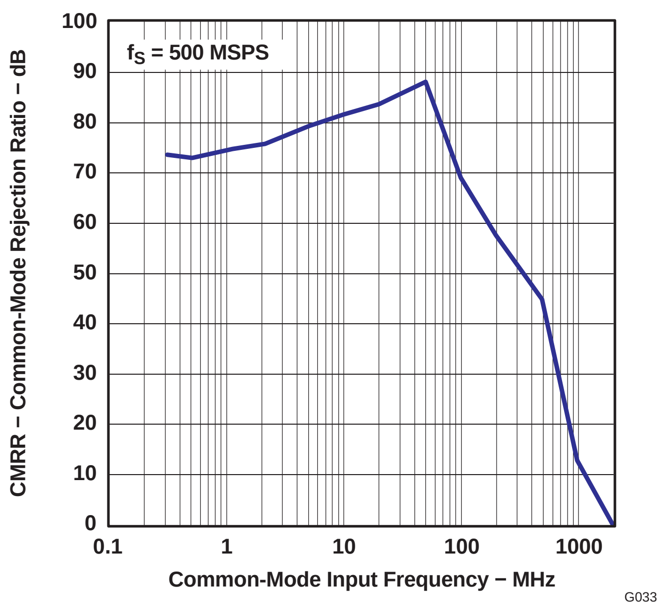


Figure 35.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

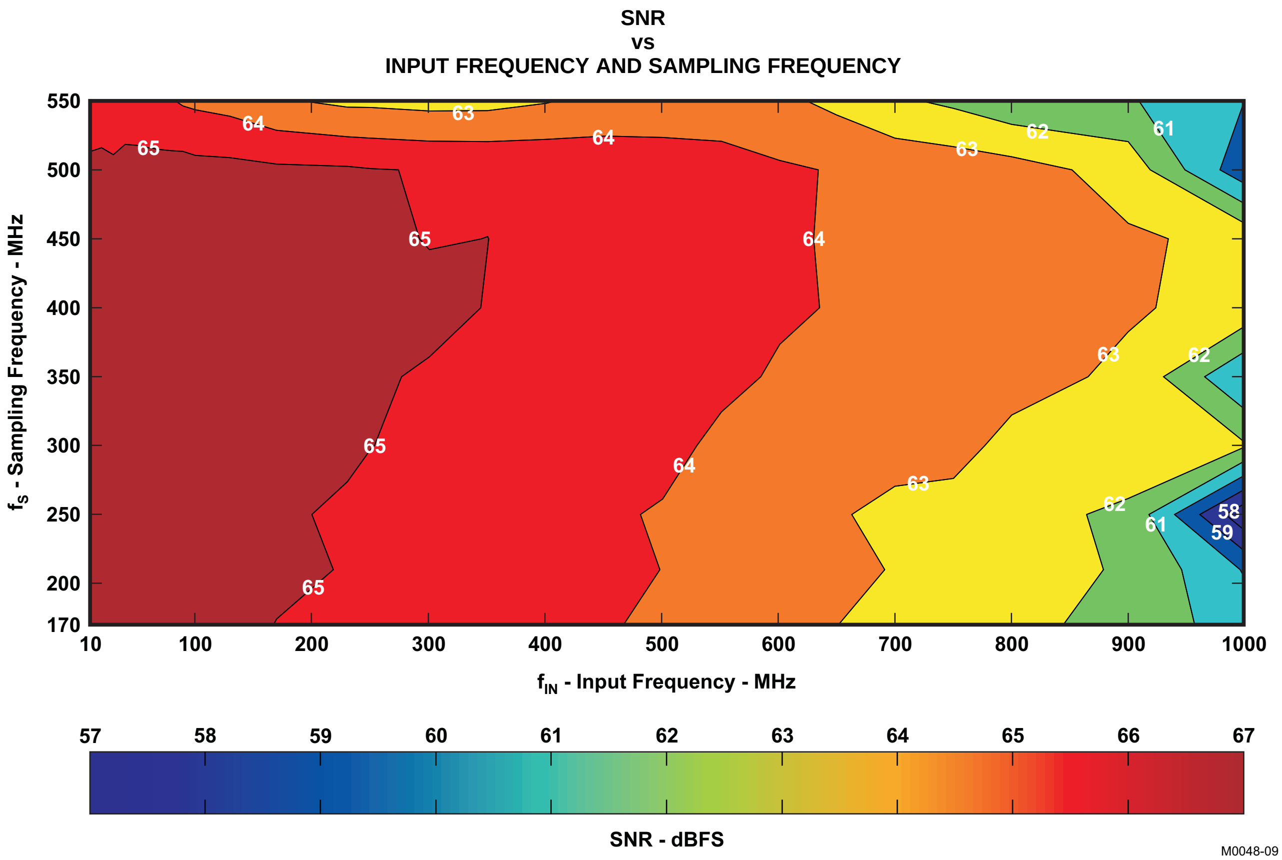


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

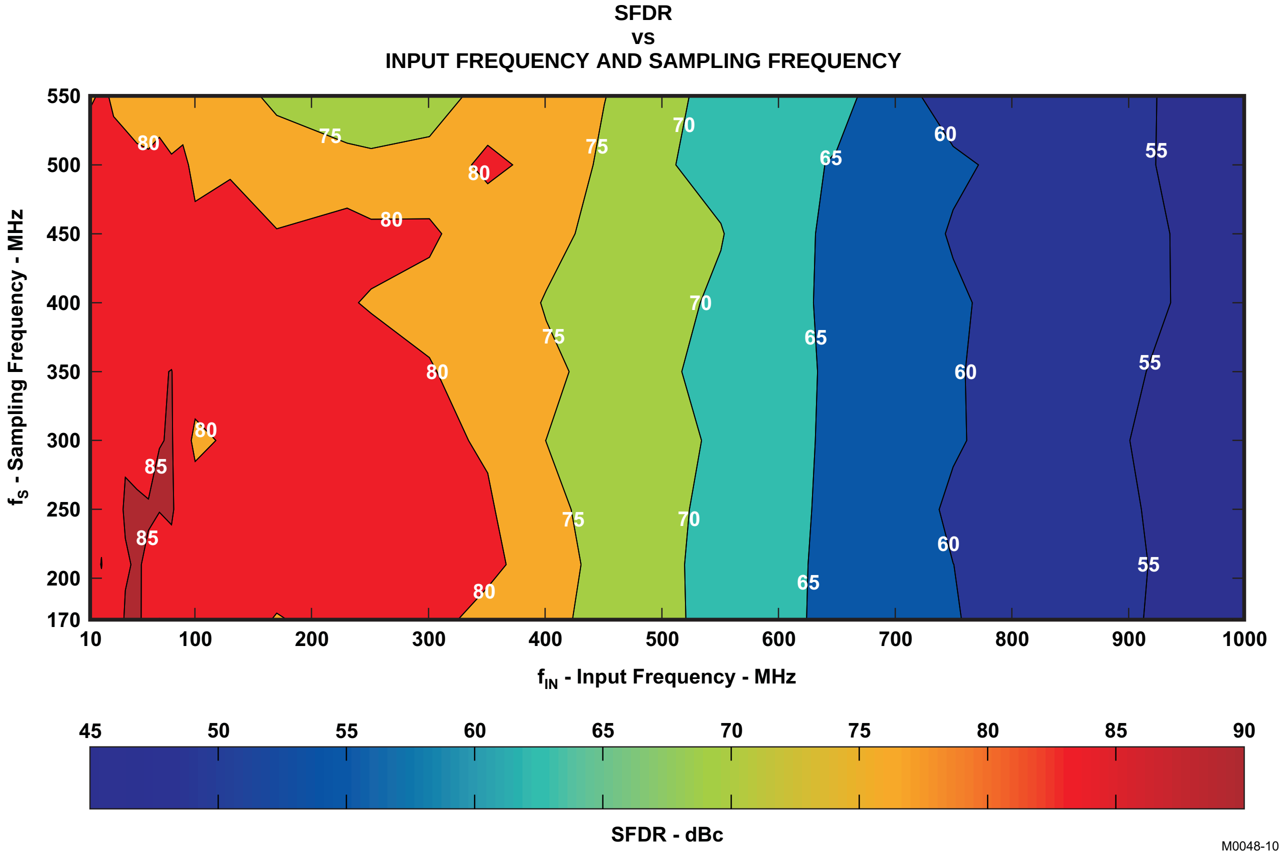


Figure 37.

APPLICATION INFORMATION

Theory of Operation

The ADS5463 is a 12-bit, 500-MSPS, monolithic-pipeline, analog-to-digital converter. Its bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold (T&H), and the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in offset binary format.

Input Configuration

The analog input for the ADS5463 consists of an analog pseudodifferential buffer followed by a bipolar transistor track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500-Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between 2.4 V + 0.55 V and 2.4 V – 0.55 V. This means that each input has a maximum signal swing of 1.1 Vpp for a total differential input signal swing of 2.2 Vpp. The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

The ADS5463 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 38 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the evaluation module is configured with two back-to-back transformers, which also demonstrates good performance. If voltage gain is required, a step-up transformer can be used.

Besides the transformer configurations, Texas Instruments offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain-block amplifier, such as Texas Instruments' THS9001, can also be used for high-input-frequency applications. For large voltage gains at intermediate-frequencies in the 50-MHz to 500-MHz range, the configuration shown in Figure 39 can be used. The component values can be tuned for different intermediate frequencies. The example shown is located on the evaluation module and is tuned for an IF of 170 MHz. More information regarding this configuration can be found in the *ADS5463 EVM User Guide* (SLAU194) and the *THS9001 50 MHz to 350 MHz Cascadeable Amplifier* data sheet (SLOS426).

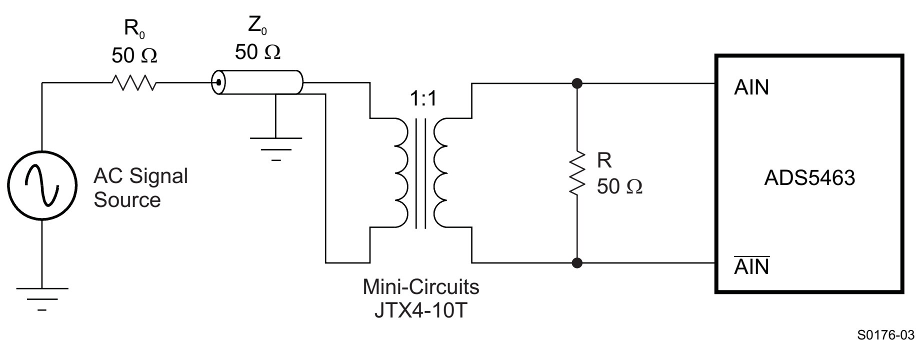


Figure 38. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

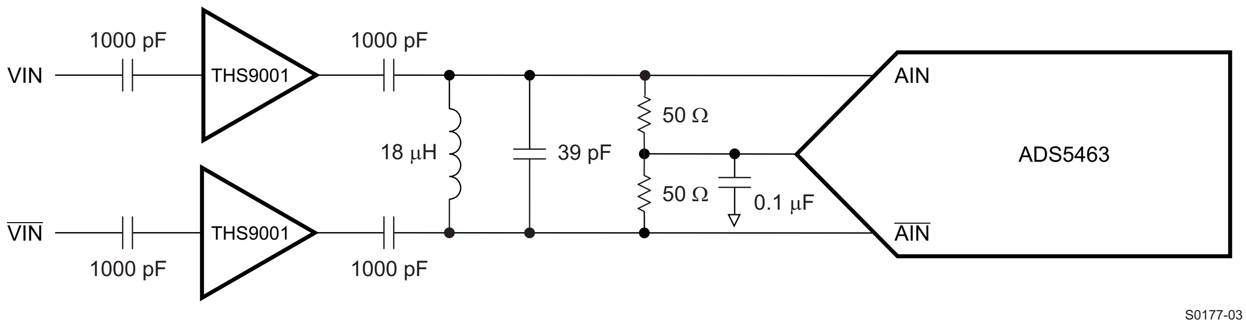


Figure 39. Using the THS9001 IF Amplifier With the ADS5463

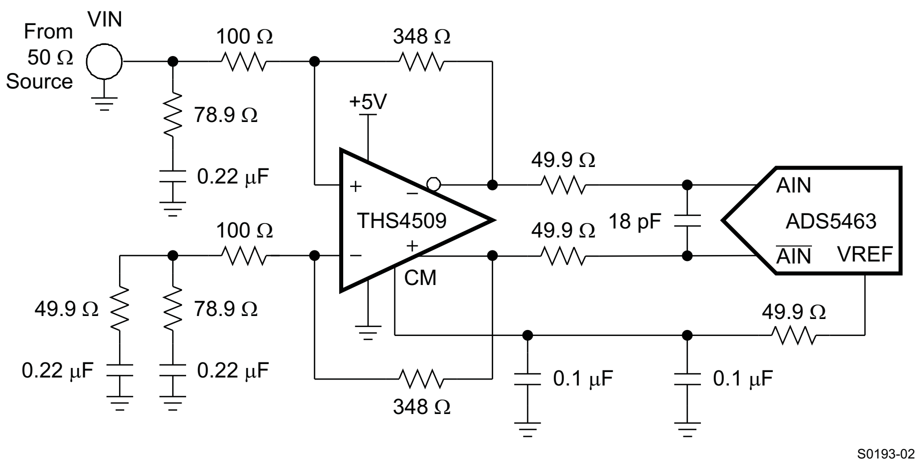


Figure 40. Using the THS4509 With the ADS5463

For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 40) is a good solution, as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10-dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5463. The 50-Ω resistors and 18-pF capacitor between the THS4509 outputs and ADS5463 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB). Input termination is accomplished via the 78.9-Ω resistor and 0.22-µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 78.9-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains. Because the ADS5463 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V S+ = 5 V and V S– = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

Clock Inputs

The ADS5463 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock (see Figure 41) could save some cost and board space without any trade-off in performance. When clocked with this configuration, it is best to connect $\overline{CLK}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 41.

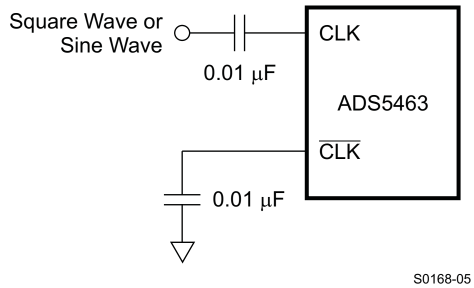


Figure 41. Single-Ended Clock

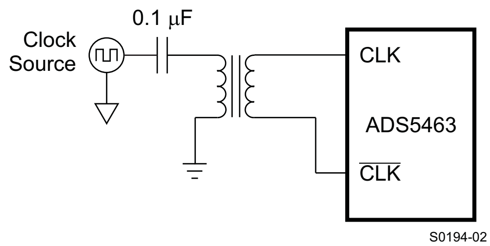


Figure 42. Differential Clock

For jitter-sensitive applications, the use of a differential clock has some advantages (as with any other ADC) at the system level. The differential clock allows for common-mode noise rejection at the PCB level. With a differential clock, the signal-to-noise ratio of the ADC is better for high intermediate frequency applications because the board clock jitter is superior.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. Figure 42 shows this approach. See *Clocking High Speed Data Converters* (SLYT075) for more details.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible due to, for instance, asynchronous clocking, the ADS5463 features good tolerance to clock common-mode variation (see Figure 26 and Figure 27). Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided.

Digital Outputs

The ADC provides 12 data outputs (D11 to D0, with D11 being the MSB and D0 the LSB), a data-ready signal (DRY), and an overrange indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is offset binary. It is recommended to use the DRY signal to capture the output data of the ADS5463. DRY is source-synchronous to the DATA/OVR bits and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. The ADS5463 digital outputs are LVDS-compatible. Due to the high data rates, care should be taken not to overload the digital outputs with too much capacitance, which shortens the data-valid timing window. The values given for timing were obtained with a measured 14-pF parasitic board capacitance to ground on each LVDS line (or 7-pF differential parasitic capacitance).

Power Supplies

The ADS5463 uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5463. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems.

The power consumption of the ADS5463 does not change substantially over clock rate or input frequency as a result of the architecture and process.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source.

The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

- Power up both AVDD3 and DVDD3 at the same time (best scenario), OR
- Keep the voltage difference less than 0.8 V between AVDD3 and DVDD3 during the power up (0.8 V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of msec) for the DVDD3 or AVDD3 pin is 500 mA to avoid potential damage to the device or reduce its lifetime.

The values for the analog and clock inputs given in the Absolute Maximum Ratings are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still being actively driven, the input voltage and current need to be limited to avoid device damage. If the ADC supplies are off, max/min continuous dc voltage is ±0.95 V and max dc current is 20 mA for each input pin (clock or analog), relative to ground.

Layout Information

The evaluation board represents a good guideline of how to lay out the board to obtain the maximum performance from the ADS5463. General design rules, such as the use of multilayer boards, single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors, should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces also should be isolated from other signals, especially in applications where low jitter is required like high IF sampling. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device. The thermal heat sink should be soldered to the board as described in the *PowerPad Package* section. See *ADS5463 EVM User Guide* (SLAU194) on the TI Web site for the evaluation board schematic.

PowerPAD Package

The PowerPAD package is a thermally enhanced standard-size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the *Mechanical Data* section.
2. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13-mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25-mil diameter holes under the package, but outside the thermal pad area, to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the *PowerPAD Made Easy* application brief (SLMA004) or the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay

Clock Pulse Duration/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR)

CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB)

ENOB is a measure in units of bits of a converter's performance as compared to the theoretical limit based on quantization noise

ENOB = (SINAD – 1.76)/6.02

Gain Error

Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL)

INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of the ability to reject frequencies present on the power supply. The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \tag{2}$$

SNR is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter’s full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \tag{3}$$

SINAD is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter’s full-scale range.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10}\frac{P_S}{P_D} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5463MPFPEP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5463MEP	Samples
V62/07607-01XE	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5463MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

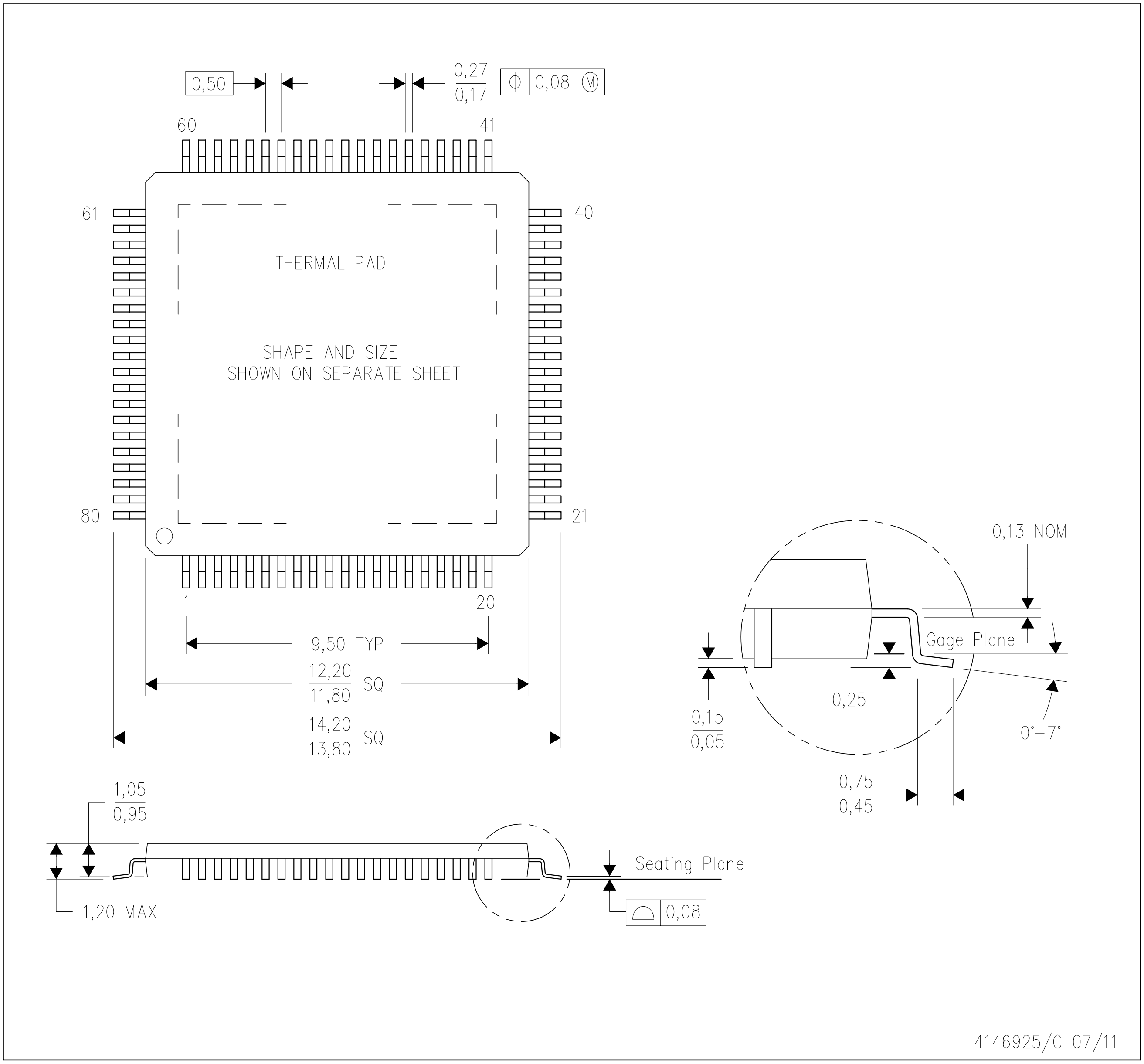
OTHER QUALIFIED VERSIONS OF ADS5463-EP :

- Catalog: ADS5463
- Space: ADS5463-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

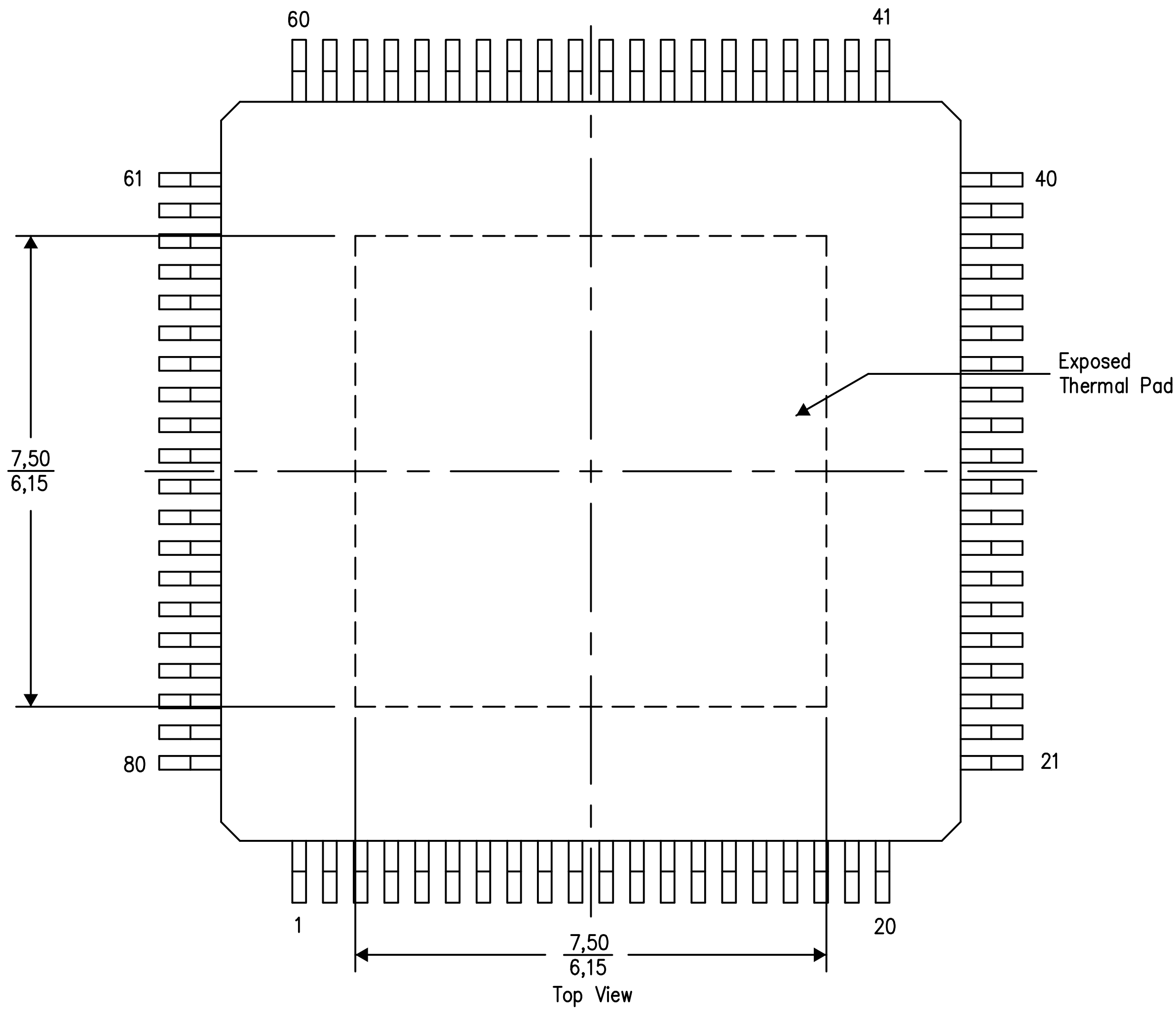
PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



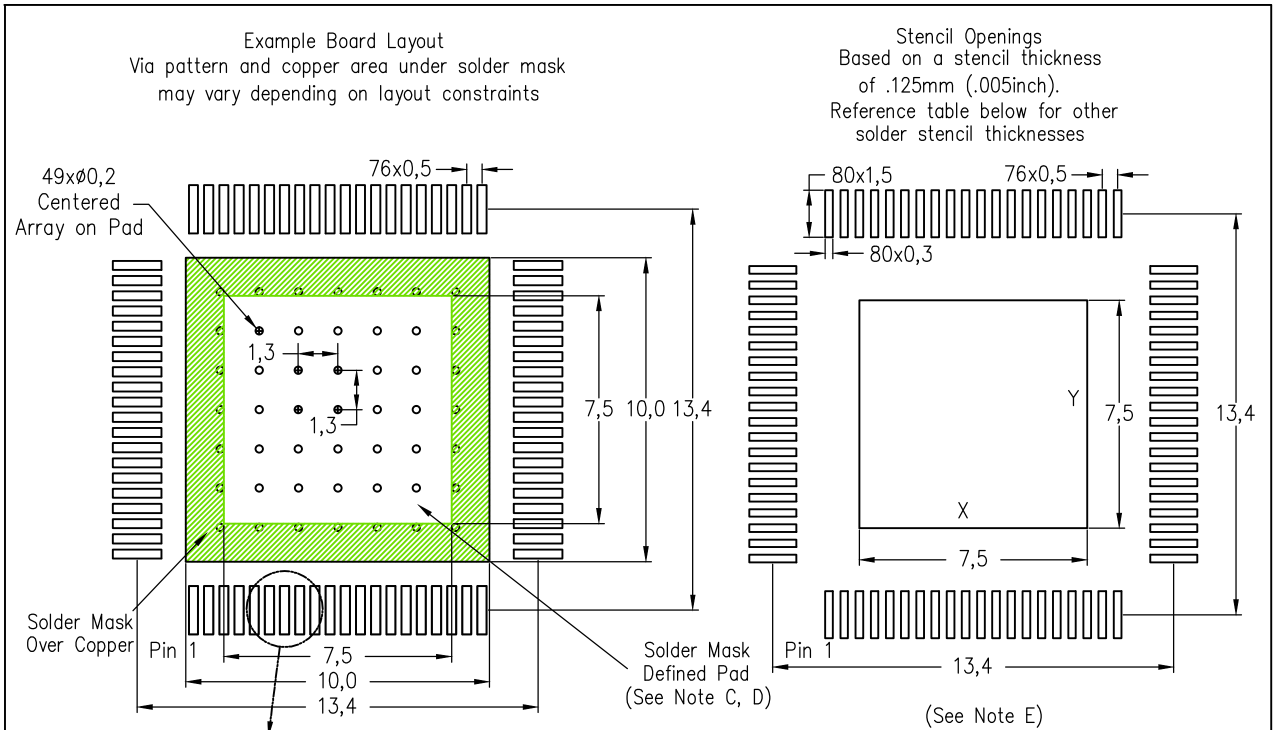
Exposed Thermal Pad Dimensions

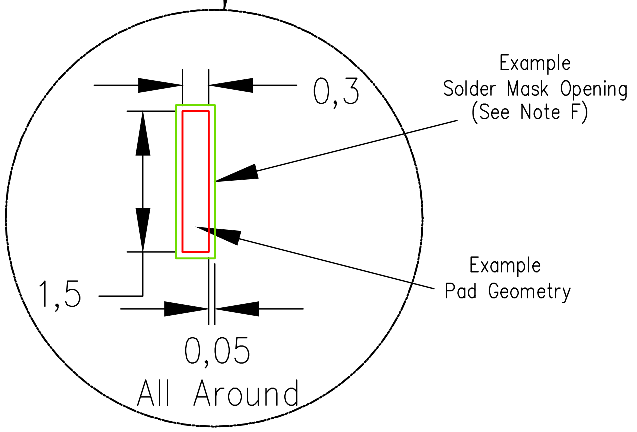
4206327-2/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

4208544-2/G 02/16

PowerPAD is a trademark of Texas Instruments.

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265