bq24295 I²C Controlled 3A Single Cell USB Charger With Narrow VDC 4.5-5.5V Adjustable Voltage at 1.5A Synchronous Boost Operation

1 Features

- 90% High Efficiency Switch Mode 3-A Charger
- 3.9-V to 6.2-V Single Input USB-Compliant Charger with 6.4-V Over-Voltage Protection
  - USB Host or Charging Port D+/D- Detection Compatible to USB Battery Charger Spec (BC1.2)
  - Support Non-Standard 2-A/1-A Adapters Detection
  - Input Voltage and Current Limit Supports USB2.0 and USB 3.0
  - Input Current Limit: 100 mA, 150 mA, 500 mA, 900 mA, 1 A, 1.5 A, 2 A, and 3 A
- Synchronous Boost Converter in Battery Boost Mode with
  - Adjustable Output 4.55 V – 5.5 V at 1.5 A
  - 90% 5.1-V Boost Mode Efficiency
  - Fast OTG Startup (22 ms Typ)
- Narrow VDC (NVDC) Power Path Management
  - Instant System On with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- 1.5-MHz Switching Frequency for Low Profile 1.2-mm Inductor
- I²C Port for Optimal System Performance and Status Reporting
- Autonomous Battery Charging with or without Host Management
  - Battery Charge Enable
  - Battery Charge Preconditioning
  - Charge Termination and Recharge
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±7% Charge Current Regulation
  - ±7.5% Input Current Regulation
  - ±3% Output Voltage Regulation in Boost Mode
- High Integration
  - Power Path Management
  - Synchronous Switching MOSFETs
  - Integrated Current Sensing
  - Bootstrap Diode
  - Internal Loop Compensation
- Safety
  - Battery Temperature Sensing for Charging and Discharging in Boost Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input and System Over-Voltage Protection
  - MOSFET Over-Current Protection
- Charge Status Outputs for LED or Host Processor
- Maximum Power Tracking Capability by Input Voltage Regulation
- 20-µA Low Battery Leakage Current and Support Shipping Mode
- 4mm x 4mm VQFN-24 Package

2 Applications

- Power Bank for Smartphone, Tablet
- Portable Media Players
- Internet Devices

3 Description

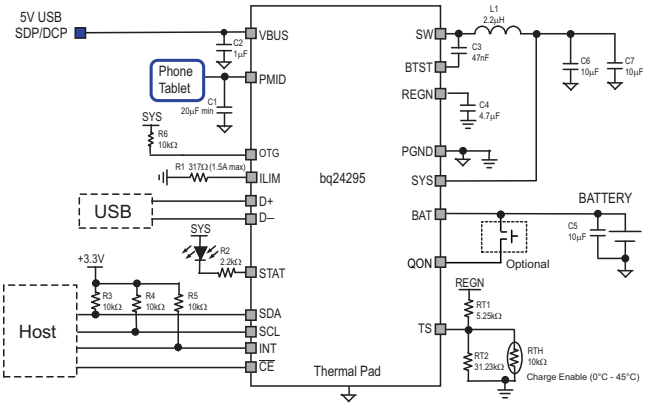
The bq24295 is a highly-integrated switch-mode battery charge management and system power path management devices for 1 cell Li-Ion and Li-polymer battery in a wide range of power bank, tablet and other portable device applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24295	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

bq24295 with USB D+/D- Detection for Charging and Discharging in Boost Mode



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- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Changed 5.52kΩ to 5.25kΩ in *bq24295 with USB D+/D- Detection for Charging and Discharging in Boost Mode* ... 1
- Changed Power Pad to Thermal Pad throughout data sheet ... 1
- Changed REG01[5] to REG01[5] = 1 in OTG description ... 5

- Added (10k NTC thermistor only) to QON description 5
- Changed I_{CHG} = 1792 mA in $I_{ICHG\_REG\_ACC}$ test conditions 8
- Changed falling to rising and TYP to 47.2% in V_{HTF} in *Electrical Characteristics* 9
- Added V_{IH_OTG} to *Electrical Characteristics* 10
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- Changed Table 3 19
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- Changed REG09[5] to REG09[3] in *Battery Over-Voltage Protection (BATOVP)* section 27
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- Changed reset = 10011010, or 0x9A to reset = 10011100, or 0x9C for REG05 35
- Changed 0 to 1 for REG05 Bit 2 Reset 35
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5 Description (Continued)

Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports 3.9V – 6.2V USB input sources, including standard USB host port and USB charging port with 6.4V over-voltage protection. The bq24295 is compliant with USB 2.0 and USB 3.0 power specifications with input current and voltage regulation. To set the default input current limit, the bq24295 detects the input source through D+/D- detection following the USB battery charging spec 1.2. In addition, the bq24295 detects non-standard 2A/1A adapters. The bq24295 supports battery boost operation by supplying adjustable voltage 4.55 – 5.5V (default 5.1V) on PMID pin with minimum current of 1.5A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode operation prevents overloading the input source.

The devices initiate and complete a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

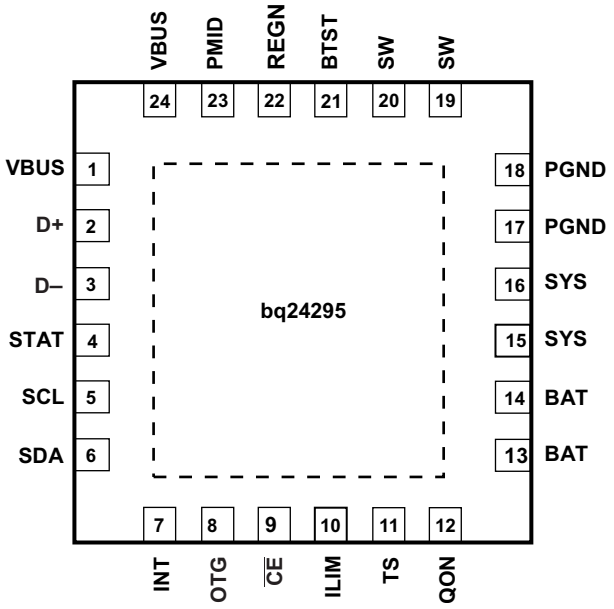
The devices provide various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable).

The STAT output reports the charging status and any fault conditions. The INT immediately notifies the host when a fault occurs.

The bq24295 is available in a 24-pin, 4x4 mm^2 thin VQFN package.

6 Pin Configuration and Functions

RGE Package
24-Pin VQFN With Exposed Thermal Pad
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VBUS	1,24	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
D+	2	I Analog	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
D–	3	I Analog	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
STAT	4	O	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin in the charge blinks at 1 Hz.
SCL	5	I	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	I/O	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	7	O	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
OTG	8	I Digital	OTG Enable pin. The boost mode is activated when the OTG pin is High, REG01[5] = 1, and no Input source is detected at VBUS.
$\overline{CE}$	9	I	Active low Charge Enable pin. Battery charging is enabled when REG01[5:4] = 01 and $\overline{CE}$ pin = Low. $\overline{CE}$ pin must be pulled high or low.
ILIM	10	I	ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1 V. A resistor is connected from ILIM pin to ground to set the maximum limit as I_{INMAX} = (1V/R_{ILIM}) × K_{ILIM}. The actual input current limit is the lower one set by ILIM and by I^2C REG00[2:0]. The minimum input current programmed on ILIM pin is 500 mA.
TS	11	I Analog	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends or Boost disable when TS pin is out of range. A 103AT-2 thermistor is recommended.
QON	12	I	BATFET enable control in shipping mode. A logic low to high transition on this pin with minimum 2ms high level turns on BATFET to exit shipping mode. It has internal 1MΩ (Typ) pull down. For backward compatibility, when BATFET enable control function is not used, the pin can be a no connect or tied to TS pin (10k NTC thermistor only). (Refer to *Shipping Mode* for detail description).
BAT	13,14	P	Battery connection point to the positive pin of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10 µF closely to the BAT pin.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
SYS	15,16	I	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage.
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	O	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	P	Battery Boost Mode Output Voltage. Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. The minimum capactiance required on PMID to PGND is 20 µF
Thermal Pad		P	Exposed pad beneath the IC for heat dissipation. Always solder thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage (with respect to GND)	VBUS (converter not switching)	–2	15(2)	V
	PMID (converter not switching)	–0.3	15(2)	V
	STAT	–0.3	12	V
	BTST	–0.3	12	V
	SW	–2	7 8 (Peak for 20ns duration)	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, ILIM, REGN, TS, QON, $\overline{CE}$, D+, D–,	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
Output sink current	INT, STAT		6	mA
Junction temperature		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground pin unless otherwise noted.
(2) VBUS is specified up to 16 V for a maximum of 24 hours under no load conditions.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.9	6.2 (1)	V
I_{IN}	Input current (VBUS)		3	A
I_{SYS}	Output current (SYS)		3.5	A
V_{BAT}	Battery voltage		4.4	V
I_{BAT}	Fast charging current		3	A
	Discharging current with internal MOSFET		5.5	A
T_A	Operating free-air temperature range	–40	85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

7.4 Thermal Information

THERMAL METRIC (1)		bq24295 RGE (VQFN) 24 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS)	$V_{VBUS} < V_{UVLO}$, VBAT = 4.2 V, leakage between BAT and VBUS		5		µA
		High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1), –40°C – 85°C		16	20	µA
		High-Z Mode, or no VBUS, BATFET enabled (REG07[5] = 0), –40°C – 85°C		32	55	µA
I_{VBUS}	Input supply current (VBUS)	V_{VBUS} = 5 V, High-Z mode, No battery		15	30	µA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0 A		4		mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, charge disable, V_{BAT} = 3.8 V, I_{SYS} = 100 µA		3.5		mA
I_{BOOST}	Battery discharge current in boost mode	VBAT = 4.2 V, Boost mode, I_{PMID} = 0 A, converter switching		3.5		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating voltage		3.9		6.2	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery	V_{VBUS} rising	3.6			V
V_{SLEEP}	Sleep mode falling threshold	V_{VBUS} falling, $V_{VBUS-VBAT}$	35	80	120	mV
V_{SLEEPZ}	Sleep mode rising threshold	V_{VBUS} rising, $V_{VBUS-VBAT}$	170	250	350	mV
V_{ACOV}	VBUS over-voltage rising threshold	V_{VBUS} rising	6.2		6.6	V
V_{ACOV_HYST}	VBUS over-voltage falling hysteresis	V_{VBUS} falling		250		mV
V_{BAT_UVLOZ}	Battery for active I^2C, no VBUS	V_{BAT} rising	2.3			V
V_{BAT_DPL}	Battery depletion threshold	V_{BAT} falling		2.4	2.6	V
$V_{BAT\_DPL\_HY}$	Battery depletion rising hysteresis	V_{BAT} rising		200		mV

Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VBUSMIN}$	Bad adapter detection threshold	V_{VBUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
POWER PATH MANAGEMENT						
V_{SYS_MAX}	Typical system regulation voltage	Isys = 0 A, BATFET (Q4) off, V_{BAT} up to 4.2 V, REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.5		4.35	V
V_{SYS_MIN}	System voltage outpu	REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.5	3.65		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMIID			28	41	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance between PMID and SW	T_J = –40°C – 85°C		39	51	mΩ
		T_J = -40°C – 125°C		39	58	
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between SW and PGND	T_J = –40°C – 85°C		61	82	mΩ
		T_J = -40°C – 125°C		61	90	
V_{FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10mA		30		mV
V_{SYS_BAT}	SYS/BAT comparator	V_{SYS} falling		70		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising		3.55		V
V_{BATGD_HYST}	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.112 V and 4.208 V	–0.5%		0.5%	
$I_{ICHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.8 V, I_{CHG} = 1024 mA, T_J = 25°C	-4%		4%	
		V_{BAT} = 3.8 V, I_{CHG} = 1024 mA, T_J = -20°C – 125°C	-7%		7%	
		V_{BAT} = 3.8 V, I_{CHG} = 1792 mA, T_J = -20°C – 125°C	–10%		10%	
I_{CHG_20pct}	Charge current with 20% option on	V_{BAT} = 3.1 V, I_{CHG} = 104 mA, REG02 = 03 and REG02[0] = 1	75		175	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV\_HYST}$	Battery LOWV rising threshold	Precharge to fast charge, REG04[1] = 1 (Typical 200-mV hysteresis)	2.8	3.0	3.1	V
I_{PRECHG_ACC}	Precharge current regulation accuracy	VBAT = 2.6 V, I_{CHG} = 256 mA	–20%		20%	
$I_{TYP\_TERM\_ACC}$	Typical termination current	I_{TERM} = 256 mA, I_{CHG} = 2048 mA		265		mA
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 256 mA, I_{CHG} = 2048 mA	–22.5%		22.5%	
V_{SHORT}	Battery short voltage	VBAT falling		2.0		V
V_{SHORT_HYST}	Battery Short Voltage hysteresis	VBAT rising		200		mV
I_{SHORT}	Battery short current	VBAT < 2.2 V		100		mA
V_{RECHG}	Recharge threshold below VBAT_REG	VBAT falling, REG04[0] = 0		100		mV
t_{RECHG}	Recharge deglitch time	VBAT falling, REG04[0] = 0		20		ms
R_{ON_BATFET}	SYS-BAT MOSFET on-resistance	T_J = 25°C		24	28	mΩ
		T_J = –40°C – 125°C		24	35	
INPUT VOLTAGE/CURRENT REGULATION						
$V_{INDPM\_REG\_ACC}$	Input voltage regulation accuracy		-2%		2%	
I_{USB_DPM}	USB Input current regulation limit, VBUS = 5V, current pulled from SW	USB100	85		100	mA
		USB150	125		150	mA
		USB500	440		500	mA
		USB900	750		900	mA
I_{ADPT_DPM}	Input current regulation accuracy	IADP = 1.5 A, REG00[2:0] = 101	1.3		1.5	A
I_{IN_START}	Input current limit during system start up	VSYS < 2.2 V		100		mA
K_{ILIM}	$I_{IN} = K_{ILIM}/R_{ILIM}$	IINDPM = 1.5 A	395	435	475	A x Ω
D+/D- DETECTION						
V_{D+_SRC}	D+ voltage source		0.5		0.7	V
I_{D+_SRC}	D+ connection check current source		7		14	µA
I_{D-_SINK}	D– current sink		50	100	150	µA

Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{D_LKG}	Leakage current into D+/D–	D–, switch open	–1		1	µA
		D+, switch open	–1		1	µA
V_{D+_LOW}	D+ low comparator threshold				0.8	V
$V_{D-\_LOWdatref}$	D– low comparator threshold		250		400	mV
R_{D-_DWN}	D– pulldown for connection check		14.25		24.8	kΩ
$t_{SDP\_DEFAULT}$	Charging timer with 100mA USB host in default mode				45	mins
V_{adpt1_lo}	D+ low comparator threshold for non-standard adapter Divider-1	As percentage of REGN, 0°C – 85°C(1)	46.5%	48%	49.5%	
V_{adpt1_hi}	D+ low comparator threshold for non-standard adapter divider-1	As percentage of REGN, 0°C – 85°C(1)	58.5%	60%	61.5%	
V_{adpt2_lo}	D+ low comparator threshold for non-standard adapter divider-2	As percentage of REGN, 0°C – 85°C(1)	15.5%	17%	18.5%	
V_{adpt2_hi}	D+ low comparator threshold for Non-standard adapter divider-2	As percentage of REGN, 0°C – 85°C(1)	28.5%	30%	31.5%	
V_{adpt3_lo}	D- low comparator threshold for non-standard adapter divider-3	As percentage of REGN, 0°C – 85°C(1)	46.5%	48%	49.5%	
V_{adpt3_hi}	D- high comparator threshold for non-standard adapter divider-3	As percentage of REGN, 0°C – 85°C(1)	58.5%	60%	61.5%	
BAT OVER-VOLTAGE PROTECTION						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%		
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{Junction\_REG}$	Junction temperature regulation accuracy	REG06[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		160		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			30		°C
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
COLD/HOT THERMISTER COMPARATOR						
V_{LTF}	Cold temperature threshold, TS pin voltage rising threshold	Charger suspends charge. as percentage to V_{REGN}	73%	73.5%	74%	
V_{LTF_HYS}	Cold temperature hysteresis, TS pin voltage falling	As percentage to V_{REGN}		0.4%		
V_{HTF}	Hot temperature TS pin voltage rising threshold	As percentage to V_{REGN}	46.6%	47.2%	48.8%	
V_{TCO}	Cut-off temperature TS pin voltage falling threshold	As percentage to V_{REGN}	44.2%	44.7%	45.2%	
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		10		ms
VBCOLD0	Cold temperature threshold, TS pin voltage rising threshold	As percentage to V_{REGN} REG02[1] = 0 (Approx. -10°C w/ 103AT)	75.5%	76%	76.5%	
VBCOLD0_HYS		As percentage to V_{REGN} REG02[1] = 0 (Approx. 1°C w/ 103AT)		1%		
VBCOLD1	Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to V_{REGN} REG02[1] = 1 (Approx. -20°C w/ 103AT)	78.5%	79%	79.5%	
VBCOLD1_HYS		As percentage to V_{REGN} REG02[1] = 1 (Approx. 1°C w/ 103AT)		1%		
VBHOT0	Hot temperature threshold, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 01 (Approx. 55°C w/ 103AT)	35.5%	36%	36.5%	
VBHOT0_HYS		As percentage to V_{REGN} REG06[3:2] = 01 (Approx. 3°C w/ 103AT)		3%		
VBHOT1	Hot temperature threshold 1, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 00 (Approx. 60°C w/ 103AT)	32.5%	33%	33.5%	

(1) REGN LDO is configured in drop-out mode. VBUS is close to REGN when I_{REGN} = 0 mA.

Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBHOT1_HYS		As percentage to V_{REGN} REG06[3:2] = 00 (Approx. 3°C w/ 103AT)		3%		
VBHOT2	Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 10 (Approx. 65°C w/ 103AT)	29.5%	30%	30.5%	
VBHOT2_HYS		As percentage to V_{REGN} REG06[3:2] = 10 (Approx. 3°C w/ 103AT)		3%		
CHARGE OVER-CURRENT COMPARATOR						
I_{HSFET_OCP}	HSFET cycle by cycle over-current threshold		5.3	7.5		A
I_{BATFET_OCP}	System over load threshold		5.5	6.6		A
V_{LSFET_UCP}	LSFET charge under-current falling threshold	From sync mode to non-sync mode		100		mA
F_{SW}	PWM Switching frequency, and digital clock		1300	1500	1700	kHz
D_{MAX}	Maximum PWM duty cycle			97%		
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold	VBTST-VSW when LSFET refresh pulse is requested, VBUS = 5 V		3.6		V
BOOST MODE OPERATION						
V_{OTG_REG}	Boost mode output voltage	I(PMID) = 0, REG06[7:4] = 1001 (5.126 V)		5.12		V
$V_{OTG\_REG\_ACC}$	Boost mode output voltage accuracy	I(PMID) = 0, REG06[7:4] = 1001 (5.126 V)	-3%		3%	
V_{OTG_BAT}	Battery voltage exiting boost mode	BAT falling, REG04[1] = 1	2.9			V
I_{OTG}	Boost mode output current on PMID		1.3			A
V_{OTG_OVP}	OTG over-voltage threshold	Rising threshold	5.8	6		V
$V_{OTG\_OVP\_HYS}$	OTG over-voltage threshold hysteresis	Falling threshold		300		mV
I_{OTG_LSOCP}	LSFET cycle by cycle current limit		5			A
I_{OTG_HSZCP}	HSFET under current falling threshold			100		mA
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 6 V, I_{REGN} = 40 mA	4.8	5	5.5	V
		V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.7	4.8		V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5 V, V_{REGN} = 3.8 V	50			mA
LOGIC I/O PIN CHARACTERISTICS (OTG, $\overline{CE}$, STAT, QON)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold ($\overline{CE}$, STAT, QON)		1.3			V
V_{IH_OTG}	Input high threshold (OTG)		1.1			V
V_{OUT_LO}	Output low saturation voltage	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current (OTG, $\overline{CE}$, STAT)	Pull-up rail 1.8 V			1	µA
I_{BIAS}	High level leakage current (QON)	Pull-up rail 3.6 V			8	µA
I^2C INTERFACE (SDA, SCL, INT)						
V_{IH}	Input high threshold level	VPULL-UP = 1.8 V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	VPULL-UP = 1.8 V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS}	High-level leakage current	VPULL-UP = 1.8 V, SDA and SCL			1	µA
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{HIZ}	Digital crude clock	REGN LDO disabled	15	35	50	kHz
f_{DIG}	Digital clock	REGN LDO enabled	1300	1500	1700	kHz

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
VBUS/BAT POWER UP						
t_{BADSRC}	Bad source detection duration			30		ms
QON TIMING						
t_{QON}	QON pin high time to turn on BATFET		2			ms
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[5:4] = 11	REGN LDO disabled	112	160		s
		REGN LDO enabled	136	160		

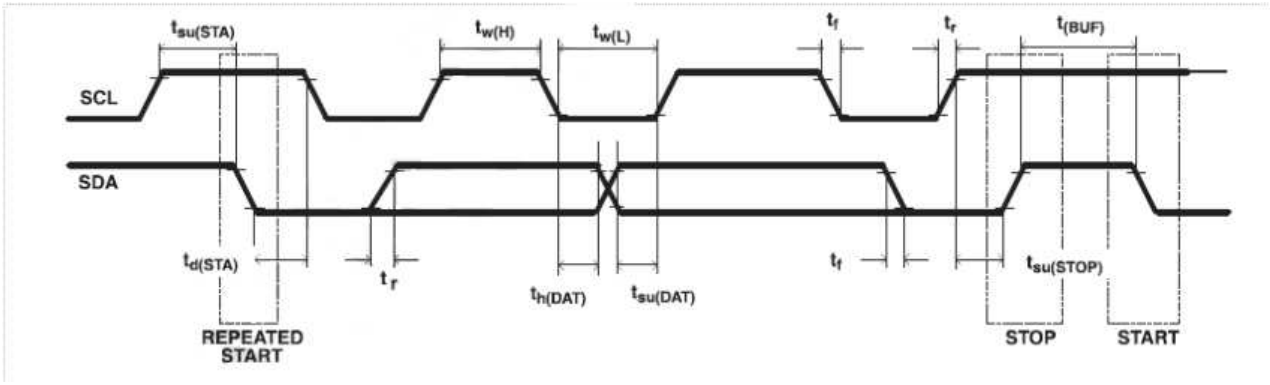


Figure 1. I²C-Compatible Interface Timing Diagram

7.7 Typical Characteristics

Table 1. Table of Figures

	FIGURE
Charging Efficiency vs Charging Current (DCR = 10 mΩ)	Figure 2
System Efficiency vs System Load Current (DCR = 10 mΩ)	Figure 3
Boost Mode Efficiency vs VBUS Load Current (DCR = 10 mΩ)	Figure 4
SYS Voltage Regulation vs System Load Current	Figure 5
Boost Mode PMID Voltage Regulation (Typical Output = 5.126 V, REG06[7:4] = 1001) vs PMID Load Current	Figure 6
SYS Voltage vs Temperature	Figure 7
BAT Voltage vs Temperature	Figure 8
Input Current Limit vs Temperature	Figure 9
Charge Current vs Package Temperature	Figure 10

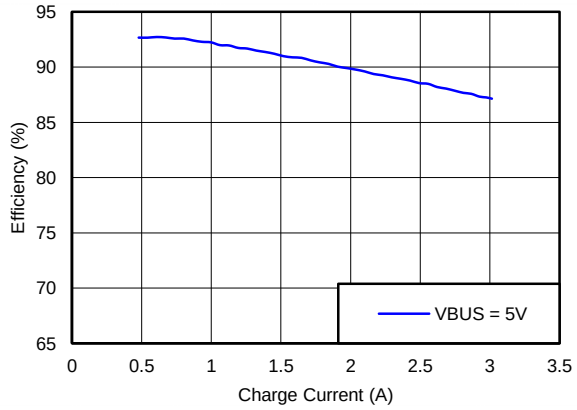


Figure 2. Charge Efficiency vs Charge Current

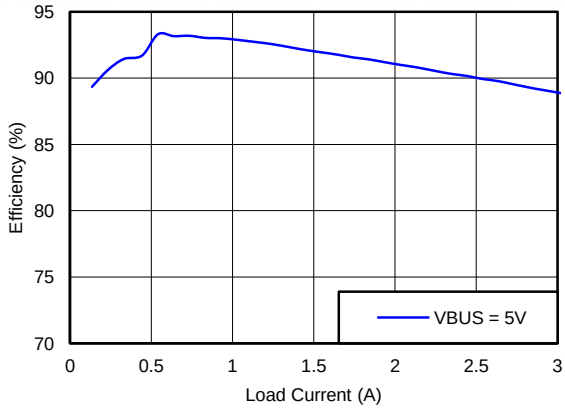


Figure 3. System Efficiency vs System Load Current

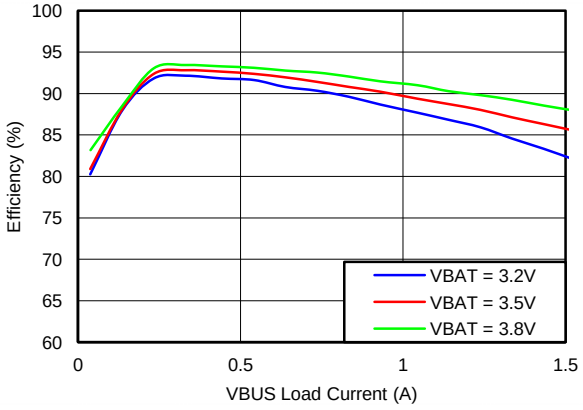


Figure 4. Boost Mode Efficiency vs VBUS Load Current

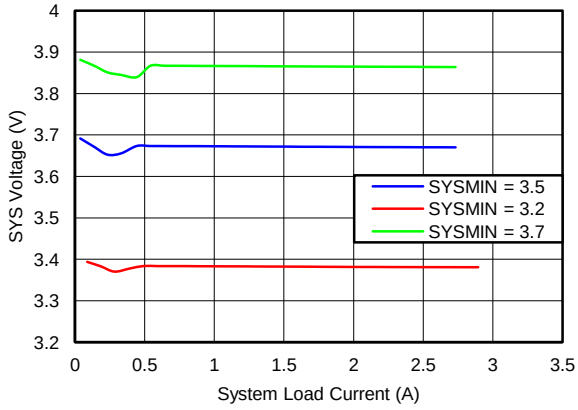
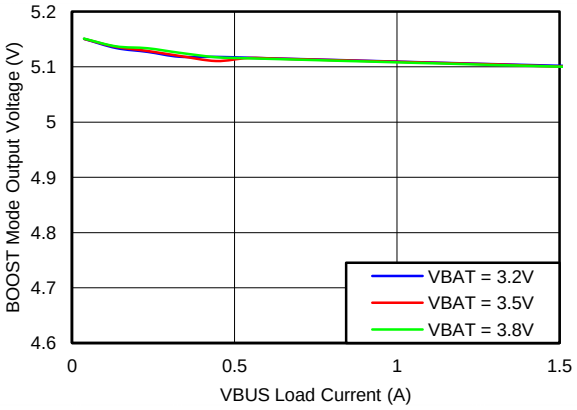


Figure 5. SYS Voltage Regulation vs System Load Current



Typical Output = 5.126 V, REG06[7:4] = 1001

Figure 6. Boost Mode PMID Voltage Regulation vs PMID Load Current

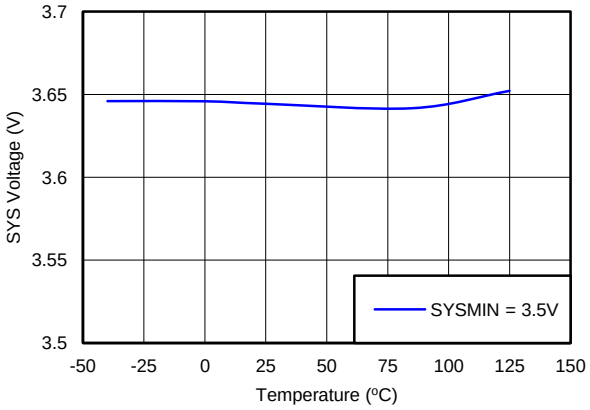


Figure 7. SYS Voltage vs Temperature

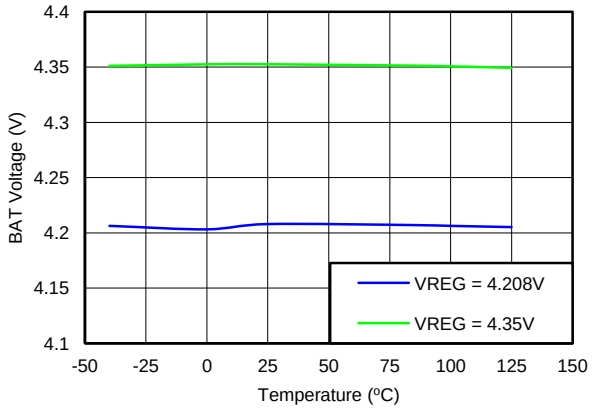


Figure 8. BAT Voltage vs Temperature

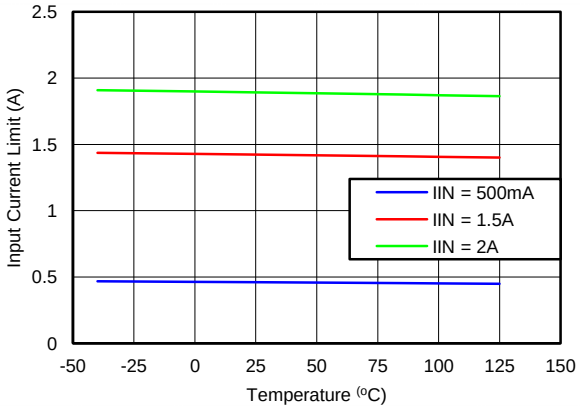


Figure 9. Input Current Limit vs Temperature

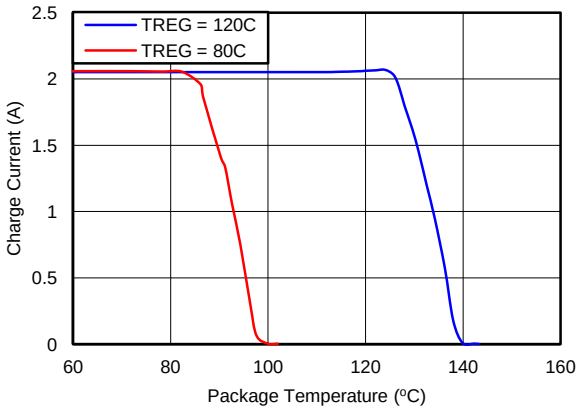


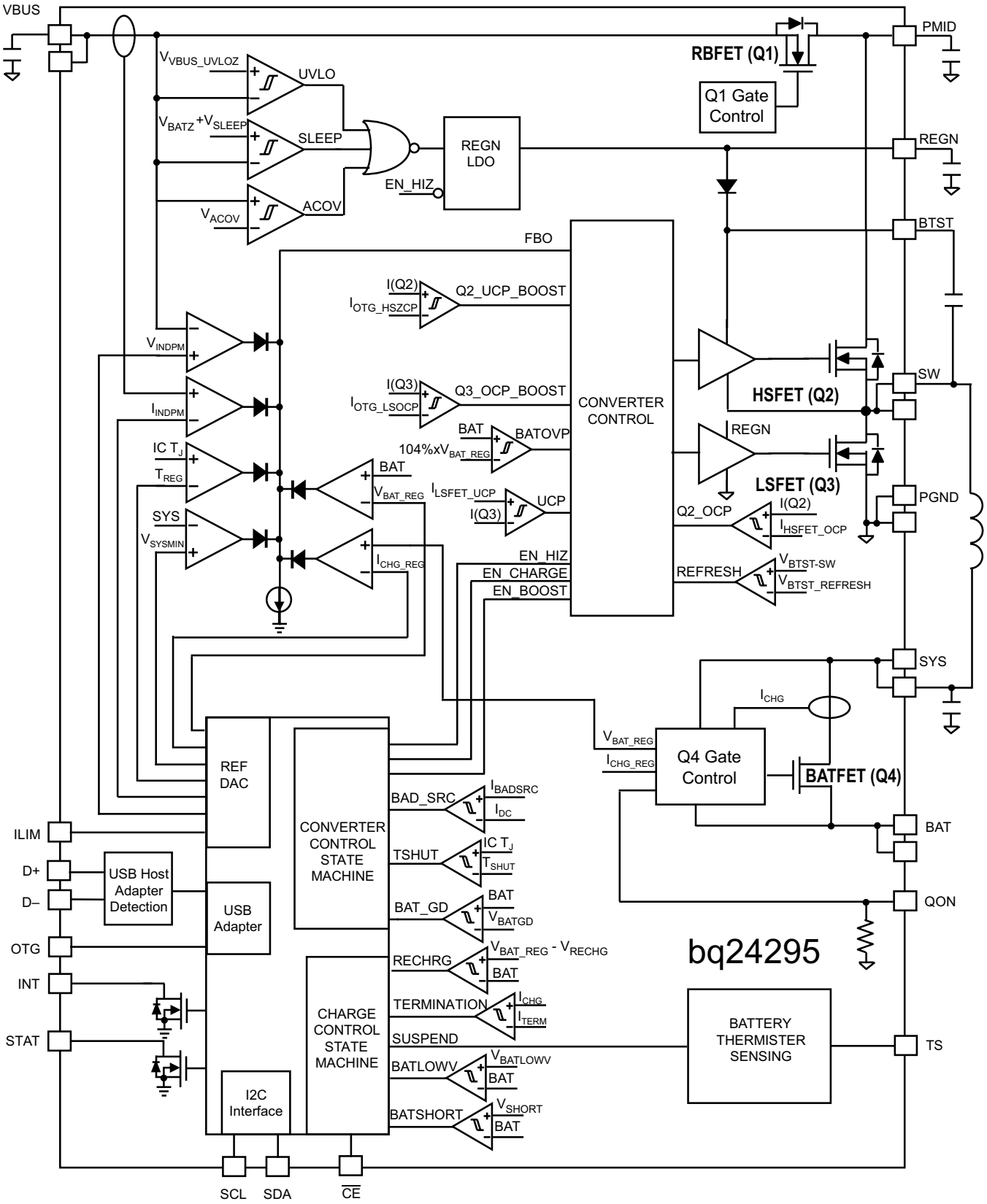
Figure 10. Charge Current vs Package Temperature

8 Detailed Description

8.1 Overview

The bq24295 is an I^2C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power Up

8.3.1.1 Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.3.1.2 Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DEPL}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. During both boost and charge mode, the device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

8.3.1.2.1 BATFET Turn Off

The BATFET can be forced off by the host through I^2C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery. When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

8.3.1.2.2 Shipping Mode

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage. The BATFET can be turned off by setting REG07[5] (BATFET_DISABLE) bit.

In order to keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4] = 00) and disable BATFET (REG07[5] = 1) at the same time. Once the BATFET is disabled, one of the following events can turn on BATFET and clear REG07[5] (BATFET_DISABLE) bit.

1. Plug in adapter
2. Write REG07[5] = 0
3. watchdog timer expiration
4. Register reset (REG01[7] = 1)
5. A logic low to high transition on QON pin (refer to Figure 11 for detail timing)

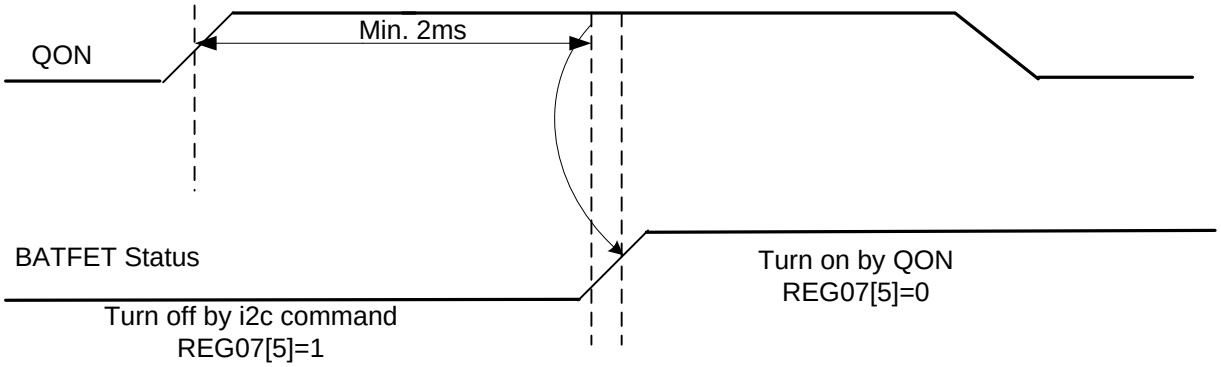


Figure 11. QON Timing

Feature Description (continued)

8.3.1.3 Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through PMID pin. The boost mode output current rating meets the 1.5-A charging requirements for smartphone and tablet. The boost operation is enabled by default if the conditions are valid:

1. BAT above BATLOWV threshold ($V_{BATLOWV}$ set by REG04[1])
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4] = 10)
4. After 30ms delay from boost mode enable

In battery boost mode, the device employs a 1.5-MHz step-up switching regulator. During boost mode, the status register REG08[7:6] is set to 11, the PMID output voltage is 5.1 V. In addition, the device provides adjustable boost voltage from 4.55 V to 5.5 V by changing BOOSTV bits in REG06[7:4]. Any fault during boost operation, including PMID over-voltage, sets the fault register REG09[6] to 1 and an INT is asserted.

For power bank applications, the boost current is supported from PMID pin as in the application diagram. It is recommended to use the minimum PMID cap value 20 uF for boost current. Please note that there is no boost current limit setting when the boost current is sourced from PMID pin, hence it is important not to overload the boost current under this condition.

8.3.1.3.1 Integrated Control to Switch Between USB Charge Mode and Boost Mode

The device features integrated control to switch between charge mode and boost mode by monitoring VBUS voltage. When VBUS is higher than VBAT+V_{SLEEP} , the RBFET is enabled and charge mode is enabled. When VBUS power source is removed, the RBFET is automatically turn off to isolate VBUS from PMID. The boost mode is started when the conditions described above are met.

8.3.1.4 Power Up from DC Source

When the DC source plugs in, the charger device checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

8.3.1.4.1 REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.

1. VBUS above V_{VBUS_UVLOZ}
2. VBUS above V_{BAT} + V_{SLEEPZ} in buck mode or VBUS below V_{BAT} + V_{SLEEP} in boost mode
3. After typical 220-ms delay (100 ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS} (15 µA typical) from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.3.1.4.2 Input Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below V_{ACOV} (not in VBUS over-voltage)
2. VBUS voltage above V_{BADSRC} (3.8 V typical) when pulling I_{BADSRC} (30 mA typical) (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

Feature Description (continued)

8.3.1.4.3 Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (500 mA in USB 2.0, and 150 mA/900 mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 3 A.

After the REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The bq24295 follows Battery Charging Specification 1.2 (BC1.2) to detect input source through USB D+/D- lines. After the input current limit detection is done, the detection result is reported in VBUS_STAT registers (REG08[7:6]) and input current limit is updated in IINLIM register (REG00[2:0]). In addition, host can write to REG00[2:0] to change the input current limit.

8.3.1.4.4 D+/D– Detection Sets Input Current Limit

The bq24295 contains a D+/D– based input source detection to program the input current limit. The D+/D- detection has three steps: data contact detect (DCD), primary detection, and non-standard adapter detection. When the charging source passes data contact detect, the device would proceed to run primary detection. Otherwise the charger would proceed to run non-standard adapter detection.

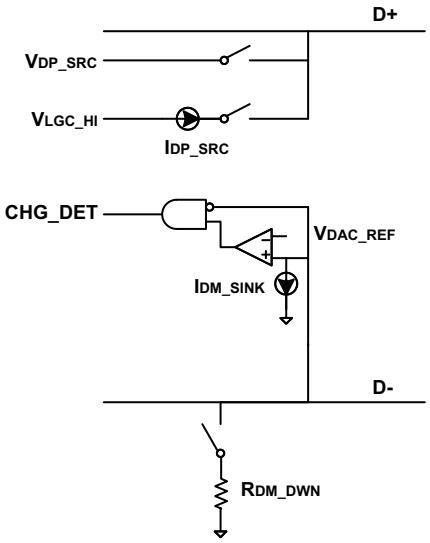


Figure 12. USB D+/D- Detection

DCD (Data Contact Detection) uses a current source to detect when the D+/D– pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and REG08[2] = 1 (power good)
- Turn on D+ I_{DP_SRC} and the D– pull-down resistor R_{DM_DWN} for 40 ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec.
- Turn off I_{DP_SRC} and disconnect R_{DM_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V_{DP_SRC} on D+ and I_{DM_SINK} on D– for 40 ms
- If PD is attached to a USB host (SDP), the D– is low. If PD is attached to a charging port (CDP or DCP), the D– is high
- Turn off V_{DP_SRC} and I_{DM_SINK}

Table 2 shows the input current limit setting after D+/D– detection.

Table 2. bq24295 USB D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT	REG08[7:6]
0.5 sec timer expired in DCD (D+/D- floating)	Proceed to non-standard adapter detection	00
USB host	500 mA	01
Charging port	3 A	10

When DCD 0.5 sec timer expires, the non-standard adapter detection is used to distinguish three different divider bias conditions on D+/D- pins. When non-standard adapter is detected, the input current limit (REG0[2:0]) is set based on the table shown below and REG08[7:6] is set to 10 (Adapter port). If non-standard adapter is not detected, REG08[7:6] is set to 00 (Unknown) and the input current limit is set in REG0[2:0] to 500mA by default.

Table 3. bq24295 Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	$V_{adpt1\_lo} < V_{D+} < V_{adpt1\_hi}$ For VBUS = 5 V, typical range 2.4 V < V_{D+} < 3.1 V	$V_{D-} < V_{adpt1\_lo}$ or $V_{D-} > V_{adpt1\_hi}$ For VBUS = 5 V, typical range V_{D-} < 2.4 V or V_{D-} > 3.1 V	2.0 A
Divider 2	$V_{adpt2\_lo} < V_{D+} < V_{adpt2\_hi}$ For VBUS = 5 V, typical range 0.85 V < V_{D+} < 1.5 V	NA	2.0 A
Divider 3	$V_{D+} < V_{adpt3\_lo}$ or $V_{D+} > V_{adpt3\_hi}$ For VBUS = 5 V, typical range V_{D+} < 2.4 V or V_{D+} > 3.1 V	$V_{adpt3\_lo} < V_{D-} < V_{adpt3\_hi}$ For VBUS = 5 V, typical range 2.4 V < V_{D-} < 3.1 V	1 A

After D+/D- detection is completed with an input source already plugged in, the input current limit is not changed unless DPDM_EN (REG07[7]) bit is set to force detection.

8.3.1.4.5 Force Input Current Limit Detection

While adapter is plugged-in, the host can force the charger device to run input current limit detection by setting REG07[7] = 1 or when watchdog timeout. During the forced detection, the input current limit is set to 100 mA. After the detection is completed, REG07[7] will return to 0 by itself and new input current limit is set based on D+/D-.

8.3.1.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when ramp up the system rail. When the system rail is below 2.2 V, the input current limit is forced to 100mA. After the system rises above 2.2 V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

As a battery charger, the charger deploys a 1.5-MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.3.1.6 Low Power HIZ State

The host can configure the converter to go into HIZ State by setting EN_HIZ (REG00[7]) to 0. The device is in the lowest quiescent state with REGN LDO and the bias circuits off, the VBUS current during HIZ state will be less than 30 µA while the system is supplied by the battery. Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7] = 0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.

8.3.2 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.2.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150 mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

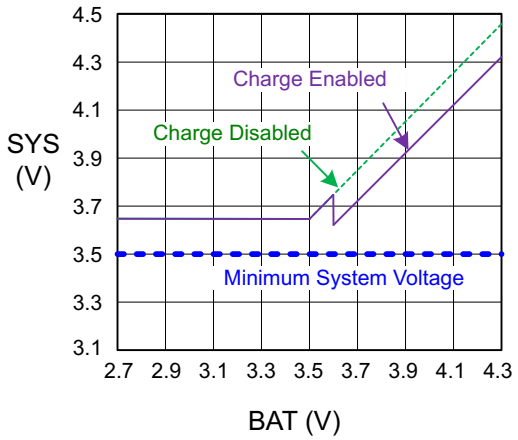


Figure 13. V(SYS) vs V(BAT)

8.3.2.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

Figure 14 shows the DPM response with 5-V/1.2-A adapter, 3.2-V battery, 2.0-A charge current and 3.4-V minimum system voltage setting.

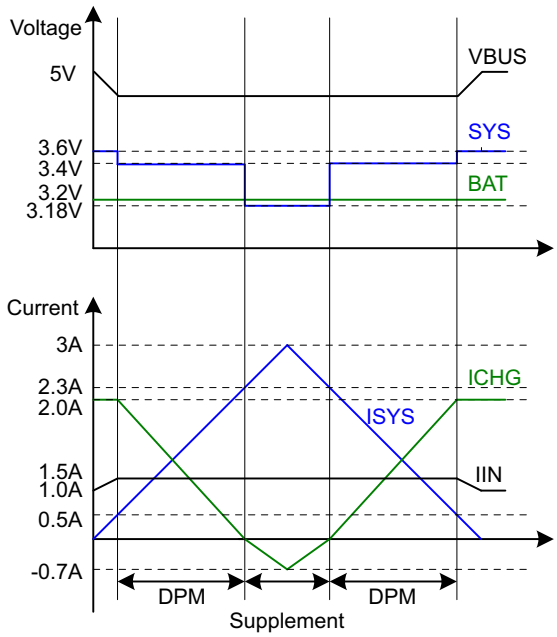


Figure 14. DPM Response

8.3.2.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

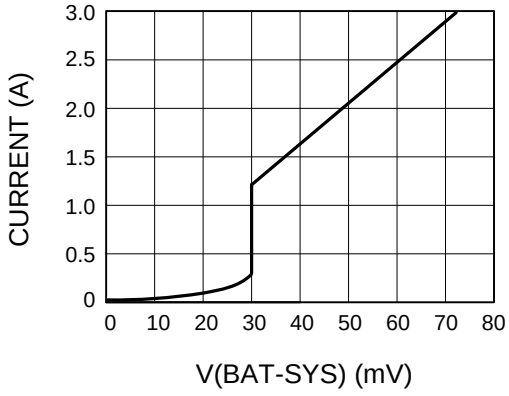


Figure 15. BATFET V-I Curve

8.3.3 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3-A charge current for high capacity tablet battery. The 24-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

8.3.3.1 Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4] = 01), the charger device complete a charging cycle without host involvement. The device default charging parameters are listed in the following table.

Table 4. Charging Parameter Default Setting

DEFAULT MODE	bq24295
Charging voltage	4.208 V
Charging current	1.024 A
Pre-charge current	256 mA
Termination current	256 mA
Temperature profile	Hot/Cold
Safety timer	12 hours(1)

(1) See *Charging Safety Timer* for more information.

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by I^2C register bit (REG01[5:4]) = 01 and $\overline{CE}$ is low
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the device automatically starts another charging cycle. After the charge done, either toggle $\overline{CE}$ pin or REG01[5:4] will initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

8.3.3.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

Table 5. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
$V_{BAT} < V_{SHORT}$ (Typical 2 V)	100 mA	–	01
$V_{SHORT} \le V_{BAT} < V_{BATLOWV}$ (Typical 2 V ≤ V_{BAT} < 3 V)	REG03[7:4]	256 mA	01
$V_{BAT} \ge V_{BATLOWV}$ (Typical V_{BAT} ≥ 3 V)	REG02[7:2]	1024 mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

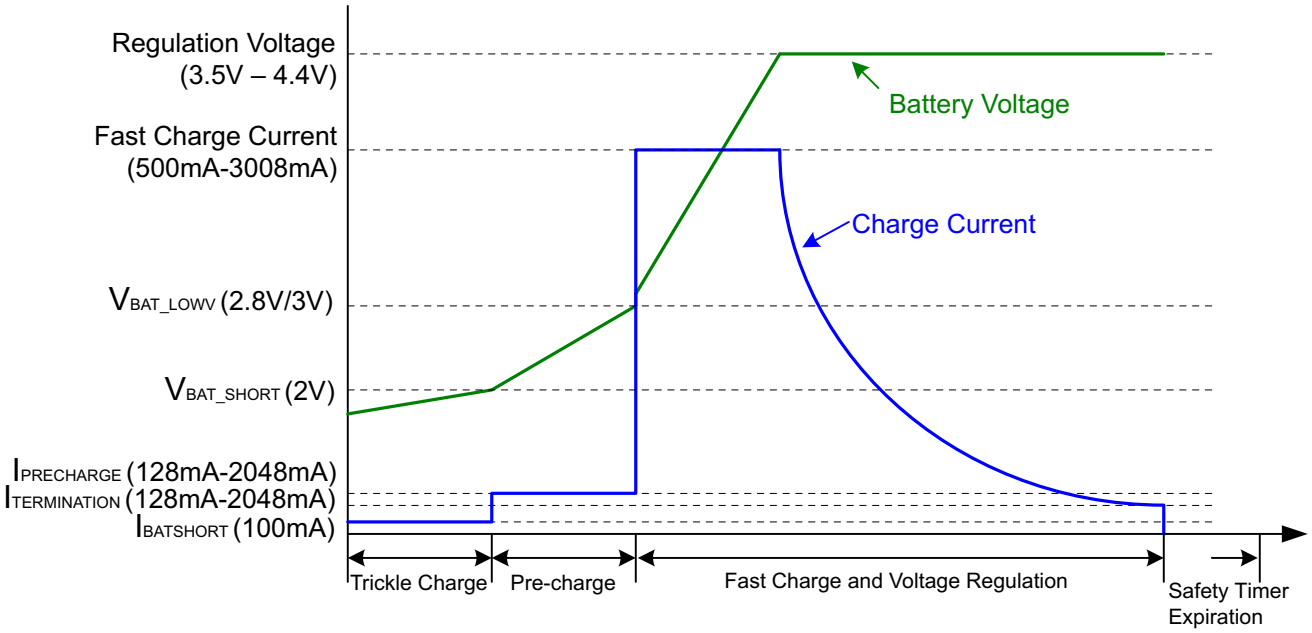


Figure 16. Battery Charging Profile

8.3.3.3 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

8.3.3.3.1 Cold/Hot Temperature Window

The device continuously monitors battery temperature by measuring the voltage between the TS pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charge or boost is allowed.

To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLDx to VBHOTx thresholds unless boost mode temperature is disabled by setting BHOT bits (REG06[3:2]) to 11. When temperature is outside of the temperature thresholds, the boost mode and BATFET are disabled and BATFET_Disable bit is set (REG07[5] bit) to reduce leakage current on PMID. Once temperature returns within thresholds, the host can clear BATFET_Disable bit (REG07[5]) or provide logic low to high transition on QON pin to enable BATFET and boost mode.

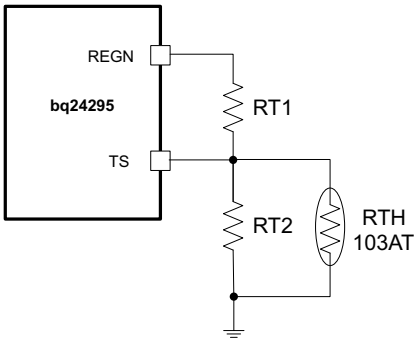


Figure 17. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

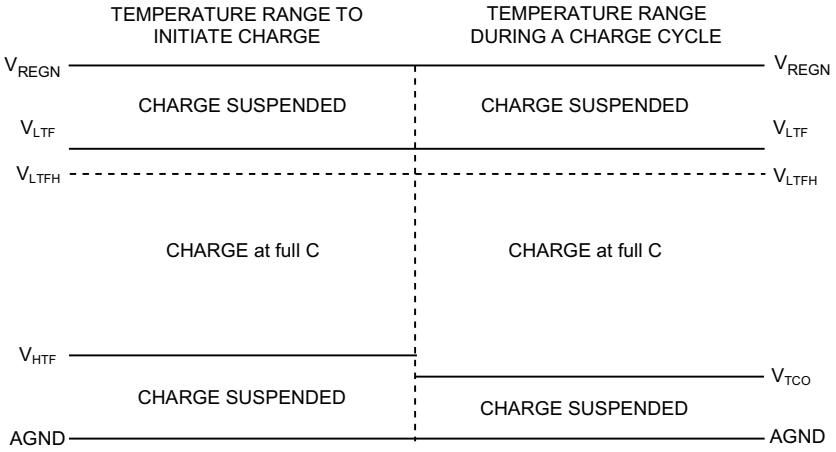


Figure 18. TS Pin Thermistor Sense Thresholds in Charge Mode

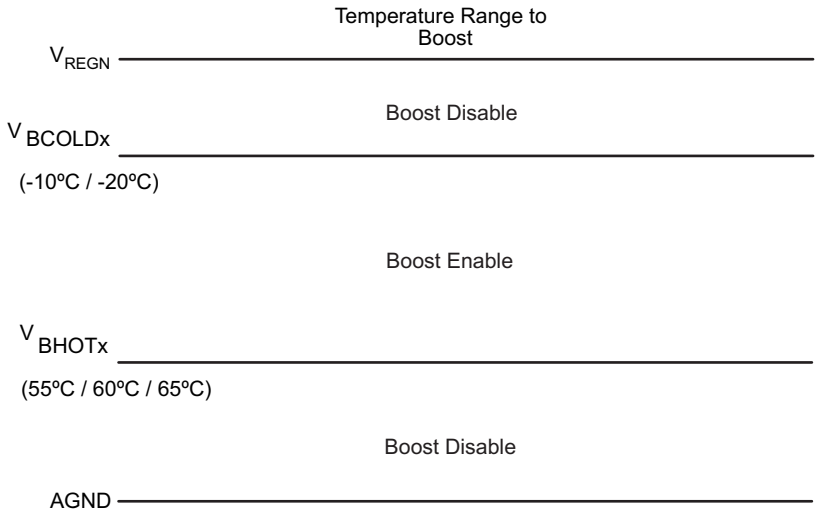


Figure 19. TS Pin Thermistor Sense Thresholds in Boost Mode

Assuming a 103AT NTC thermistor is used on the battery pack Figure 18, the value RT1 and RT2 can be determined by using the following equation:

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{V_{LTF}} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (1)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.25 kΩ
RT2 = 31.23 kΩ

8.3.3.4 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

8.3.3.4.1 Termination When REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through $\overline{CE}$ pin or REG01[5:4].

8.3.3.5 Charging Safety Timer

The device has safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below batlowv threshold. The user can program fast charge safety timer (default 12 hours) through I^2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I^2C (REG05[3]).

The following actions restart the safety timer after safety timer expires:

- Toggle the $\overline{CE}$ pin HIGH to LOW to HIGH (charge enable)
- Write REG01[5:4] from 00 to 01 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)

During input voltage/current regulation, thermal regulation, or FORCE_20PCT bit (REG02[0]) is set , the safety timer counting at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

8.3.3.5.1 Safety Timer Configuration Change

When safety timer value needs to be changed, it is recommended that the timer is disabled first before new configuration is written to REG05[2:1]. The safety timer can be disable by writing 1 to REG05[3]. This ensures the safety timer restart counting after new value is configured.

8.3.4 Status Outputs (STAT, and INT)

8.3.4.1 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

Table 6. STAT Pin State

CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH

8.3.4.2 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate a 256-µs INT pulse.

1. USB/adapter source identified (through DPDM detection)
2. Good input source detected
   - not in sleep
   - VBUS below V_{ACOV} threshold
   - current limit above I_{BADSRC}
3. Input removed or VBUS above V_{ACOV} threshold
4. Charge Complete
5. Any FAULT event in REG09

For the first four events, INT pulse is always generated. For the last event, when a fault occurs, the charger device sends out INT and latches the fault state in REG09 until the host reads the fault register. If a prior fault exists, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last read and the 2nd reads the current fault register status.

8.3.5 Protections

8.3.5.1 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times K_{LIM} \quad (2)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3 A, and ILIM has a 316-Ω resistor to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1 V. If ILIM voltage exceeds 1 V, the device enters input current regulation (Refer to *Dynamic Power Path Management* section).

The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following Equation 3:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (3)$$

For example, if ILIM pin sets 2 A, and the ILIM voltage is 0.75 V, the actual input current 1.5 A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1 V. If ILIM pin is short, the input current limit is set by the register.

8.3.5.2 Thermal Regulation and Thermal Shutdown

During charge operation, the device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

8.3.5.3 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck mode operation.

8.3.5.3.1 Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

8.3.5.3.2 System Over-Voltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

8.3.5.4 Current Monitoring in Boost Mode

The bq24295 closely monitors LSFET current to ensure safe boost mode operation.

8.3.5.5 Battery Protection

8.3.5.5.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at V_{BAT_OVP} (4% nominal) above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[3] goes high and an INT is asserted to the host.

8.3.5.5.2 Battery Short Protection

If the battery voltage falls below V_{short} (2V typical), the device immediately turns off BATFET to disable the battery charging or supplement mode. 1ms later, the BATFET turns on and charge the battery with 100-mA current. The device does not turn on BATFET to discharge a battery that is below 2.5 V.

8.3.5.5.3 System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the device latches off BATFET. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The device is a host controlled device, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings. The device keeps charging the battery by default with 12-hour fast charging safety timer. At the end of the 12 hours, the charging is stopped and the buck converter continues to operate to supply system load.

Device Functional Modes (continued)

Any write command to device transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4] = 00.

When the host changes watchdog timer configuration (REG05[5:4]), it is recommended to first disable watchdog by writing 00 to REG05[5:4] and then change the watchdog to new timer values. This ensures the watchdog timer is restarted after new value is written.

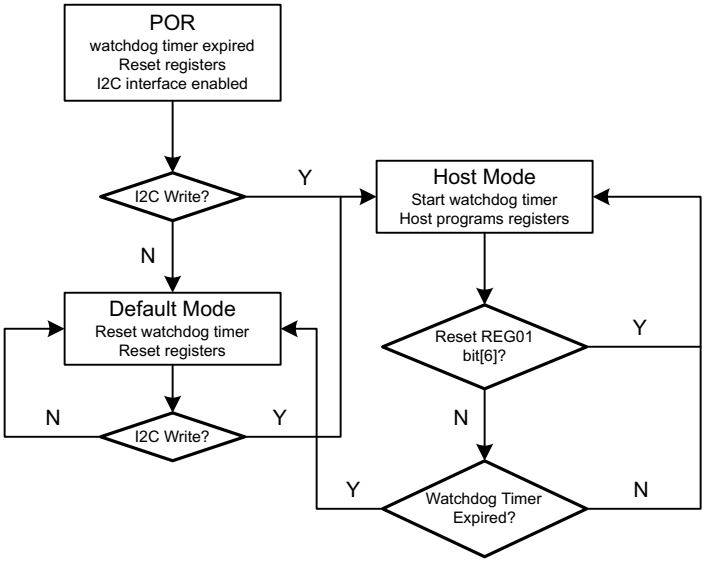


Figure 20. Watchdog Timer Flow Chart

8.5 Programming

8.5.1 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

Programming (continued)

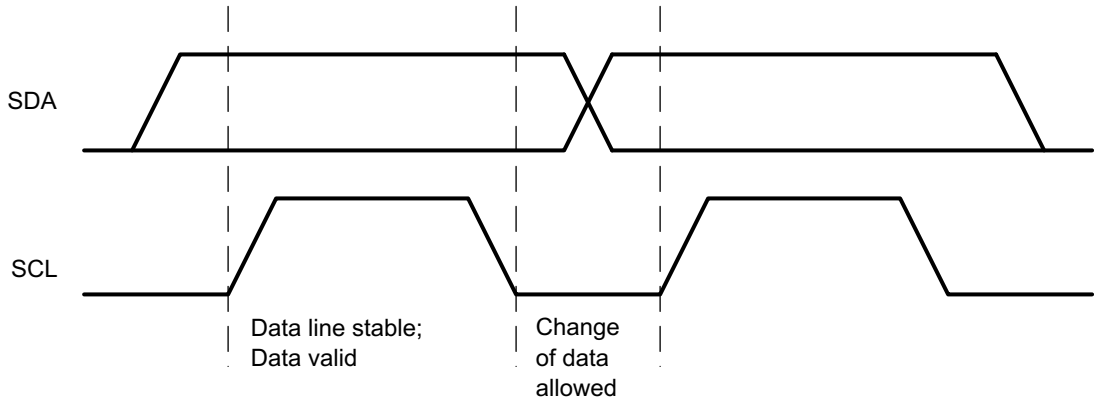


Figure 21. Bit Transfer on the I²C Bus

8.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

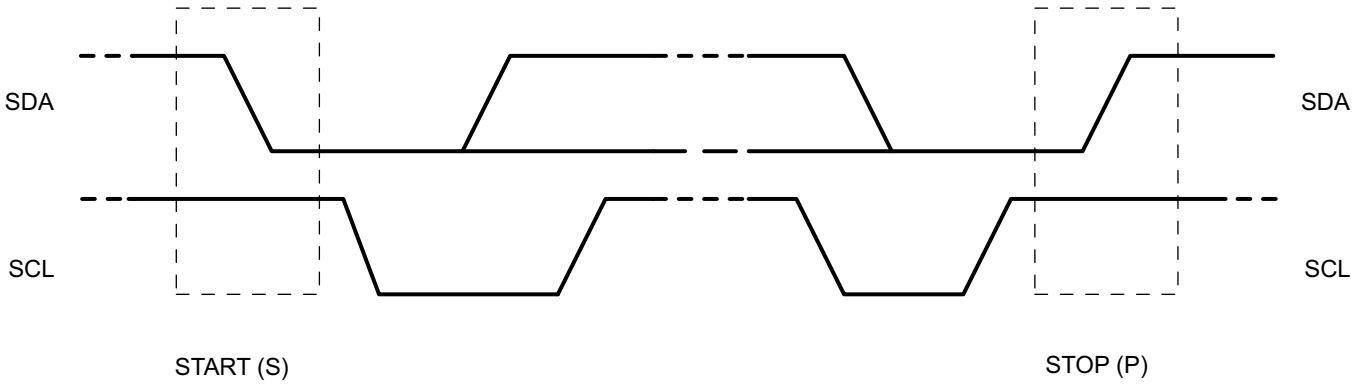


Figure 22. START and STOP Conditions

8.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

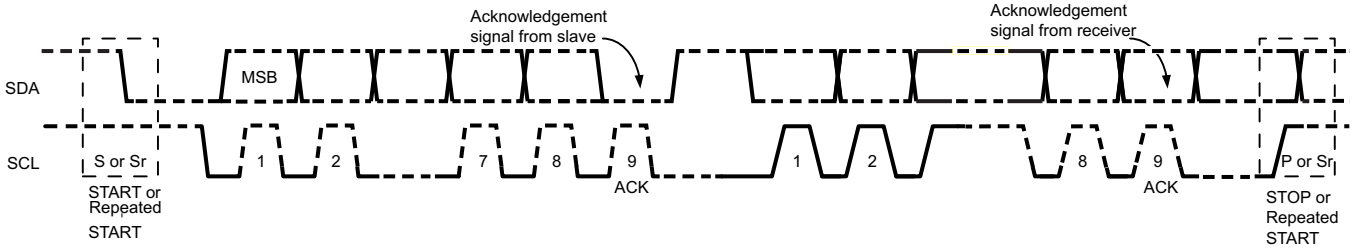


Figure 23. Data Transfer on the I²C Bus

Programming (continued)

8.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.5.1.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

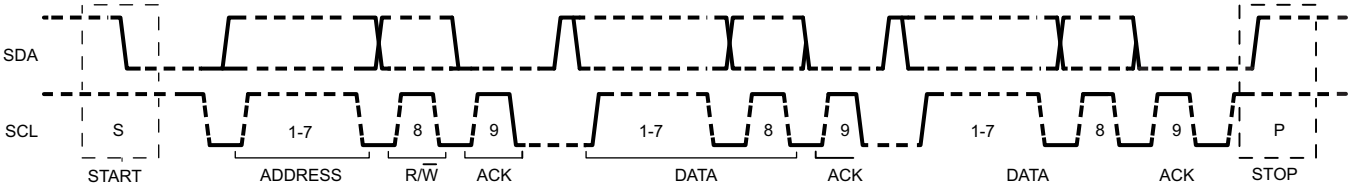


Figure 24. Complete Data Transfer

8.5.1.5.1 Single Read and Write

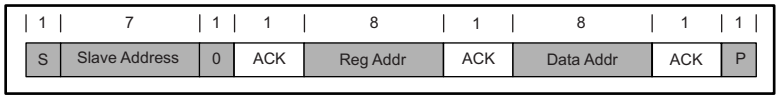


Figure 25. Single Write

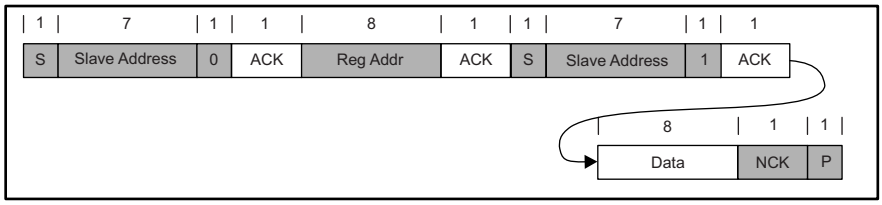


Figure 26. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.5.1.5.2 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

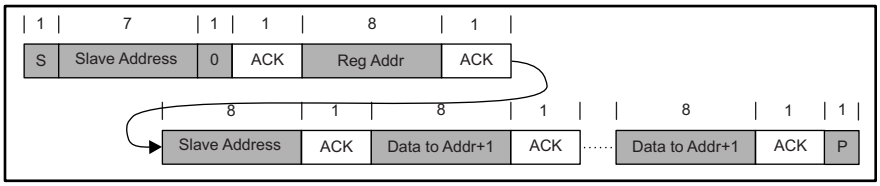


Figure 27. Multi-Write

Programming (continued)

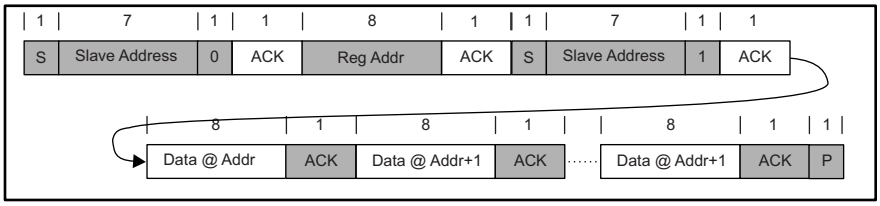


Figure 28. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if there is a TS fault but gets recovered immediately, the host still sees TS fault during the first read. In order to get the fault information at present, the host has to read REG09 for the second time. REG09 does not support multi-read and multi-write.

8.6 Register Map

8.6.1 I²C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are Read only.

8.6.1.1 Input Source Control Register REG00 [reset = 01011000, or 0x58]

Figure 29. Input Source Control Register REG00 Format

7	6	5	4	3	2	1	0
EN_HIZ	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]	IINLIM[2]	IINLIM[1]	IINLIM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 7. Input Source Control Register REG00 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	EN_HIZ	R/W	0	0 – Disable, 1 – Enable	Default: Disable (0)
Input Voltage Limit					
Bit 6	VINDPM[3]	R/W	1	640 mV	Offset 3.88 V, Range: 3.88 V – 5.08 V Default: 4.76 V (1011)
Bit 5	VINDPM[2]	R/W	0	320 mV	
Bit 4	VINDPM[1]	R/W	1	160 mV	
Bit 3	VINDPM[0]	R/W	1	80 mV	
Input Current Limit (Actual input current limit is the lower of I²C and ILIM)					
Bit 2	IINLIM[2]	R/W	0	000 – 100 mA, 001 – 150 mA, 010 – 500 mA, 011 – 900 mA, 100 – 1 A, 101 – 1.5 A, 110 – 2 A, 111 – 3A	Default SDP: 500 mA (010) Default DCP/CDP: 3 A (101) Default Divider 1 and 2: 2 A (110) Default Divider 3: 1 A (100)
Bit 1	IINLIM[1]	R/W	0		
Bit 0	IINLIM[0]	R/W	0		

8.6.1.2 Power-On Configuration Register REG01 [reset = 00111011, or 0x3B]

Figure 30. Power-On Configuration Register REG01 Format

7	6	5	4	3	2	1	0
Register Reset	I^2C Watchdog Timer Reset	OTG_CONFIG	CHG_CONFIG	SYS_MIN[2]	SYS_MIN[1]	SYS_MIN[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 8. Power-On Configuration Register REG01 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	Register Reset	R/W	0	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Note: Register Reset bit does not reset device to default mode
Bit 6	I^2C Watchdog Timer Reset	R/W	0	0 – Normal ; 1 – Reset	Default: Normal (0) Note: Consecutive I^2C watchdog timer reset requires minimum 20-µs delay
Charger Configuration					
Bit 5	OTG_CONFIG	R/W	1	0 – OTG Disable; 1 – OTG Enable	Default: OTG Enable (1) Note: OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG
Bit 4	CHG_CONFIG	R/W	1	0- Charge Disable; 1- Charge Enable	Default: Charge Battery (1)
Minimum System Voltage Limit					
Bit 3	SYS_MIN[2]	R/W	1	0.4 V	Offset: 3.0 V, Range 3.0 V – 3.7 V Default: 3.5 V (101)
Bit 2	SYS_MIN[1]	R/W	0	0.2 V	
Bit 1	SYS_MIN[0]	R/W	1	0.1 V	
Bit 0	Reserved	R/W	1	1 - Reserved	

8.6.1.3 Charge Current Control Register REG02 [reset = 00100000, or 0x20]

Figure 31. Charge Current Control Register REG02 Format

7	6	5	4	3	2	1	0
ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]	BCOLD	FORCE_20PCT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 9. Charge Current Control Register REG02 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Fast Charge Current Limit					
Bit 7	ICHG[5]	R/W	0	2048 mA	Offset: 512 mA Range: 512 – 3008 mA (000000 – 100111) Default: 1024mA (001000) Note: ICHG higher than 3008mA is not supported
Bit 6	ICHG[4]	R/W	0	1024 mA	
Bit 5	ICHG[3]	R/W	1	512 mA	
Bit 4	ICHG[2]	R/W	0	256 mA	
Bit 3	ICHG[1]	R/W	0	128 mA	
Bit 2	ICHG[0]	R/W	0	64 mA	
Bit 1	BCOLD	R/W	0	Set Boost Mode temperature monitor threshold voltage to disable boost mode 0 – V_{bcold0} (Typ. 76% of REGN or -10°C w/ 103AT thermistor) 1 – V_{bcold1} (Typ. 79% of REGN or -20°C w/ 103AT thermistor)	Default: V_{bcold0} (0)
Bit 0	FORCE_20PCT	R/W	0	0 – ICHG as Fast Charge Current (REG02[7:2]) and IPRECH as Pre-Charge Current (REG03[7:4]) programmed 1 – ICHG as 20% Fast Charge Current (REG02[7:2]) and IPRECH as 50% Pre-Charge Current (REG03[7:4]) programmed	Default: ICHG as Fast Charge Current (REG02[7:2]) and IPRECH as Pre-Charge Current (REG03[7:4]) programmed (0)

8.6.1.4 Pre-Charge/Termination Current Control Register REG03 [reset = 00010001, or 0x11]

Figure 32. Pre-Charge/Termination Current Control Register REG03 Format

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 10. Pre-Charge/Termination Current Control Register REG03 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Pre-Charge Current Limit					
Bit 7	IPRECHG[3]	R/W	0	1024 mA	Offset: 128 mA, Range: 128 mA – 2048 mA Default: 256 mA (0001)
Bit 6	IPRECHG[2]	R/W	0	512 mA	
Bit 5	IPRECHG[1]	R/W	0	256 mA	
Bit 4	IPRECHG[0]	R/W	1	128 mA	
Termination Current Limit					
Bit 3	ITERM[3]	R/W	0	1024 mA	Offset: 128 mA Range: 128 mA – 2048 mA Default: 256 mA (0001)
Bit 2	ITERM[2]	R/W	0	512 mA	
Bit 1	ITERM[1]	R/W	0	256 mA	
Bit 0	ITERM[0]	R/W	1	128 mA	

8.6.1.5 Charge Voltage Control Register REG04 [reset = 10110010, or 0xB2]

Figure 33. Charge Voltage Control Register REG04 Format

7	6	5	4	3	2	1	0
VREG[5]	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	BATLOWV	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 11. Charge Voltage Control Register REG04 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charge Voltage Limit					
Bit 7	VREG[5]	R/W	1	512 mV	Offset: 3.504 V Range: 3.504 V – 4.400 V Default: 4.208 V (101100)
Bit 6	VREG[4]	R/W	0	256 mV	
Bit 5	VREG[3]	R/W	1	128 mV	
Bit 4	VREG[2]	R/W	1	64 mV	
Bit 3	VREG[1]	R/W	0	32 mV	
Bit 2	VREG[0]	R/W	0	16 mV	
Bit 1	BATLOWV	R/W	1	0 – 2.8 V, 1 – 3.0 V	Default: 3.0 V (1) (pre-charge to fast charge)
Battery Recharge Threshold (below battery regulation voltage)					
Bit 0	VRECHG	R/W	0	0 – 100 mV, 1 – 300 mV	Default: 100 mV (0)

8.6.1.6 Charge Termination/Timer Control Register REG05 [reset = 10011100, or 0x9C]

Figure 34. Charge Termination/Timer Control Register REG05 Format

7	6	5	4	3	2	1	0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER[1]	CHG_TIMER[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 12. Charge Termination/Timer Control Register REG05 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charging Termination Enable					
Bit 7	EN_TERM	R/W	1	0 – Disable, 1 – Enable	Default: Enable termination (1)
Bit 6	Reserved	R/W	0	0 - Reserved	
I2C Watchdog Timer Setting					
Bit 5	WATCHDOG[1]	R/W	0	00 – Disable timer, 01 – 40 s, 10 – 80 s, 11 – 160 s	Default: 40 s (01)
Bit 4	WATCHDOG[0]	R/W	1		
Charging Safety Timer Enable					
Bit 3	EN_TIMER	R/W	1	0 – Disable, 1 – Enable	Default: Enable (1)
Fast Charge Timer Setting					
Bit 2	CHG_TIMER[1]	R/W	1	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 12 hrs (10) (See *Charging Safety Timer* for details)
Bit 1	CHG_TIMER[0]	R/W	0		
Bit 0	Reserved	R/W	0	0 - Reserved	

8.6.1.7 Boost Voltage/Thermal Regulation Control Register REG06 [reset = 10010011, or 0x93]

Figure 35. Boost Voltage/Thermal Regulation Control Register REG06 Format

7	6	5	4	3	2	1	0
BOOSTV[3]	BOOSTV[2]	BOOSTV[1]	BOOSTV[0]	BHOT[1]	BHOT[0]	TREG[1]	TREG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 13. Boost Voltage/Thermal Regulation Control Register REG06 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	BOOSTV[3]	R/W	1	512 mV	Offset: 4.55 V Range: 4.55 V – 5.51 V Default:5.126 V (1001)
Bit 6	BOOSTV[2]	R/W	0	256 mV	
Bit 5	BOOSTV[1]	R/W	0	128 mV	
Bit 4	BOOSTV[0]	R/W	1	64 mV	
Bit 3	BHOT[1]	R/W	0	Set Boost Mode temperature monitor threshold voltage to disable boost mode Voltage to disable boost mode 00 – V_{bhot1} (33% of REGN or 55°C w/ 103AT thermistor) 01 – V_{bhot0} (36% of REGN or 60°C w/ 103AT thermistor) 10 – V_{bhot2} (30% of REGN or 65°C w/ 103AT thermistor) 11 – Disable boost mode thermal protection.	Default: V_{bhot1} (00) Note: For BHOT[1:0] = 11, boost mode operates without temperature monitor and the NTC_FAULT is generated based on V_{bhot1} threshold
Bit 2	BHOT[0]	R/W	0		
Thermal Regulation Threshold					
Bit 1	TREG[1]	R/W	1	00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C	Default: 120°C (11)
Bit 0	TREG[0]	R/W	1		

8.6.1.8 Misc Operation Control Register REG07 [reset = 01001011, or 0x4B]

Figure 36. Misc Operation Control Register REG07 Format

7	6	5	4	3	2	1	0
DPDM_EN	TMR2X_EN	BATFET_Disable	Reserved	Reserved	Reserved	INT_MASK[1]	INT_MASK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 14. Misc Operation Control Register REG07 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Force DPDM detection					
Bit 7	DPDM_EN	R/W	0	0 – Not in input source detection; 1 – Force input source detection when VBUS power is presence	Default: Not in input source detection (0), Back to 0 after detection complete
Safety Timer Setting during Input DPM and Thermal Regulation					
Bit 6	TMR2X_EN	R/W	1	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
Force BATFET Off					
Bit 5	BATFET_Disable	R/W	0	0 – Allow BATFET (Q4) turn on, 1 – Turn off BATFET (Q4)	Default: Allow BATFET (Q4) turn on(0)
Bit 4	Reserved	R/W	0	0 - Reserved	
Bit 3	Reserved	R/W	1	1 - Reserved	
Bit 2	Reserved	R/W	0	0 - Reserved	
Bit 1	INT_MASK[1]	R/W	1	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	R/W	1	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

8.6.1.9 System Status Register REG08

Figure 37. System Status Register REG08 Format

7	6	5	4	3	2	1	0
VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	DPM_STAT	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 15. System Status Register REG08 Field Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	VBUS_STAT[1]	R	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	R	
Bit 5	CHRG_STAT[1]	R	00 – Not Charging, 01 – Pre-charge (<$V_{BATLOWV}$), 10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	R	
Bit 3	DPM_STAT	R	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	R	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	R	0 – Normal, 1 – In Thermal Regulation
Bit 0	VSYS_STAT	R	0 – Not in VSYSMIN regulation (BAT > VSYSMIN), 1 – In VSYSMIN regulation (BAT < VSYSMIN)

8.6.1.10 New Fault Register REG09

Figure 38. New Fault Register REG09 Format

7	6	5	4	3	2	1	0
WATCHDOG_FAULT	OTG_FAULT	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	Reserved	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 16. New Fault Register REG09 Field Description(1)(2)(3)

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	WATCHDOG_FAULT	R	0 – Normal, 1- Watchdog timer expiration
Bit 6	OTG_FAULT	R	0 – Normal, 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that cannot start boost function)
Bit 5	CHRG_FAULT[1]	R	00 – Normal, 01 – Input fault (OVP or bad source), 10 - Thermal shutdown, 11 – Charge Timer Expiration
Bit 4	CHRG_FAULT[0]	R	
Bit 3	BAT_FAULT	R	0 – Normal, 1 – Battery OVP
Bit 2	Reserved	R	Reserved – 0
Bit 1	NTC_FAULT[1]	R	0-Normal 1–Cold Note: Cold temperature threshold is different based on device operates in buck or boost mode
Bit 0	NTC_FAULT[0]	R	0-Normal 1–Hot Note: Hot temperature threshold is different based on device operates in buck or boost mode

(1) REG09 only supports single byte I^2C read.
(2) All register bits in REG09 are latched fault. First time read of REG09 clears the previous fault and second read updates fault register to any fault that still presents.
(3) When adapter is unplugged, input fault (bad source) in CHRG_FAULT bits[5:4] is set to 01 once.

8.6.1.11 Vender / Part / Revision Status Register REG0A

Figure 39. Vender / Part / Revision Status Register REG0A Format

7	6	5	4	3	2	1	0
PN[2]	PN[1]	PN[0]	Reserved	Reserved	Rev[2]	Rev[1]	Rev[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 17. Vender / Part / Revision Status Register REG0A Field Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	PN[2]	R	110 (bq24295)
Bit 6	PN[1]	R	
Bit 5	PN[0]	R	
Bit 4	Reserved	R	0 – Reserved
Bit 3	Reserved	R	0 – Reserved
Bit 2	Rev[2]	R	000
Bit 1	Rev[1]	R	
Bit 0	Rev[0]	R	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a single cell Li-Ion battery charger for single cell Li-Ion and Li-polymer batteries used in a wide range of tablets and other portable devices. It integrates an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application

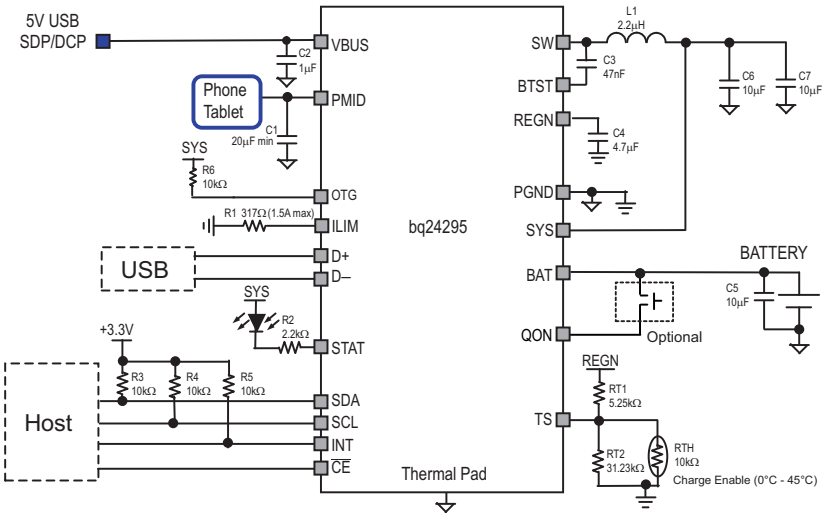


Figure 40. bq24295 with USB D+/D- Detection for Charging and Discharging in Boost Mode

9.2.1 Design Requirements

Table 18. Design Requirements

DESIGN PARAMATER	EXAMPLE VALUE
Input voltage range	3.9 V to 6.2 V
Input current limit	3000 mA
Fast charge current	3000 mA
Boost mode output current	1.5 A

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5-MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (VBUS), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (6)$$

For best performance, VBUS should be decouple to PGND with 1-μF capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for 15-V input voltage. 22-μF capacitance is suggested for typical of 3-A to 4-A charging current.

9.2.2.3 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

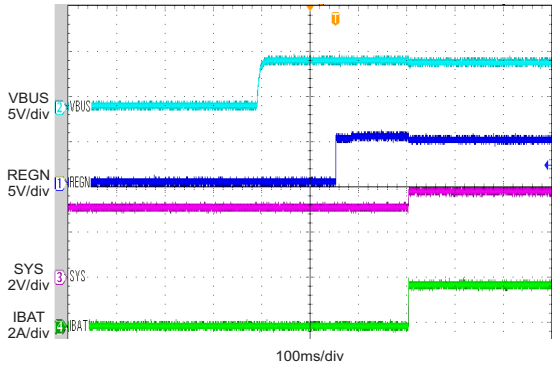
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

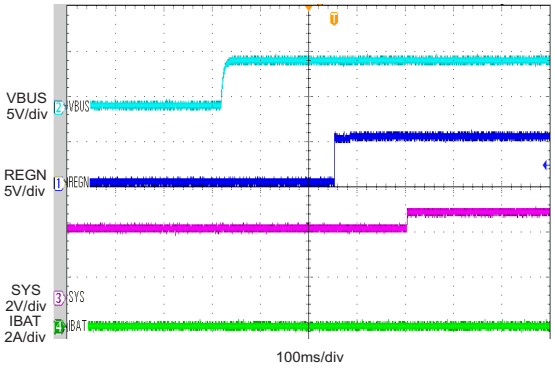
The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 36 kHz. The preferred ceramic capacitor is 6 V or higher rating, X7R or X5R.

9.2.3 Application Performance Plots



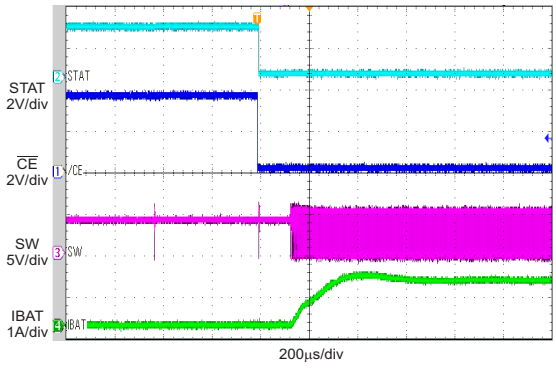
VBAT = 3.2 V

Figure 41. Power Up with Charge Enabled



VBAT = 3.2 V

Figure 42. Power Up with Charge Disabled



VBAT = 5 V

Figure 43. Charge Enable

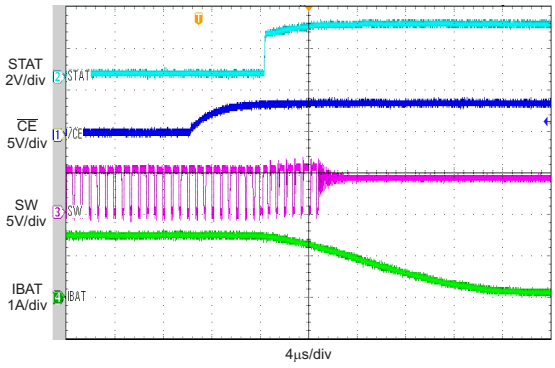
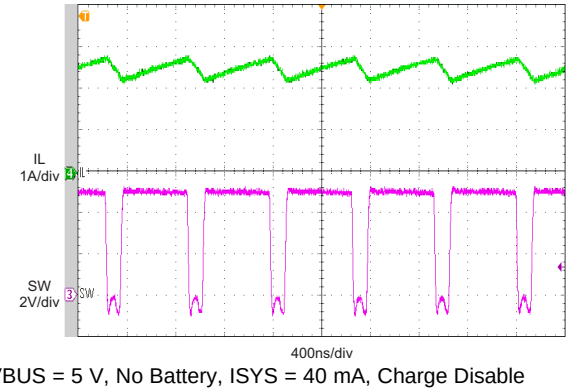
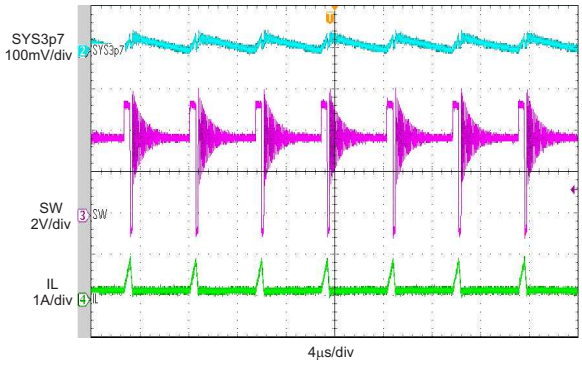


Figure 44. Charge Disable



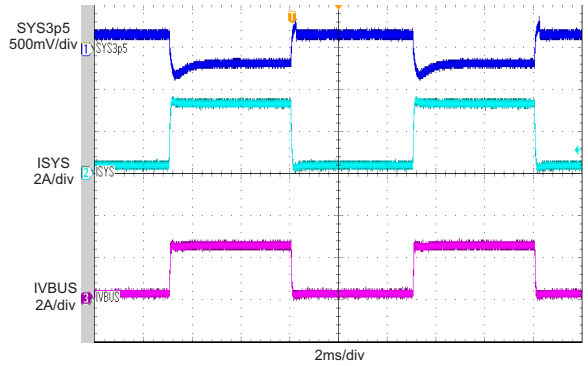
VBUS = 5 V, No Battery, ISYS = 40 mA, Charge Disable

Figure 45. PWM Switching in Buck Mode



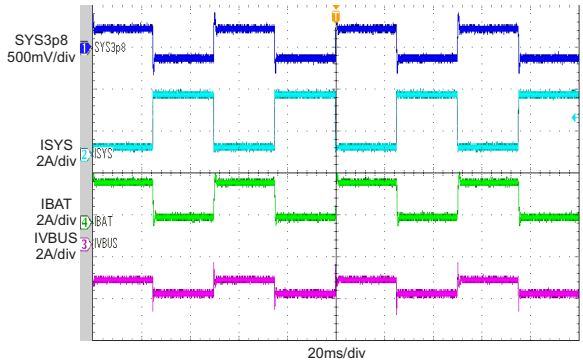
VBUS = 5 V, VBAT = 3.6 V, ICHG = 2.5 A

Figure 46. PFM Switching in Buck Mode



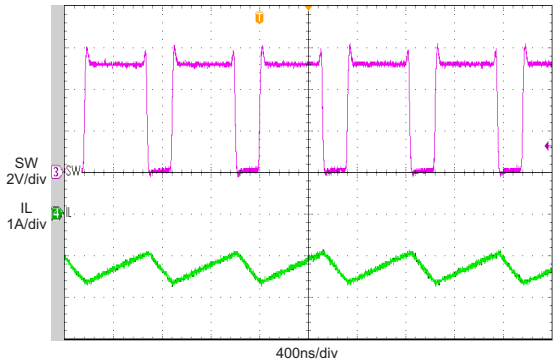
VBUS = 5 V, IIN = 3 A, No Battery, Charge Disable

Figure 47. Input Current DPM Response without Battery



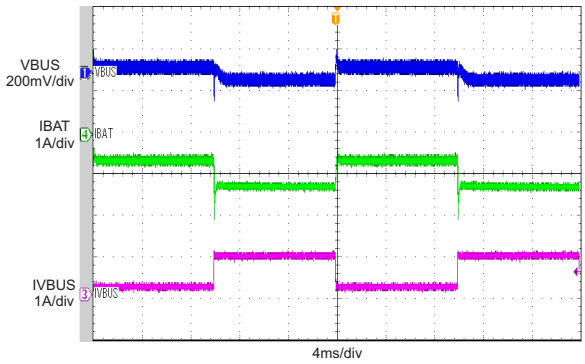
VBUS = 5 V, IIN = 1.5 A, VBAT = 3.8 V

Figure 48. Load Transient During Supplement Mode



VBAT = 3.8 V, ILOAD = 1 A

Figure 49. Boost Mode Switching



VBAT = 3.8 V

Figure 50. Boost Mode Load Transient

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the bq24295 requireS a power supply between 3.9 V and 6.2 V input with at least 100-mA current rating connected to V_{BUS}; or, a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 51) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the VQFN information, refer to SCBA017 and SLUA271.

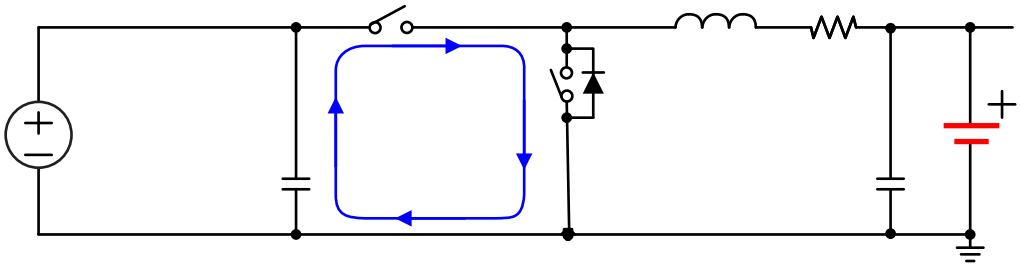


Figure 51. High Frequency Current Path

11.2 Layout Example

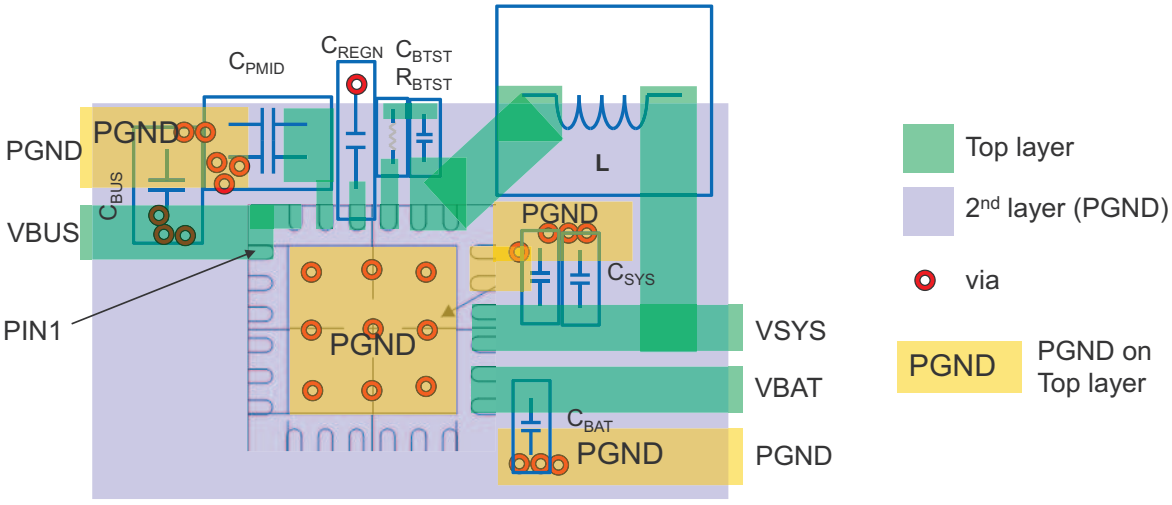


Figure 52. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

bq24296/7 EVM (PWR021) User's Guide (SLUUAQ1)

Quad Flatpack No-Lead Logic Packages Application Report (SCBA017)

QFN/SON PCB Attachment Application Report (SLUA271)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24295RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24295	Samples
BQ24295RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24295	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

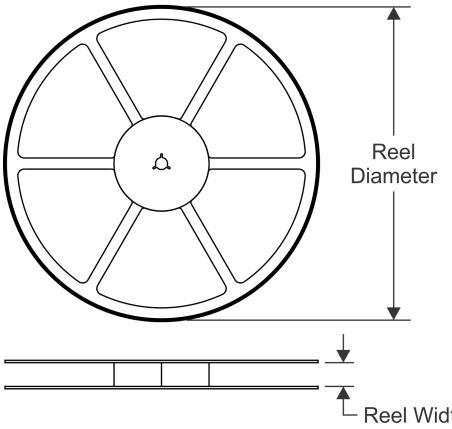
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

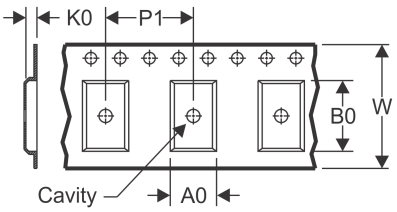
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

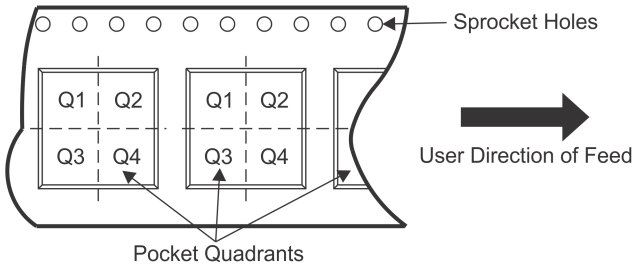


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

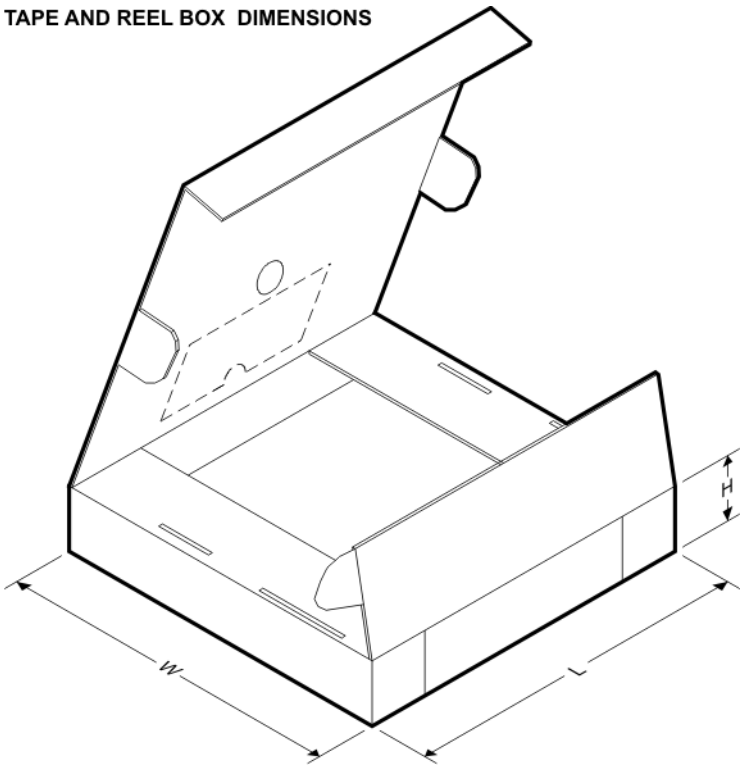
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24295RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24295RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



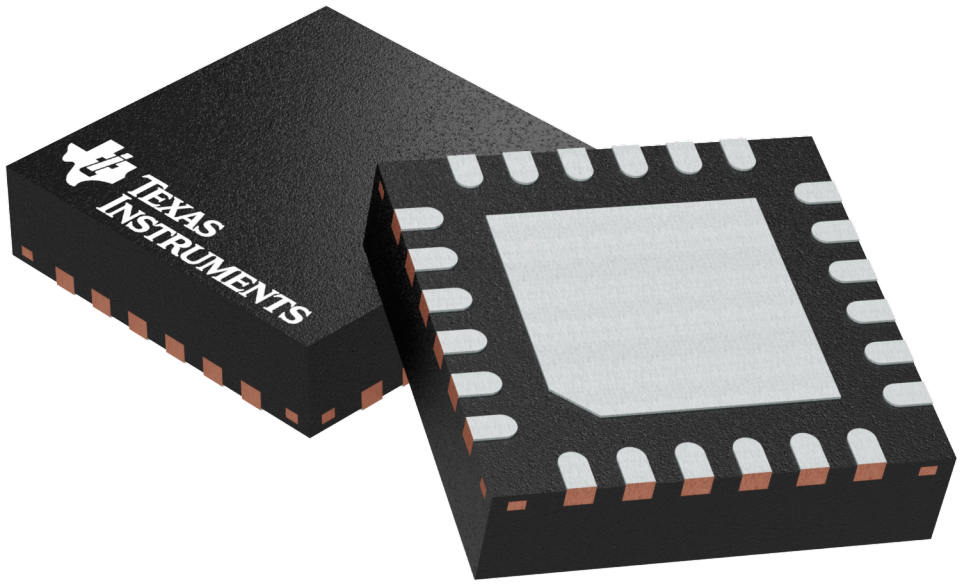
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24295RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24295RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

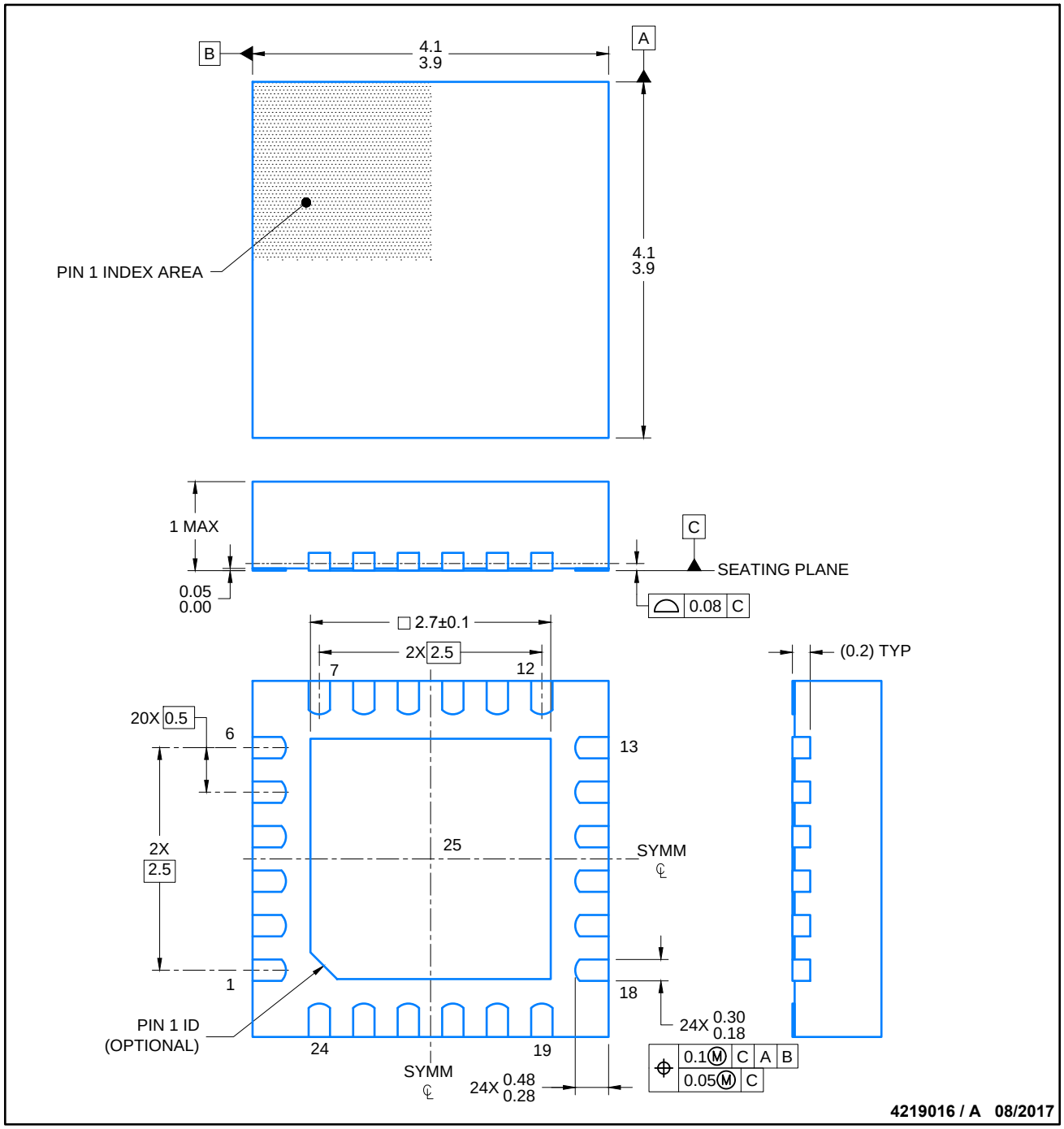
4204104/H

PACKAGE OUTLINE

RGE0024H

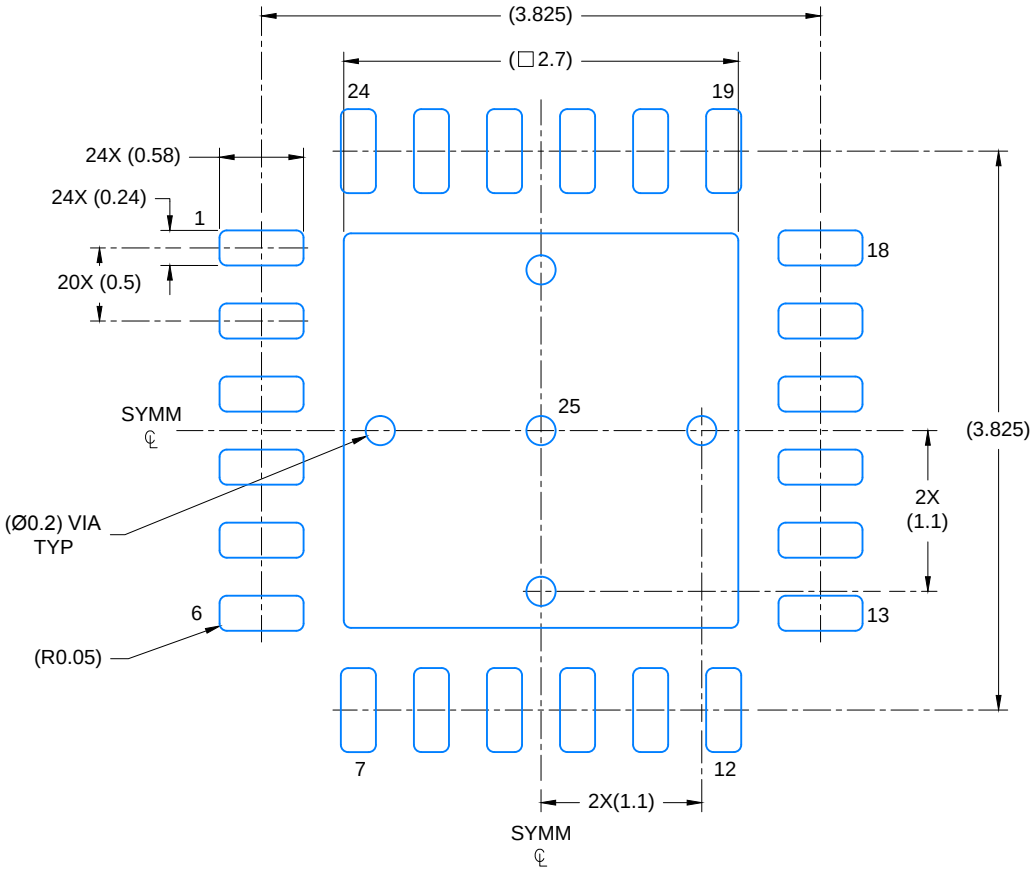
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



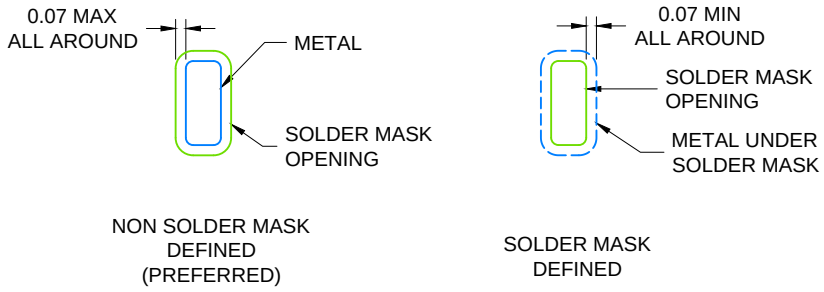
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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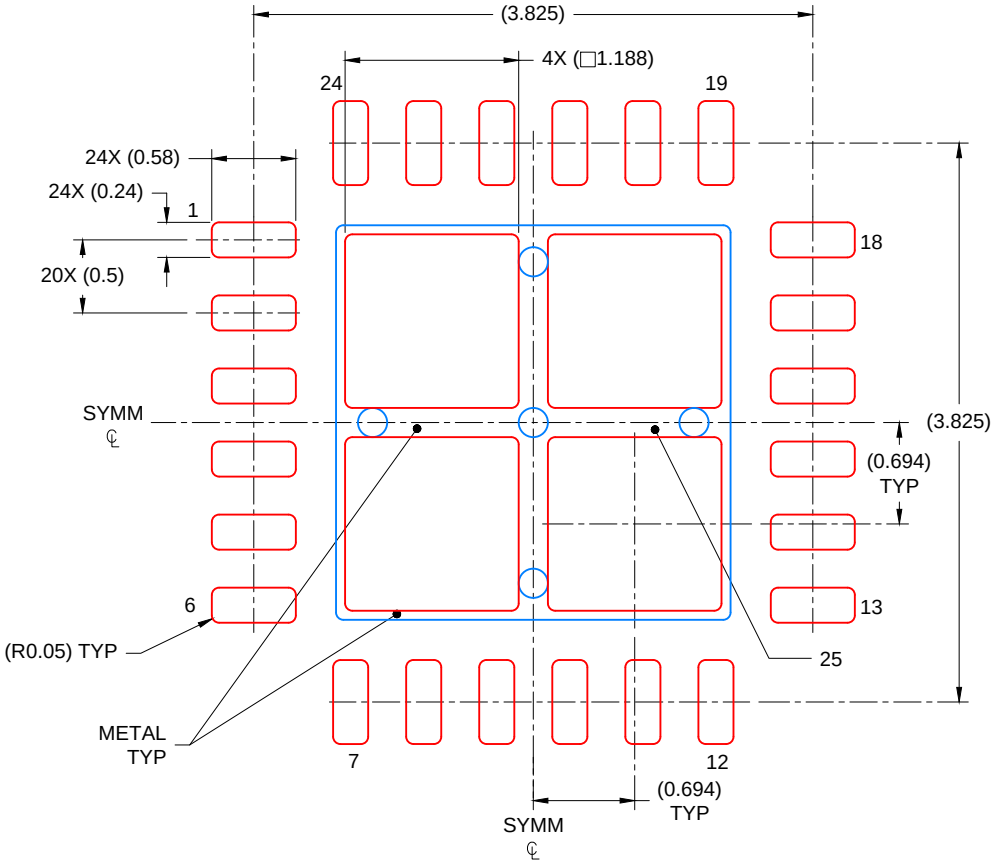
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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