INTEGRATED CHARGE CONTROLLER FOR LEAD-ACID BATTERIES

Check for Samples: bq24450

FEATURES

- **Regulates Both Voltage and Current During Charging**
- **Precision Temperature-Compensated Reference:**
  - **Maximizes Battery Capacity Over Temperature**
  - **Ensures Safety While Charging Over Temperature**
- **Optimum Control to Maximize Battery Capacity and Life**
- **Supports Different Configurations**
- **Minimum External Components**
- **Available in 16-Pin SOIC (DW)**

APPLICATIONS

- **Emergency Lighting Systems**
- **Security and Alarm Systems**
- **Telecommunication Backup Power**
- **Uninterruptible Power Supplies**

DESCRIPTION

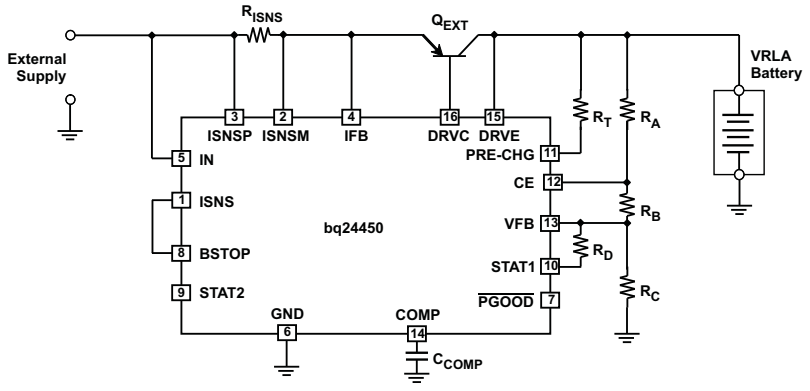
The bq24450 contains all the necessary circuitry to optimally control the charging of valve-regulated lead-acid batteries. The IC controls the charging current as well as the charging voltage to safely and efficiently charge the battery, maximizing battery capacity and life. Depending on the application, the IC can be configured as a simple constant-voltage float charge controller or a dual-voltage float-cum-boost charge controller.

The built-in precision voltage reference is especially temperature-compensated to track the characteristics of lead-acid cells, and maintains optimum charging voltage over an extended temperature range without using any external components. The ICs low current consumption allows for accurate temperature monitoring by minimizing self-heating effects.

The IC can support a wide range of battery capacities and charging currents, limited only by the selection of the external pass transistor. The versatile driver for the external pass transistor supports both NPN and PNP types and provides at least 25mA of base drive.

In addition to the voltage- and current-regulating amplifiers, the IC features comparators that monitor the charging voltage and current. These comparators feed into an internal state machine that sequences the charge cycle. Some of these comparator outputs are made available as status signals at external pins of the IC. These status and control pins can be connected to a processor, or they can be connected up in flexible ways for standalone applications.

Figure 1. TYPICAL APPLICATION SCHEMATIC



A dual-level Float-cum-Boost Charger with Pre-Charge

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

DEVICE PACKAGE	PACKING	ORDERABLE PART NUMBER	MARKING
SOIC (D)	Tube of 50	bq24450D	bq24450D
	Reel of 2500	bq24450DR	bq24450D

ABSOLUTE MAXIMUM RATINGS(1) (2) (3)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input Voltage	IN	–0.3 to 40	V
	PGOOD, STAT1, STAT2, ISNS	–0.3 to 40	V
	VFB, IFB, ISNSP, ISNSM	–0.3 to 40	V
	BSTOP	–0.3 to 40	V
Voltage	PRE-CHG (with respect to IN)	–32	V
Input Current	ISNS	80	mA
	STAT1, STAT2, PGOOD	20	mA
Output Current	PRE-CHG	–40	mA
Input Current	DRVC	80	mA
Output Current	DRVE	–80	mA
Power Dissipation at T_A = 25°C		1000	mW
Junction temperature, T_J		–40 to 150	°C
Storage temperature, T_{STG}		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminal (pin 6) unless otherwise noted.
(3) Positive currents are into, and negative currents out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	5	40	V
I_{STAT1}, I_{STAT2}, I_{PGOOD}	Input current, open-collector status pins		5	mA
I_{ISNS}	Input current, open-collector ISNS comparator output		25	mA
T_J	Junction Temperature	–40	70	°C

ELECTRICAL CHARACTERISTICS

Over junction temperature range –40°C ≤ T_J ≤ 70°C, V_{IN} = 10V, T_J = T_A. (Positive currents are into, and negative currents out of, the specified terminal)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Input power detected threshold	V_{IN} increasing from 0V to 5V	4.2	4.5	4.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{IN} decreasing from 5V to 0V		200	300	mV
I_{IN}	Operating current	V_{IN} = 10V		1.6	3.3	mA
		V_{IN} = 40V		1.8	3.6	
		V_{IN} = 40V, T_A = –40°C to 85°C		1.8	4	
INTERNAL REFERENCE (V_{REF})						
V_{REF}	Reference voltage level	Measured as regulating level on VFB pin when device is in FLOAT mode. T_J = 25°C	2.275	2.300	2.325	V
dV_{REF}/dT	Temperature coefficient of V_{REF}			–3.5		mV/°C
ΔV_{REF}	Line regulation of VREF	V_{IN} = 5V to 40V		3	8	mV
VOLTAGE AMPLIFIER						
I_{VFB}	Input bias current	V_{VFB} = 2.30V	–500	–200		nA
A_{OV}	Open-loop gain	Driver current = 1mA	50	65		dB
V_O	Output voltage swing (above GND or below V_{IN})			200		mV
CURRENT LIMIT AMPLIFIER						
I_{IFB}	Input bias current			0.2	1	µA
V_{ILIM}	Threshold voltage (wrt V_{IN})		225	250	275	mV
ΔV_{ILIM}	Sensitivity of V_{ILIM} to V_{IN}	V_{IN} = 5V to 40V		0.03	0.25	%/V
DRIVER TRANSISTOR						
V_{CE}	Minimum collector to emitter differential	V_{DRVC} = V_{IN}, I_{DRVE} = 10mA		2	2.2	V
$I_{DRVE-MAX}$	Maximum output current	V_{DRVC} – V_{DRVE} = 2 V	25	40		mA
PRE-CHG						
I_{PRE}	Maximum output current VPRE = VIN - 3V		–40	–25		mA
V_{PRE}	Maximum output voltage (V_{IN} – $V_{PRE-CHG}$)	I_{PRE} = –10mA		2	2.6	V
$V_{PRE-REV}$	PRE-CHG reverse hold-off voltage	V_{IN} = 0 V, I_{PRE} = –10µA		6.3	7	V
ENABLE COMPARATOR						
V_{TH-CE}	Threshold voltage (x V_{REF})		0.99	1.00	1.01	V/V
I_{CE}	Input bias current		–500	–200		nA
CURRENT SENSE COMPARATOR						
$I_{IB-ISNS}$	Input bias current			100	500	nA
$I_{OS-ISNS}$	Input offset current			10	200	nA
V_{ISNS}	Threshold voltage (V_{ISNSP} – V_{ISNSM})		20	25	30	mV
$\Delta V_{ISNS}/\Delta V_{IN}$	Threshold sensitivity to V_{IN}	V_{IN} = 5V to 40V		0.05	0.35	%/V
$\Delta V_{ISNS}/\Delta_{VCM}$	Threshold sensitivity to common-mode voltage	V_{CM} = 2V to VIN		0.05	0.35	%/V
I_{ISNS}	Maximum sink current, ISNS pin	V_{ISNS} = 2 V		25	40	mA
$V_{ISNS-SAT}$	Saturation voltage, ISNS pin	I_{ISNS} = 10 mA		200	450	mV
VOLTAGE SENSE COMPARATOR						
V_{VSNS}	Threshold voltage (x V_{REF})	L1 = RESET	0.94	0.95	0.96	
		L1 = SET	0.895	0.90	0.910	
INPUT LOGIC LEVELS – BSTOP						
V_{TH-BS}	Threshold voltage		0.7	1	1.3	V
I_{PU-BS}	Internal pull-up current	V_{BSTOP} = V_{TH-BS}		10		µA
OUTPUT LOGIC LEVELS – STAT1, STAT2, $\overline{\text{PGOOD}}$						
$I_{SINK-MAX}$	Maximum sink current	V_{PIN} = 2V, output transistor ON	2.5	5		mA
V_{SAT}	Output saturation voltage	I_{SINK} = 1.6 mA		250	450	mV
		I_{SINK} = 50 µA		30	50	mV
I_{lkg}	Leakage current	V_{PIN} = 40V, output transistor OFF		1	3	µA

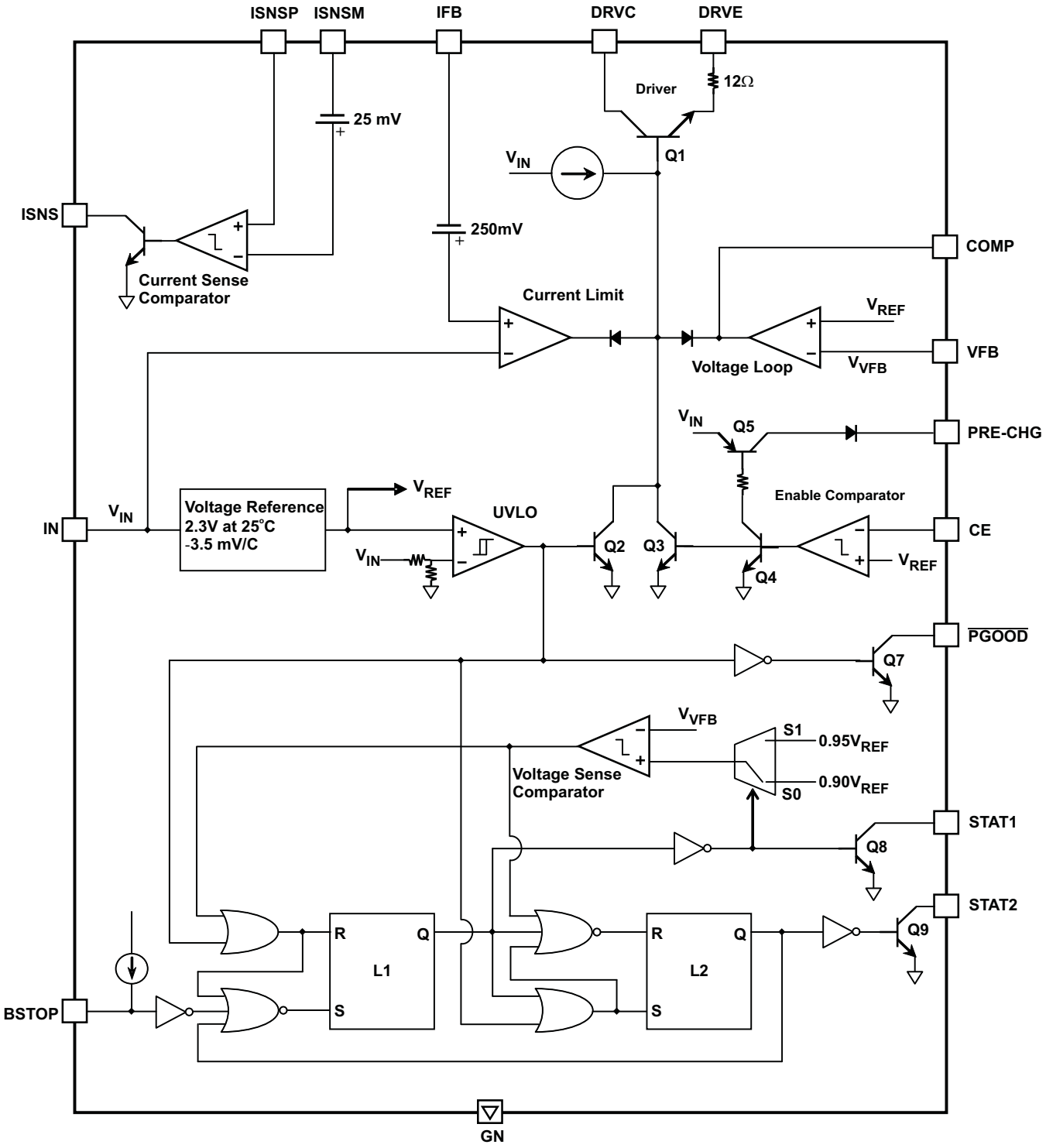


Figure 2. Simplified Block Diagram

PIN FUNCTIONS

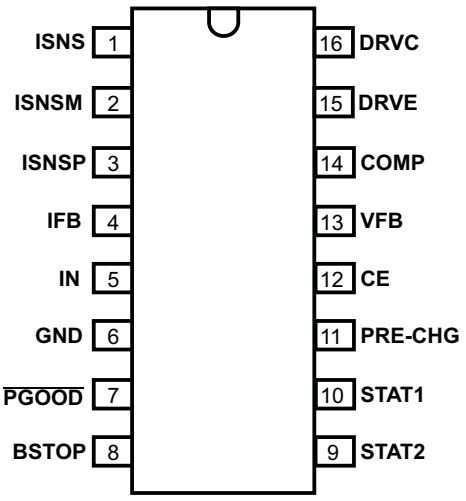
PIN		I/O	DESCRIPTION
NO.	NAME		
1	ISNS	O	Output of the current-sense comparator. Open-Collector.
2	ISNSM	I	Negative input of the current-sense comparator.
3	ISNSP	I	Positive input of the current-sense comparator.
4	IFB	I	Input for the current-regulating loop. External resistor between IN and IFB sets the charging current value.
5	IN	I	Supply voltage pin. Connect to external DC source.
6	GND	–	Ground terminal.
7	PGOOD	O	Open-collector output, indicates supply status at IN pin. Active low.
8	BSTOP	I	Control input. Taking this pin from low to high transitions the charger from Boost Mode to Float Mode. Internally pulled up through a 10µA current source.
9	STAT2	O	Open-collector status outputs. See table below.
10	STAT1	O	
11	PRE-CHG	O	Can be used to trickle-charge the battery till its voltage rises to a safe value. PRE-CHG will source current as long as the control voltage on the CE pin is below VREF. If using, connect to battery pack through external resistor.
12	CE	I	Charge enable control. If the voltage on the CE pin is below VREF, the driver transistor will be off and the PRE-CHG pin will source current.
13	VFB	I	Voltage feedback pin. Connect to battery through external resistive divider.
14	COMP	I/O	Compensation terminal for voltage loop. Connect a capacitor from this pin to GND.
15	DRVE	O	Emitter of the internal (NPN) driver transistor.
16	DRVC	I	Collector of the internal (NPN) driver transistor.

STAT1	STAT2	CONDITION
On	Hi-Z	Bulk Charge
On	On	Boost Mode

PINOUT

STAT1	STAT2	CONDITION
Hi-Z	Hi-Z	Float Mode

DW PACKAGE
(TOP VIEW)



TYPICAL OPERATING PERFORMANCE

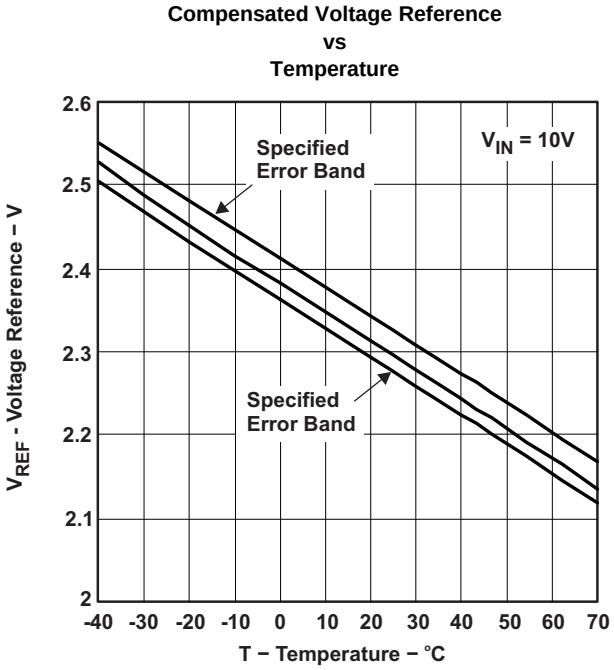


Figure 3. -

DETAILED FUNCTIONAL DESCRIPTION

The bq24450 contains all the necessary circuitry to optimally control the charging of sealed lead-acid batteries. The IC controls the charging current as well as the charging voltage to safely and efficiently charge the battery, maximizing battery capacity and life. Depending on the application, the IC can be configured in various ways: examples are a constant-voltage float charger, a dual-voltage float-cum-boost charger or a dual step current charger.

Only an external pass transistor and minimum number of external passive components are required along with the IC to implement a charger for sealed lead-acid batteries. The IC's internal driver transistor Q1 (see Figure 2) supports NPN as well as PNP pass transistors, and provides enough drive current (25mA specified) to support a wide range of charging rates.

The driver transistor is controlled by a voltage regulating loop and a current limiting-limiting loop (see Figure 2). The current-limiting loop reduces drive when the voltage between the IN pin and the IFB pin increases towards V_{ILIM} (250mV typical). The voltage regulating loop tries to maintain the voltage on the VFB pin at V_{REF}. Together, these two loops constitute a current-limited precision constant-voltage system, which is the heart of any lead-acid charger. The voltage regulating amplifier needs an external compensation circuit which depends on the type of external pass transistor (see Application Information section).

An important feature of the bq24450 is the precision reference voltage. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. Additionally, the IC operates with low supply current, only 1.6mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature by avoiding self-heating effects. To take full advantage of the temperature-compensated reference, the IC should be in the same thermal environment as the battery.

An undervoltage lock-out circuit is also provided (see Figure 2). This circuit disables the driver transistor as long as the input voltage is below UVLO (4.5V typical). The UVLO circuit also drives an open-collector output PGOOD.

Voltage-sense and current-sense comparators are available in the IC. The current-sense comparator is uncommitted. Its open-collector output is OFF when the difference between the ISNSP and ISNSM pins is less than V_{ISNS} (25mV typical), and ON when the difference is more than V_{ISNS}. Depending on the application, this comparator may be used to switch to float charging after the boost phase is over. The voltage sense comparator can be used to sense the voltage level of the battery to initiate a new charge cycle.

Latches L1 and L2 constitute a state-machine to control the charging sequence. The internal inputs to the state-machine come from the UVLO circuit and the voltage-sense comparator. One external input is provided, the BSTOP pin. The outputs of the L1 and L2 latches are available at the STAT1 and STAT2 pins. The BSTOP pin is internally pulled up through a 10µA current source. The states of the state-machine are:

Q(L1)	Q(L2)	STAT1	STAT2	Condition	State #
LOW	HIGH	ON	OFF	Bulk Charge	State 1
LOW	LOW	ON	ON	Boost Mode	State 2
HIGH	HIGH	OFF	OFF	Float Mode	State 3

A small bias current source is available at the PRE-CHG pin to provide pre-charge to deeply discharged batteries. The PRE-CHG pin sources current when the voltage at the CE pin is below VREF. Driver transistor Q1 is turned OFF when the PRE-CHG current is ON.

DETAILED OPERATION AND APPLICATION INFORMATION

A Simple Dual-Level Float-Cum-Boost Charger

Figure 4 shows the bq24450 configured as a simple dual-level float-cum-boost charger. Figure 5 shows the sequence of events that occur in a normal charge cycle. At (1) in Figure 5, power is switched ON. As long as the input voltage V_{IN} is below the undervoltage lockout threshold UVLO, Q2 is ON, disabling the driver transistor Q1. As the input voltage V_{IN} ramps up and rises above UVLO Q2 turns OFF. This enables Q1 and thus the external transistor Q_{EXT}. At the same time, Q7 turns ON, latch L1 is forced to RESET and latch L2 is SET (see Figure 2 for the internals of the Charging State Logic).

The voltage regulating amplifier tries to force the voltage at the VFB pin to V_{REF} by turning Q1 and thus Q_{EXT} fully ON, but the current limiting amplifier limits the charging current I_{CHG} to $I_{MAX-CHG}$ such that the voltage across R_{ISNS} is V_{ILIM} – 250mV typical. Thus $I_{MAX-CHG}$ is given by:

$$I_{MAX-CHG} = V_{ILIM} \div R_{ISNS}$$

As I_{CHG} flows into the battery, the battery terminal voltage increases. The voltage at the VFB pin is the battery voltage scaled by the resistive divider formed by R_A and $R_B//R_C$ (because Q8 is ON). At (3), the voltage on the VFB pin exceeds $0.95V_{REF}$, and the output of the voltage sense comparator goes HIGH. This forces L2 to RESET, and STAT2 turns ON. The battery voltage V_{BI} at this point when STAT2 indicates boost is given by:

$$V_{BI} = 0.95V_{REF} \times (R_A + R_B//R_C) \div R_B//R_C$$

Other than STAT2 changing state at this point, there is no externally observable change in the charging conditions. $I_{MAX-CHG}$ continues to flow into the battery.

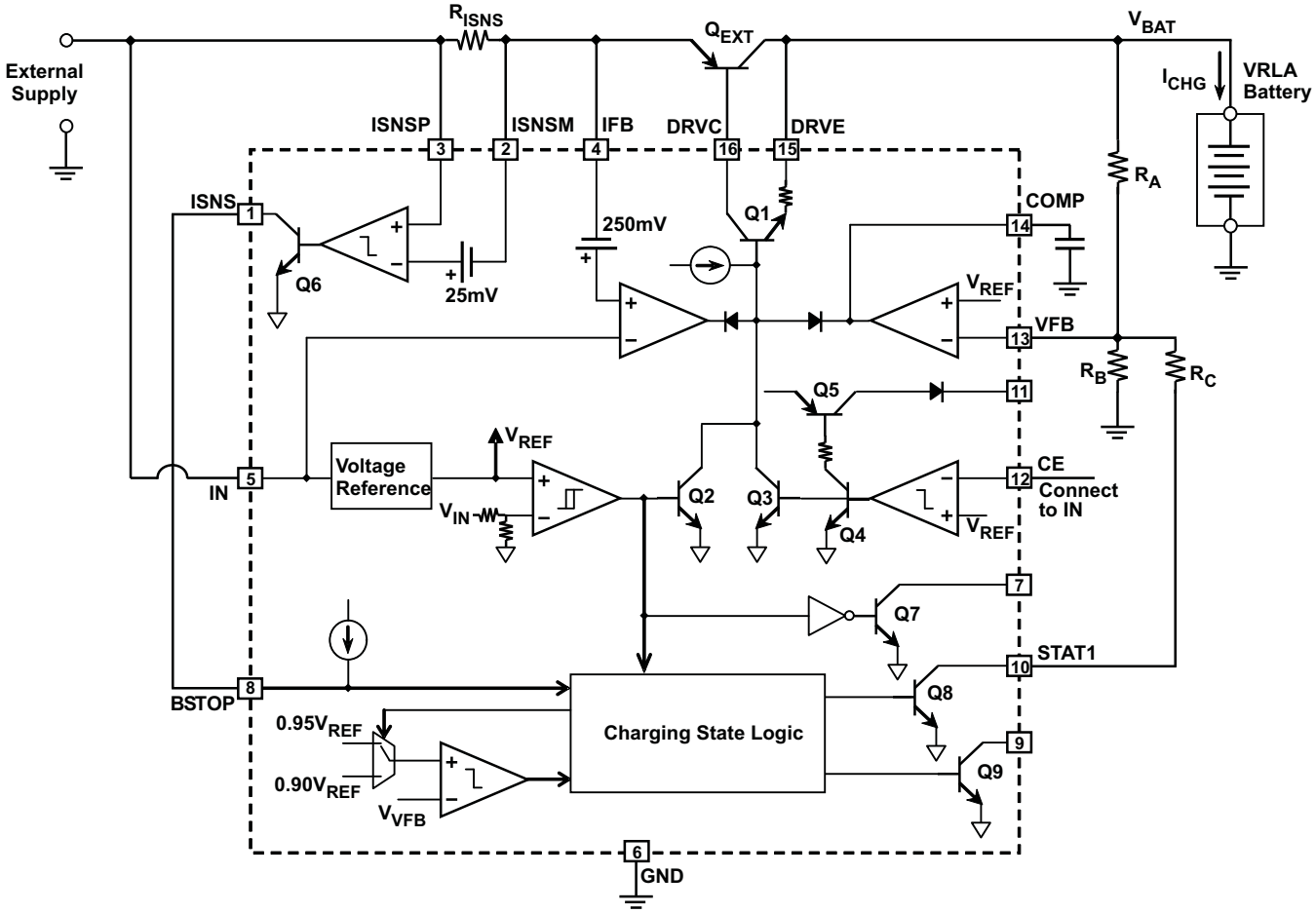


Figure 4.

As charging proceeds, the voltage at the VFB pin increases further to V_{REF}. At this point, the voltage regulating amplifier prevents the voltage at the VFB pin from rising further, maintaining the battery voltage at V_{BOOST}. [(4) in Figure 4].

$$V_{BOOST} = V_{REF} \times (R_A + R_B//R_C) \div R_B//R_C$$

I_{CHG} keeps flowing into the battery. As the battery approaches full charge, the current into the battery decreases, while the battery terminal voltage is maintained at V_{BOOST}.

At (5), the charging current I_{CHG} reduces to a value I_{TAPER} such that the voltage across R_{ISNS} becomes less than V_{ISNS} (25mV typical)

$$I_{TAPER} = V_{ISNS} \div R_{ISNS}$$

Q6 at the output of the current sense comparator turns OFF. The internal current source pulls the BSTOP pin HIGH, latch L1 is forced to SET, in turn forcing L2 to SET. The reference voltage on the voltage sense comparator is now $0.9V_{REF}$. STAT1 turns OFF, and the voltage on the battery settles to:

$$V_{FLOAT} = V_{REF} \times (R_A + R_B) \div R_B$$

As long as the peak load current is less than $I_{MAX\text{-}CHG}$, it will be supplied by Q_{EXT}, and the voltage across the battery will be maintained at V_{FLOAT}. But if the peak load current exceeds $I_{MAX\text{-}CHG}$, the battery will have to provide the excess current, and the battery terminal voltage will drop. Once it drops below $0.9V_{REF}$, at (6) in Figure 4, a new charge cycle is initiated. The battery voltage V_{BAT} at this point, V_{RCH}, is given by:

$$V_{RCH} = 0.9V_{REF} \times (R_A + R_B) / R_B$$

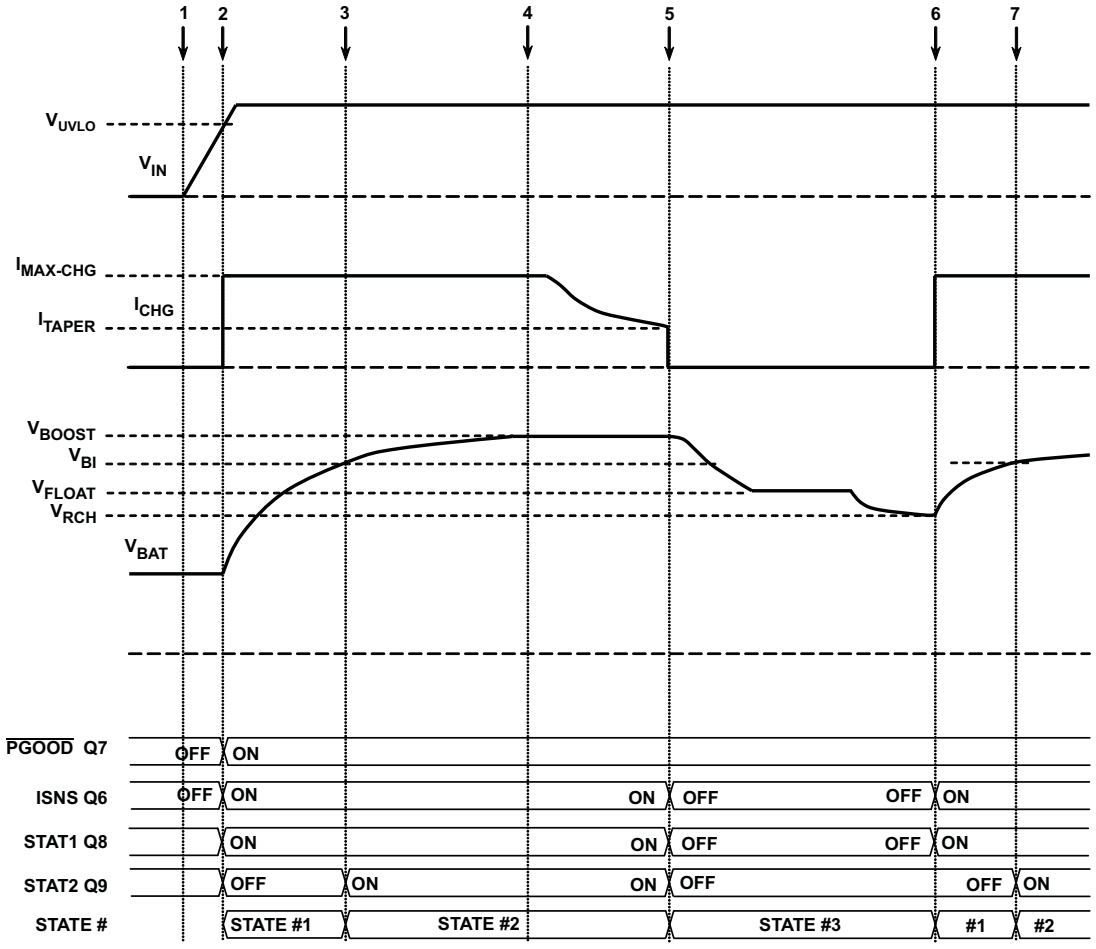


Figure 5.

An Improved Dual-Level Float-Cum-Boost Charger with Pre-Charge

The problem with the charger circuit shown in Figure 4 is that even with deeply discharged batteries, charging starts at full current level $I_{MAX-CHG}$. This can sometimes be hazardous, resulting in out-gassing from the battery. The bq24450 can be configured to pre-charge the battery till the voltage levels rise to levels safe enough to permit charging at $I_{MAX-CHG}$.

In the circuit of Figure 6, the CE pin is used to detect the battery voltage. As long as the voltage at the CE pin is below V_{REF}, the enable comparator turns ON Q3 and Q4. This turns OFF Q1 and turns ON Q5, permitting a pre-charge current I_{PRE} to flow from the PRE-CHG pin through R_T into the battery. In the following equation, V_{PRE} is the voltage drop across the internal transistor, Q5, and the internal diode.

$$I_{PRE} = (V_{IN} – V_{PRE} – V_{BAT}) \div R_T$$

Once the battery voltage rises above a safe threshold V_{TH} at (2) in Figure 7, the enable comparator turns OFF Q3 and Q4, thus turning OFF Q5 and enabling Q1. Q_{EXT} then provides $I_{MAX-CHG}$, and the circuit after this performs as described before.

$$V_{TH} = V_{REF} \times (R_A + R_B + R_C//R_D) \div (R_B + R_C//R_D)$$

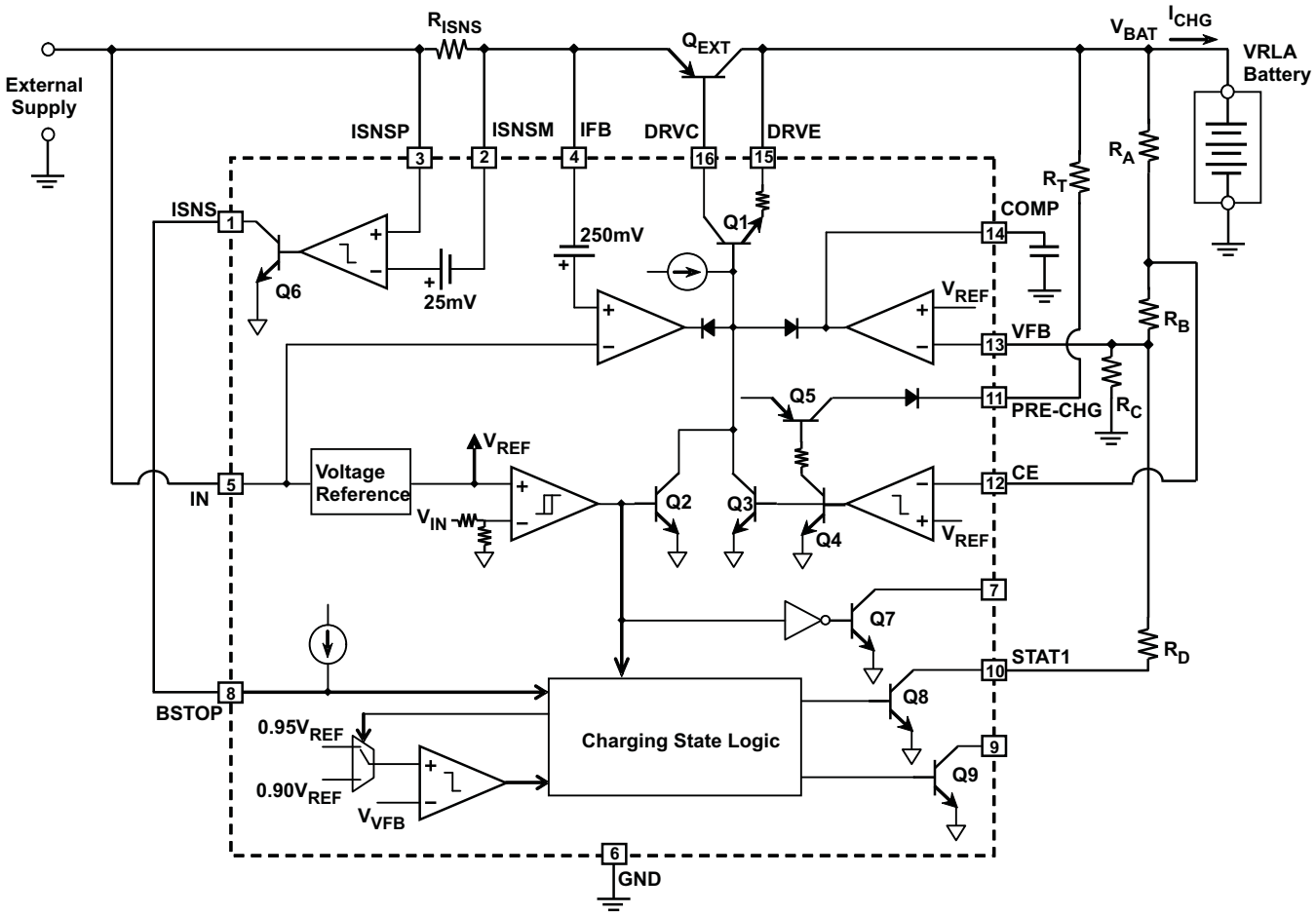


Figure 6.

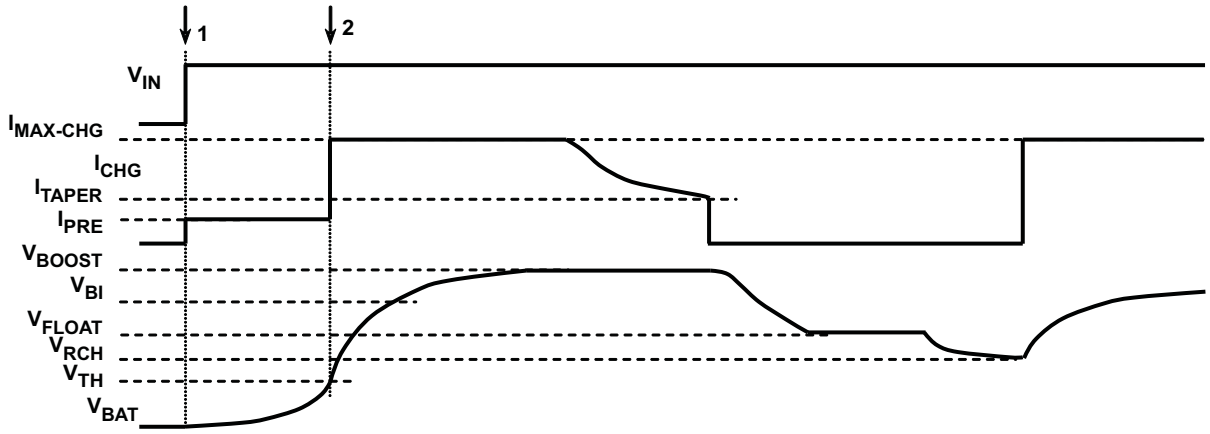


Figure 7.

Further Improvements to the Circuit of Figure 6

In applications where the load current is low, the current through the V_{BAT} voltage divider can be a non-negligible proportion of the load current. Current flowing back thorough Q_{EXT} when the input power is removed constitutes another drainage path. The modifications in Figure 8 fix both these issues.

The addition of D_{EXT} (see Figure 8) fixes the reverse current problem. Returning the voltage feedback divider chain to the PGOOD pin instead of to GND ensures that the divider does not draw any current when the input supply is not present. (When sinking 50µA, the saturation voltage of the PGOOD transistor is typically only 30mV).

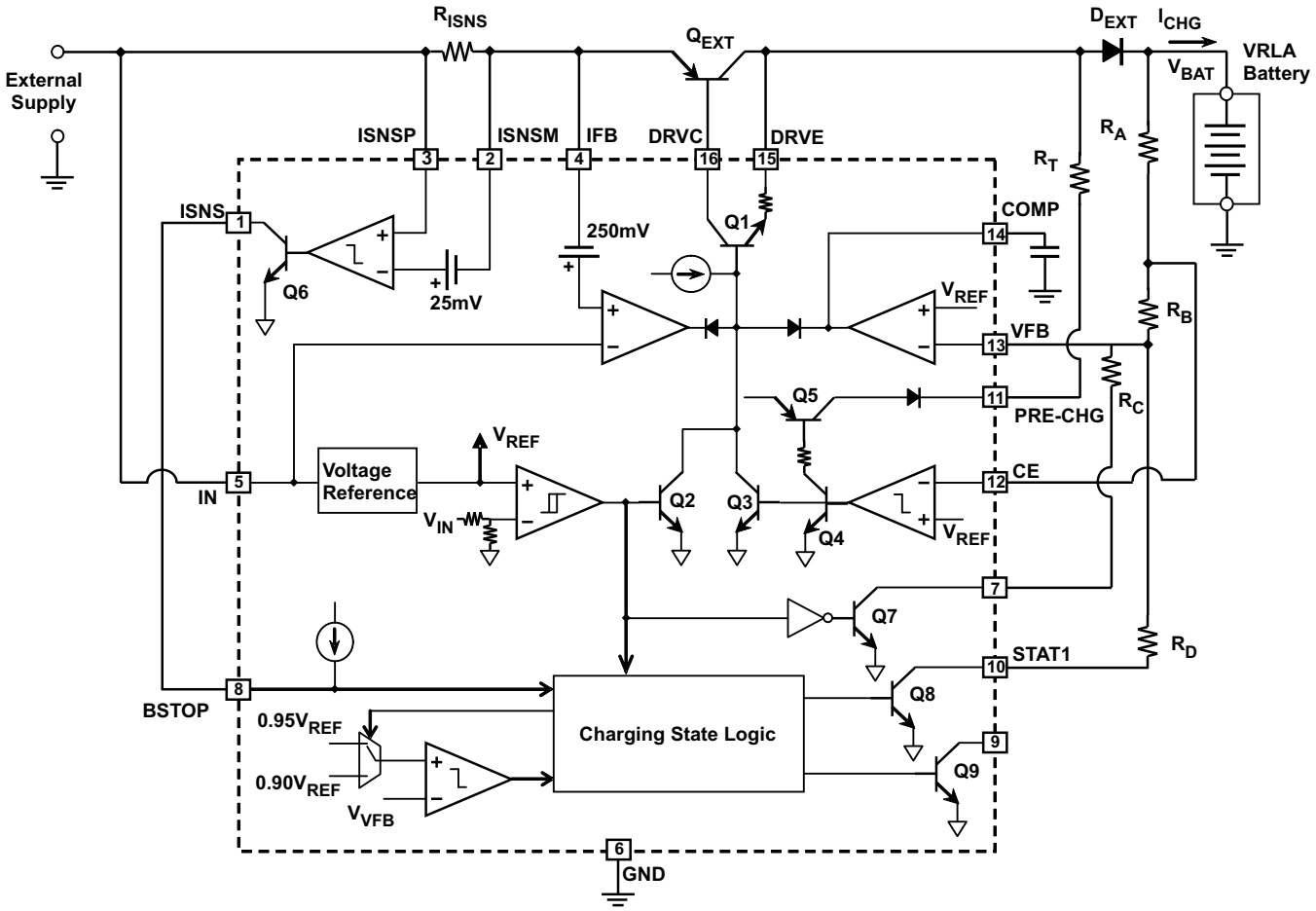


Figure 8.

Changing the value of I_{TAPER} for a given $I_{MAX-CHG}$

In the examples above, I_{TAPER} is 10% of $I_{MAX-CHG}$, because V_{ILIM} is 250mV and V_{ISNS} is 25mV (typical values), and the same resistor is used for both, the taper comparator and the current-loop amplifier. In most applications, setting I_{TAPER} to 10% of $I_{MAX-CHG}$ is perfectly fine. But if, for some reason, a different value of I_{TAPER} is required, it can be achieved, as shown in Figure 9(a) and Figure 9(b).

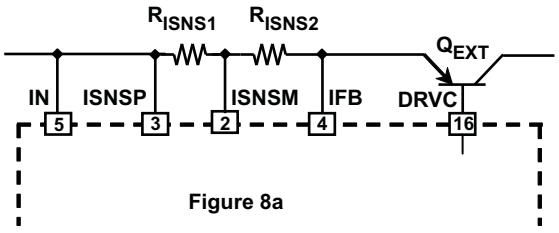


Figure 8a

$I_{MAX-CHG} = V_{ILIM} \div (R_{ISNS1} + R_{ISNS2})$

$I_{TAPER} = V_{ISNS} \div R_{ISNS2}$

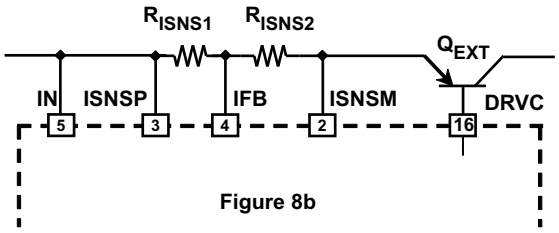


Figure 8b

$I_{MAX-CHG} = V_{ILIM} \div R_{ISNS1}$

$I_{TAPER} = V_{ISNS} \div (R_{ISNS1} + R_{ISNS2})$

Figure 9.

Selecting the External Pass Transistor

All the examples so far have used a PNP transistor for the external pass element. But the driver transistor in the bq24450 can be configured to drive many different types of pass transistors. This section will look at some of the different configurations that are possible. In all configurations, though, these factors hold:

1. The external pass device must have sufficient voltage rating for the application, and must have the current and power handling capabilities to charge at the desired rate at the maximum input to output differential in the application.
2. The device must have enough current gain at the required charging current to keep the drive current below 25mA.

The choice of the pass device and the configuration of the internal driver transistor have an effect on the following:

1. The minimum and maximum practical charging current.
2. The open-loop gains of the current and voltage loops, and hence the value of the compensation capacitor at the COMP pin. In battery charging applications, dynamic response is not a requirement, and the values of C_{COMP} given below should give stable operation under all conditions.
3. The IC's power dissipation and thus its self-heating. The IC typically has a thermal resistance of 100°C/W. An external resistance R_P can be added to share some of the power dissipation and reduce the IC's self-heating.
4. The minimum differential voltage ΔV (from the input to the battery) required to operate.

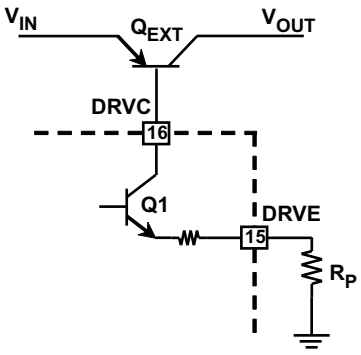
The next section addresses a few topologies, and gives values for the charge current range, the minimum input to output differential ΔV, power dissipation P_D in the IC, R_P and C_{COMP} for each of the topologies. (In the expressions below, h_{FE} is the current gain of the external transistor).

Common-Emitter PNP

$I_{MAX-CHG}$ range: 25mA to 1000mA

Minimum ΔV: 0.5V

$R_P = (V_{IN(MIN)} – 2.0V) \div I_{MAX-CHG} \times h_{FE(MIN)}$
$P_D = (V_{IN(MAX)} – 0.7V) \div h_{FE} \times I_{MAX-CHG} – (I_{MAX-CHG})^2 \div (h_{FE})^2 \times R_P$
C_{COMP} = 0.1 µF

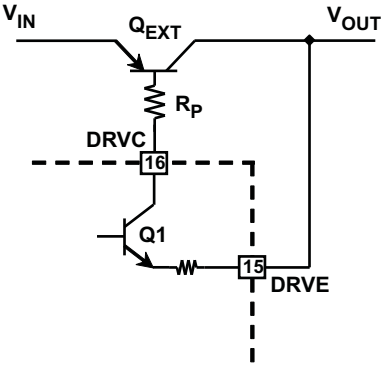


PNP in a Quasi-Darlington With Internal Driver

$I_{MAX-CHG}$ range: 25mA to 1000mA

Minimum ΔV: 2V

$R_P = (V_{IN(MIN)} – V_{OUT(MAX)} – 1.2\ V) \div I_{MAX-CHG} \times h_{FE(MIN)}$
$P_D = (V_{IN(MAX)} – V_{OUT} – 0.7V) \div h_{FE} \times I_{MAX-CHG} – (I_{MAX-CHG})^2 \div (h_{FE})^2 \times R_P$
C_{COMP} = 0.01µF to 0.047µF



External Quasi-Darlington

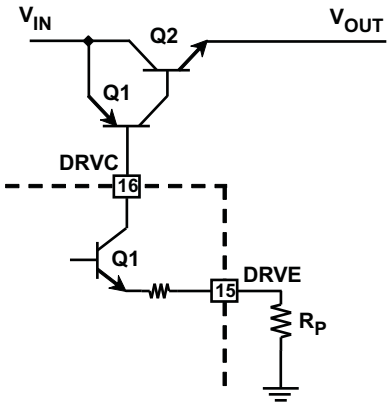
$I_{MAX-CHG}$ range: 0.6A to 15A

Minimum ΔV: 1.2V

$R_P = (V_{IN(MIN)} – 0.7\ V) \div I_{MAX-CHG} \times h_{FE1(MIN)}h_{FE2(MIN)}$

$P_D = (V_{IN(MAX)} – 0.7\ V) \div (h_{FE1} \times h_{FE2}) \times I_{MAX-CHG} – (I_{MAX-CHG})^2 \div (h_{FE1} \times h_{FE2})^2 \times R_P$

C_{COMP} = 0.22µF with 470Ω series resistor to GND



NPN Emitter-Follower

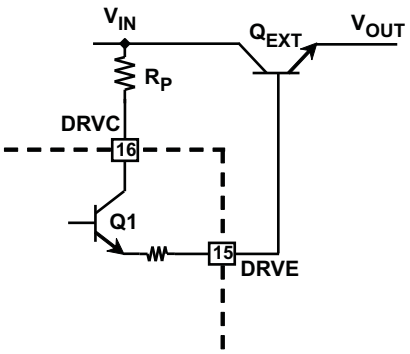
$I_{MAX-CHG}$ range: 25mA to 1000mA

Minimum ΔV: 2.7V

$R_P = (V_{IN(MIN)} – V_{OUT(MAX)} – 1.2\ V) \div I_{MAX-CHG} \times h_{FE(MIN)}$

$P_D = (V_{IN(MAX)} – V_{OUT} – 0.7\ V) \div h_{FE} \times I_{MAX-CHG} – (I_{MAX-CHG})^2 \div (h_{FE})^2 \times R_P$

C_{COMP} = 0.01µF to 0.047µF



DESIGN EXAMPLE

This section covers the design of a dual-level charger for a 6V 4Ah sealed lead-acid battery. The application is a system where the battery is used in standby mode, and the load on the battery when it powers the system is 250mA (0.06C).

The battery parameters are (see References 1 and 2)

Final discharge voltage	1.75V per cell	5.25V	V_{TH}
Float voltage	2.30V per cell	6.9V	V_{FLOAT}
Voltage in boost mode	2.45V per cell	7.35V	V_{BOOST}
Charge rate	0.05C to 0.3C	Use 0.15C = 600 mA	$I_{MAX-CHG}$
$V_{BAT(MIN)}$		4V	
Trickle charge rate		10 mA	

The charger is required to operate from a supply voltage of 9V to 13V. Therefore, the minimum input to output differential is 1.65V. To block reverse current from the battery to the input supply use a blocking diode as in Figure 8. This leaves only 0.65V as the differential across the external transistor, forcing the use of the Common-Emitter PNP topology.

Figure 10 is the schematic for this charger (from Figure 8, with the pass transistor topology changed), with the remaining task being the calculation of all the component values.

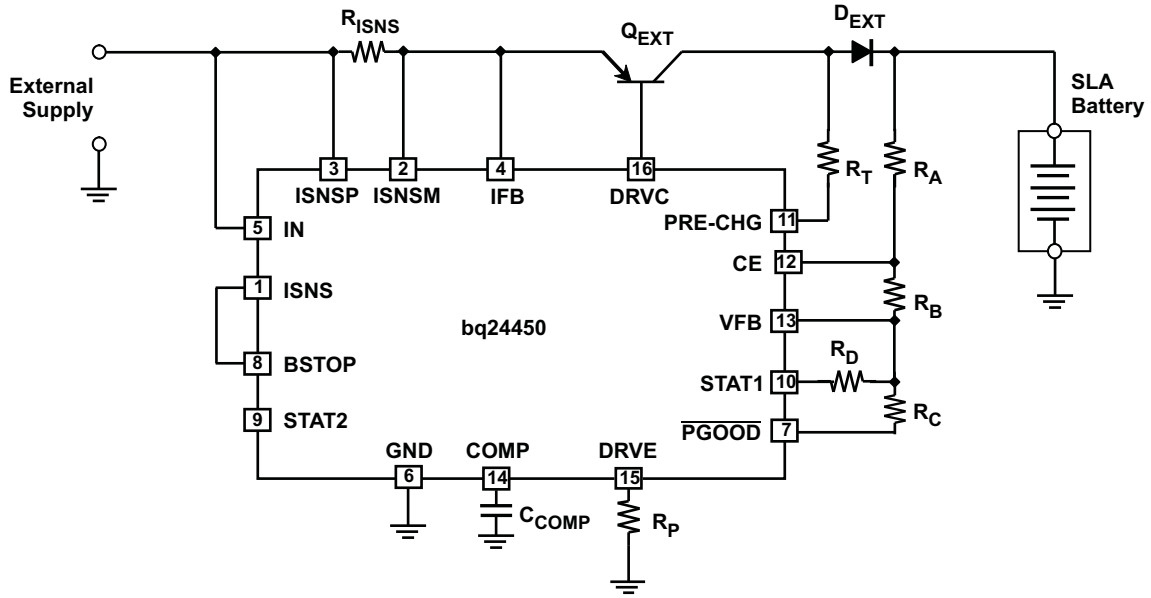


Figure 10.

The first step is to decide on the value of the current in the voltage divider resistor string in FLOAT mode. This should be substantially higher than the input bias current in the CE and VFB pins and the leakage current in the STAT1 pin, but low enough such that the voltage on the PGOOD pin does not introduce errors. A value of 50µA is suitable.

In FLOAT mode, STAT1 is OFF, so there is no current in R_D. The voltage on the VFB pin (V_{REF}) is 2.3V.

R_C = 2.30V ÷ 50µA = 46kΩ. The closest 1% value is 46.4kΩ.

$V_{FLOAT} = V_{REF} \times (R_A + R_B + R_C) \div R_C \rightarrow R_A + R_B = 2 \times R_C = 92.8k\Omega$.

$V_{BOOST} = V_{REF} \times (R_A + R_B + R_C//R_D) \div R_C//R_D \rightarrow R_D = 474.3k\Omega$. Pick the closest 1% value of 475kΩ.

$V_{TH} = V_{REF} \times (R_A + R_B + R_C//R_D) \div (R_B + R_C//R_D) \rightarrow R_B = 16.9k\Omega$.

$R_A = 92.8k\Omega - R_B = 75.9k\Omega$. The closest standard value is 75kΩ.

$I_{PRE} = (V_{IN} - V_{PRE} - V_{DEXT} - V_{BAT}) \div R_T$. Select $R_T = 634\Omega$.

For example: $I_{PRE} = (13 - 2 - 0.7 - 4) / 634 = 10mA$

$I_{MAX\text{-}CHG} = V_{ILIM} \div R_{ISNS} \rightarrow R_{ISNS} = 250mV \div 600mA = 0.417\Omega$. The closest 1% value is 0.422Ω.

For Q_{EXT}, the BD242 is suitable, and a 1N4001 will do for D_{EXT}

$R_P = (V_{IN(MIN)} - 2.0V) \div I_{MAX\text{-}CHG} \times h_{FE(MIN)} = 7 \div 0.6 \times 25 = 291.6\Omega$. Pick 294Ω from the standard values.

$P_D = (V_{IN(MAX)} - 0.7V) \div h_{FE} \times I_{MAX\text{-}CHG} - (I_{MAX\text{-}CHG})^2 \div (h_{FE})^2 \times R_P = 126mW$ under worst case conditions.

Choose C_{COMP} = 0.1µF.

REFERENCES

1. Yuasa Battery Co., NP Valve Regulated Lead Acid Battery Manual
2. Panasonic, Methods of charging the Valve-Regulated Lead-Acid Battery

REVISION HISTORY

NOTE: Page numbers of previous versions may differ from current version.

Changes from Original (April 2009) to Revision A — **Page**

- Deleted PDIP package option from Features 1
- Deleted PDIP package from Ordering Information table 2
- Changed equations to correct typo/formatting errors (3 equations) 8
- Changed equations to correct typo/formatting errors 9
- Changed equation to correct typo/formatting errors 10
- Changed three equations to correct typo/formatting errors 15
- Changed component values in "Design Example" calculations. 15

Changes from Revision A (January 2010) to Revision B — **Page**

- Added V_{PRE} with definition 10
- Changed compenent values in the I_{PRE} calculations 15

Changes from Revision B (October 2010) to Revision C — **Page**

- Changed compenent values in the I_{PRE} calculations in FLOAT mode description..... FROM "332" TO "634"; FROM "5) /332 = 16mA" TO "4)/634 = 10mA" 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24450DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ24450DW	Samples
BQ24450DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ24450DW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

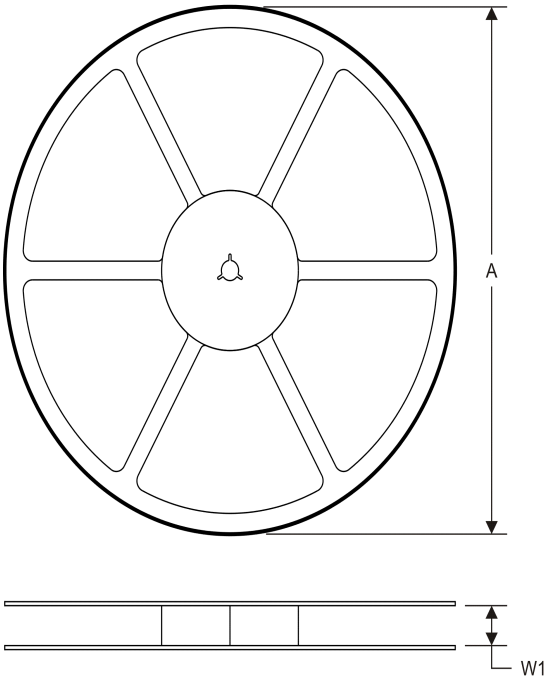
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

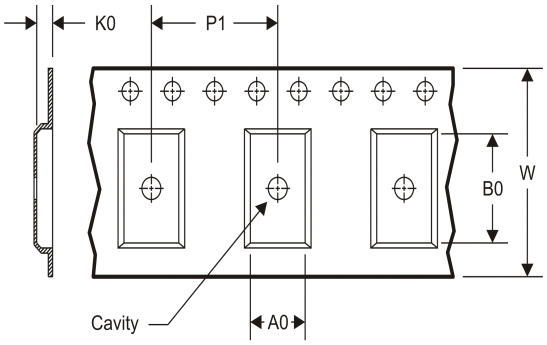
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



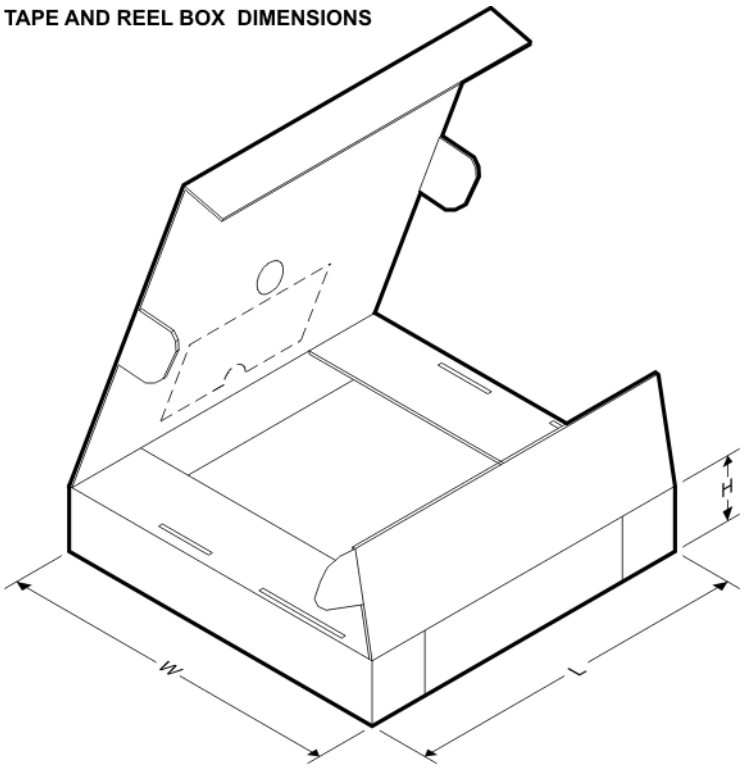
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24450DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



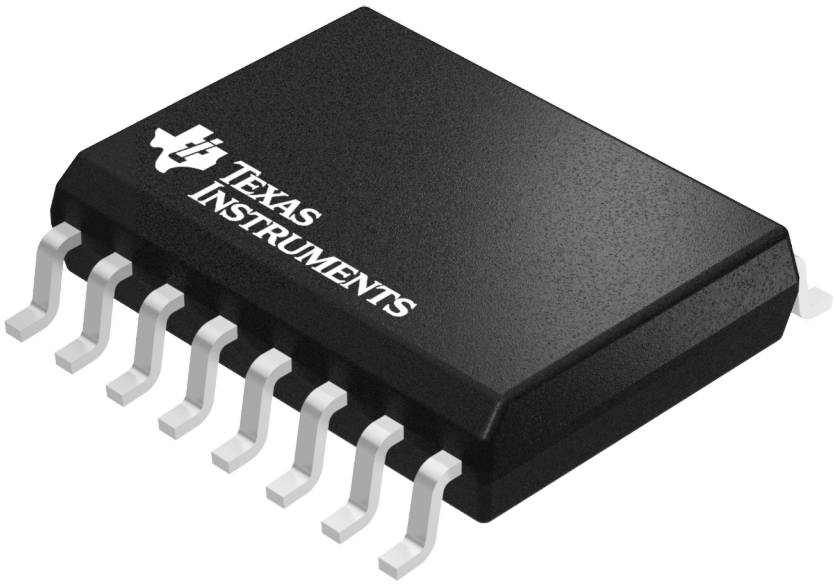
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24450DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

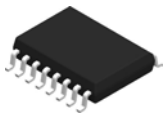
GENERIC PACKAGE VIEW

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

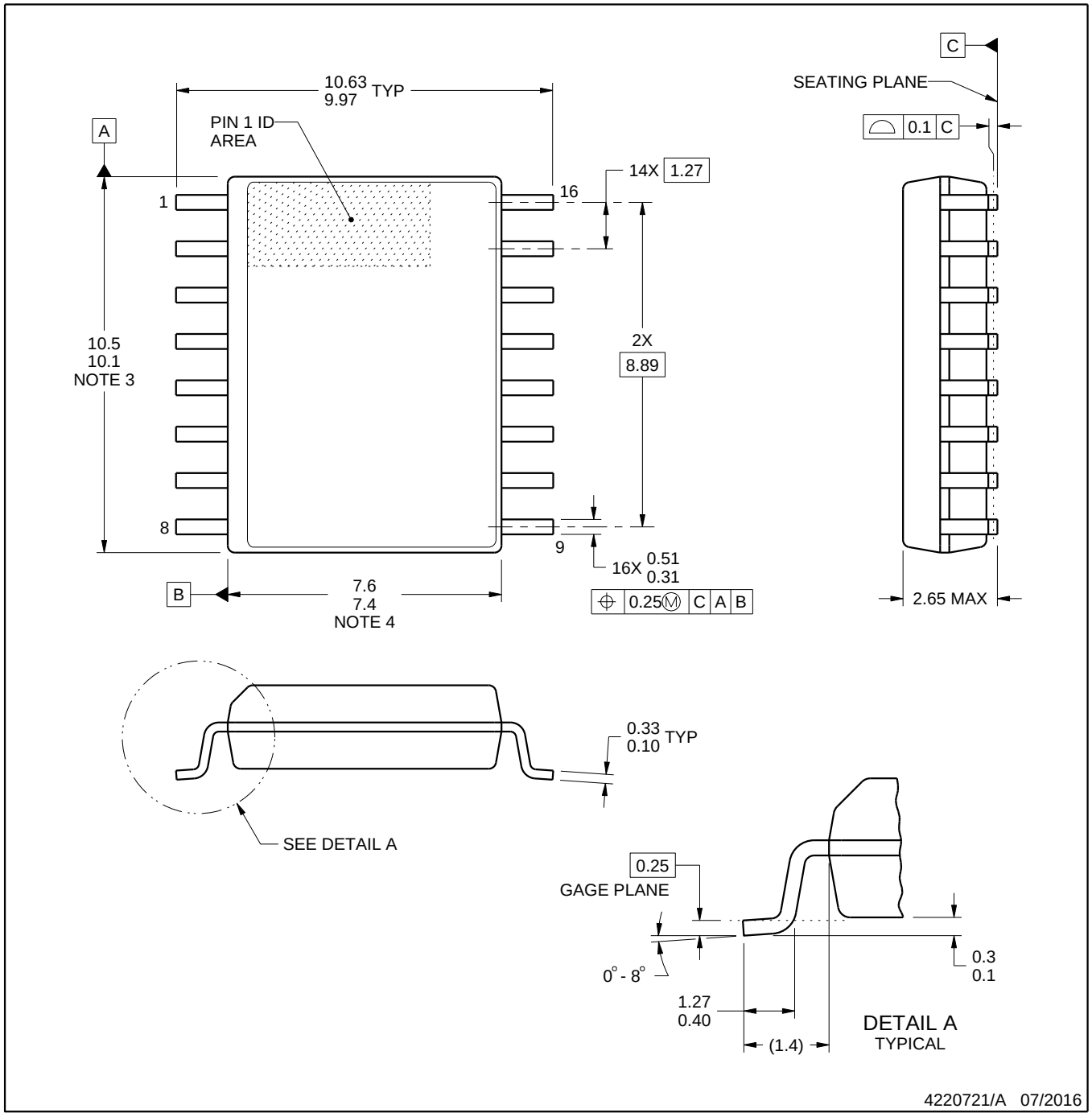


PACKAGE OUTLINE

DW0016A

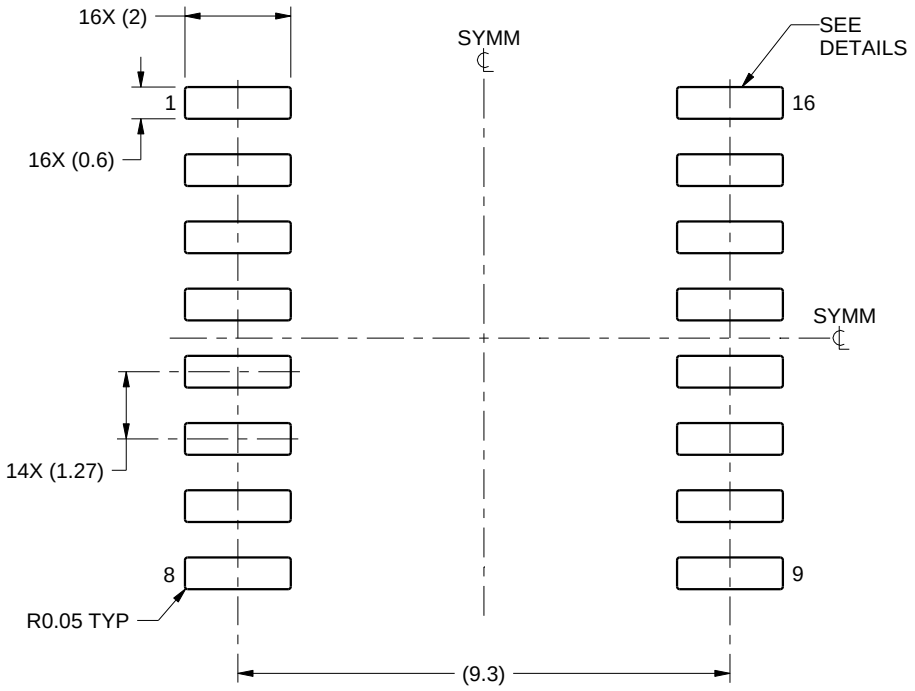
SOIC - 2.65 mm max height

SOIC

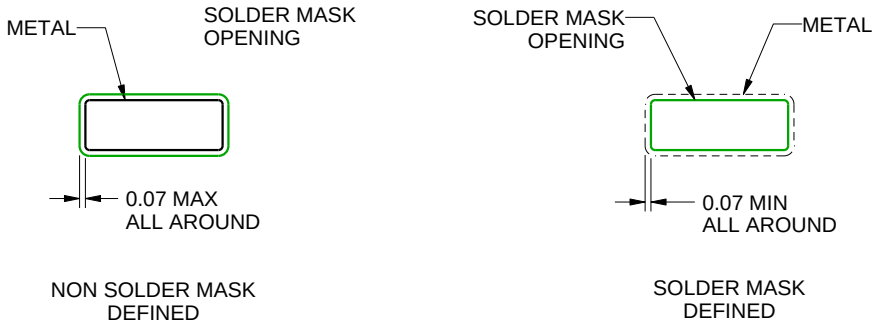


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

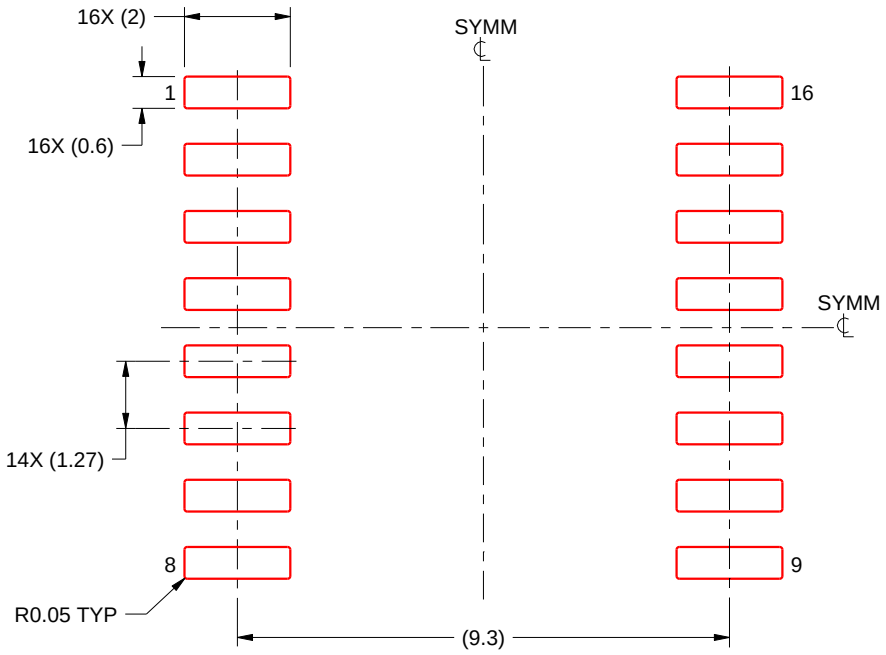


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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