![Texas Instruments logo] **TEXAS INSTRUMENTS**

# CD54/74AC257, CD54/74ACT257, CD74ACT258

## Quad 2-Input Multiplexer with Three-State Outputs

## Features

- **'AC257, 'ACT257. . . . . . . . . . . . . Non-Inverting Outputs**

- **CD74ACT258 . . . . . . . . . . . . . . . . . . Inverting Outputs**

- **Buffered Inputs**

- **Typical Propagation Delay**
  - **4.4ns at $V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 50pF**

- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**

- **SCR-Latchup-Resistant CMOS Process and Circuit Design**

- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**

- **Balanced Propagation Delays**

- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**

- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**

**Drives 50Ω Transmission Lines**

## Pinout

**CD54AC257, CD54ACT257
(CERDIP)
CD74AC257, CD74ACT257, CD74ACT258
(PDIP, SOIC)
TOP VIEW**

| ACT258 | AC/ACT257 | | | AC/ACT257 | ACT258 |
|---|---|---|---|---|---|
| **S** | **S** | 1 | 16 | $V_{CC}$ | $V_{CC}$ |
| **$1I_0$** | **$1I_0$** | 2 | 15 | $\overline{OE}$ | $\overline{OE}$ |
| **$1I_1$** | **$1I_1$** | 3 | 14 | **$4I_0$** | **$4I_0$** |
| **$\overline{1Y}$** | **1Y** | 4 | 13 | **$4I_1$** | **$4I_1$** |
| **$2I_0$** | **$2I_0$** | 5 | 12 | **4Y** | **$\overline{4Y}$** |
| **$2I_1$** | **$2I_1$** | 6 | 11 | **$3I_0$** | **$3I_0$** |
| **$\overline{2Y}$** | **2Y** | 7 | 10 | **$3I_1$** | **$3I_1$** |
| **GND** | **GND** | 8 | 9 | **3Y** | **$\overline{3Y}$** |

## Description

The 'AC257, 'ACT257 and CD74ACT258 are quad 2-input multiplexers with three-state outputs that utilize Advanced CMOS Logic technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs (Y or $\overline{Y}$) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 'AC257, 'ACT257, and CD74ACT258. The state of the Select input determines the particular register from which the data comes. The 'AC257, 'ACT257 and CD74ACT258 can also be used as function generators.

## Ordering Information

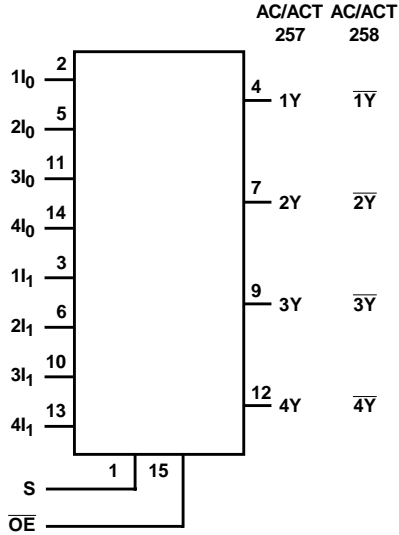| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---|---|---|
| CD54AC257F3A | -55 to 125 | 16 Ld CERDIP |
| CD74AC257E | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld PDIP |
| CD74AC257M | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld SOIC |
| CD54ACT257F3A | -55 to 125 | 16 Ld CERDIP |
| CD74ACT257E | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld PDIP |
| CD74ACT257M | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld SOIC |
| CD74ACT258E | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld PDIP |
| CD74ACT258M | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld SOIC |
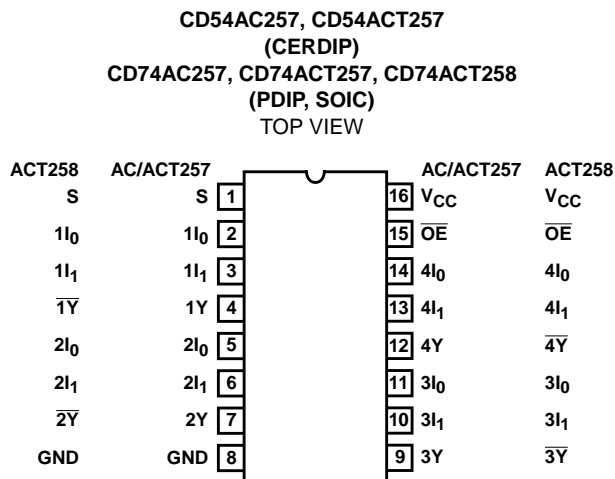
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

## *Functional Diagram*

```
                                  AC/ACT AC/ACT
                                   257    258
1I0  ──2──┐                      ┌──4── 1Y    1̄Ȳ
2I0  ──5──┤                      │
3I0  ──11─┤                      ├──7── 2Y    2̄Ȳ
4I0  ──14─┤                      │
1I1  ──3──┤                      ├──9── 3Y    3̄Ȳ
2I1  ──6──┤                      │
3I1  ──10─┤                      ├──12── 4Y   4̄Ȳ
4I1  ──13─┤                      │
          └── 1 │ 15 ────────────┘
S    ───────┘
OE̅   ──────────────┘
```

**TRUTH TABLE**

| OUTPUT ENABLE | SELECT INPUT | DATA INPUTS | | 257 OUTPUTS | 258 OUTPUTS |
|---|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | Y | $\overline{Y}$ |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = High level voltage, L = Low level voltage, Z = High impedance (off) state, X = Don't Care

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 6V
DC Input Diode Current, $I_{IK}$
   For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
   For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . ±50mA
DC Output Source or Sink Current per Output Pin, $I_O$
   For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . ±50mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) . . . . . . . . ±100mA

### Thermal Information

Thermal Resistance (Typical, Note 5)       $\theta_{JA}$ ($^{o}$C/W)
   PDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .   ___
   SOIC Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .   ___
Maximum Junction Temperature (Plastic Package) . . . . . . . . . . 150$^{o}$C
Maximum Storage Temperature Range . . . . . . . . . . -65$^{o}$C to 150$^{o}$C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . . 300$^{o}$C

### Operating Conditions

Temperature Range, $T_A$ . . . . . . . . . . . . . . . . . . . . . . . -55$^{o}$C to 125$^{o}$C
Supply Voltage Range, $V_{CC}$ (Note 4)
   AC Types. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1.5V to 5.5V
   ACT Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . . . . . . . . . . . . . 0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv
   AC Types, 1.5V to 3V . . . . . . . . . . . . . . . . . . . . . . . . 50ns (Max)
   AC Types, 3.6V to 5.5V . . . . . . . . . . . . . . . . . . . . . . . 20ns (Max)
   ACT Types, 4.5V to 5.5V . . . . . . . . . . . . . . . . . . . . . . 10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

3. For up to 4 outputs per device, add ±25mA for each additional output.

4. Unless otherwise specified, all voltages are referenced to ground.

5. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25$^{o}$C | | -40$^{o}$C TO 85$^{o}$C | | -55$^{o}$C TO 125$^{o}$C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **AC TYPES** | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |

## DC Electrical Specifications  (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | MAX | -40°C TO 85°C MIN | MAX | -55°C TO 125°C MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| **ACT TYPES** | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State or Leakage Current | $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | $\Delta I_{CC}$ | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA |

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

## ACT Input Load Table

| INPUT | UNIT LOAD |
|---|---|
| Data | 0.83 |
| S | 1.27 |
| $\overline{OE}$ | 1.27 |

NOTE: Unit load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

## Switching Specifications  Input $t_r$, $t_f$ = 3ns, $C_L$ = 50pF (Worst Case)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **AC TYPES** | | | | | | | | | |
| Propagation Delay, In to Y AC/ACT257 | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 106 | - | - | 117 | ns |
| | | 3.3 (Note 9) | 3.3 | - | 11.8 | 3.3 | - | 13 | ns |
| | | 5 (Note 10) | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to Y AC/ACT257 | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, $\overline{OE}$ to Y AC/ACT257 | $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$ | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Propagation Delay, In to $\overline{Y}$ 'AC/CD74ACT258 | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 91 | - | - | 100 | ns |
| | | 3.3 | 2.9 | - | 10.2 | 2.8 | - | 11.2 | ns |
| | | 5 | 2.1 | - | 7.3 | 2 | - | 8 | ns |
| Propagation Delay, S to $\overline{Y}$ 'AC/CD74ACT258 | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, $\overline{OE}$ to $\overline{Y}$ 'AC/CD74ACT258 | $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$ | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Three-State Output Capacitance | $C_O$ | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | $C_I$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ (Note 11) | - | - | 130 | - | - | 130 | - | pF |
| **ACT TYPES** | | | | | | | | | |
| Propagation Delay, In to Y AC/ACT257 | $t_{PLH}$, $t_{PHL}$ | 5 (Note 10) | 2.8 | - | 9.7 | 2.7 | - | 10.7 | ns |
| Propagation Delay, S to Y AC/ACT257 | $t_{PLH}$, $t_{PHL}$ | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 3ns, $C_L$ = 50pF (Worst Case)   **(Continued)**

| PARAMETER | SYMBOL | V$_{CC}$ (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Propagation Delay, $\overline{OE}$ to Y AC/ACT257 | t$_{PLZ}$, t$_{PHZ}$, t$_{PZL}$, t$_{PZH}$ | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Propagation Delay, In to $\overline{Y}$ 'AC/CD74ACT258 | t$_{PLH}$, t$_{PHL}$ | 5 | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to $\overline{Y}$ 'AC/CD74ACT258 | t$_{PLH}$, t$_{PHL}$ | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |
| Propagation Delay, $\overline{OE}$ to $\overline{Y}$ 'AC/CD74ACT258 | t$_{PLZ}$, t$_{PHZ}$, t$_{PZL}$, t$_{PZH}$ | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Three-State Output Capacitance | C$_O$ | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | C$_I$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C$_{PD}$ (Note 11) | - | - | 130 | - | - | 130 | - | pF |

NOTES:

8. Limits tested 100%.

9. 3.3V Min is at 3.6V, Max is at 3V.

10. 5V Min is at 5.5V, Max is at 4.5V.

11. $C_{PD}$ is used to determine the dynamic power consumption per multiplexer.
   AC: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
   ACT: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where $f_i$ = input frequency, $f_o$ = output frequency, $C_L$ = output load capacitance, $V_{CC}$ = supply voltage.



†FOR AC SERIES ONLY: WHEN V$_{CC}$ = 1.5V, R$_L$ = 1kΩ
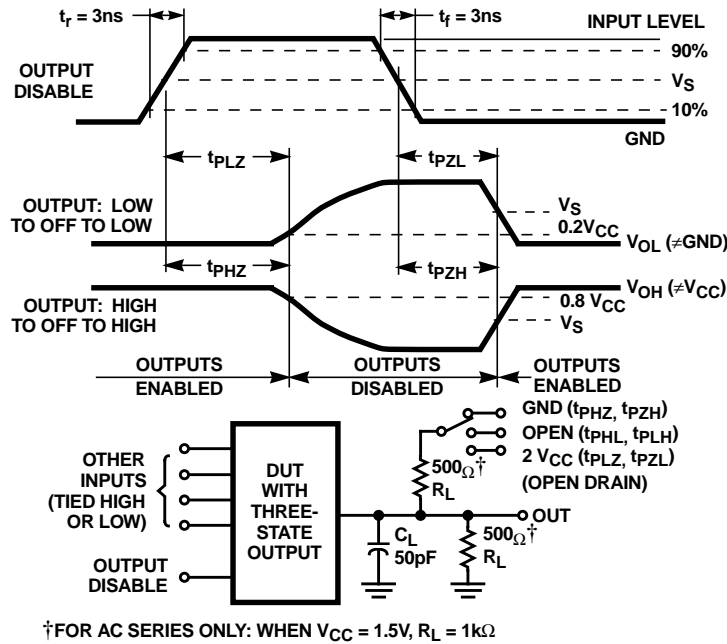
**FIGURE 1.  THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT**
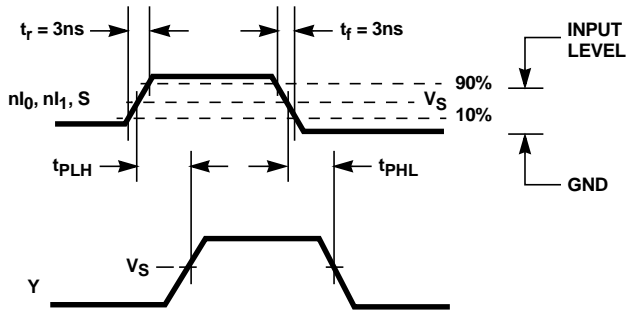
**FIGURE 2. INPUTS OR SELECT TO OUTPUT PROPAGATION DELAYS (AC/ACT257)**
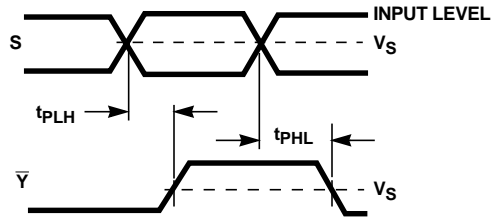


**FIGURE 3. SELECT TO OUTPUT PROPAGATION DELAYS (CD74ACT258)**
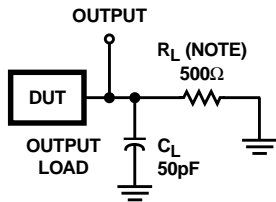


NOTE: For AC Series Only: When $V_{CC}$ = 1.5V, $R_L$ = 1kΩ.

|  | AC | ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

**FIGURE 4. PROPAGATION DELAY TIMES**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| CD54AC257F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54ACT257F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74AC257E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC257EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC257M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC257M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC257M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC257M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC257ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC257MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT257EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT257M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT257MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT258M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CD74ACT258M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CD74ACT258M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CD74ACT258M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CD74ACT258ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CD74ACT258MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



Cavity

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT258M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CD74AC257M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74ACT258M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

1                     7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R−PDSO−G16)                    PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
⚠C

16                    9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1                    8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/J  09/09

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
     ⚠C   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed .006 (0,15) per end.
     ⚠D   Body width does not include interlead flash.  Interlead flash shall not exceed .017 (0,43) per side.
         E.  Reference JEDEC MS−012 variation AC.

**TEXAS INSTRUMENTS**
www.ti.com

D(R−PDSO−G16)

Example Board Layout
(Note C)

0.60

1.27

1.55

5.40

Non Solder Mask Define Pad

Stencil Openings
(Note D)

0.55

1.27

1.5

5.40

0.6

1.55

Solder Mask Opening
(Note E)

Pad Geometry
(Note C)

0.07
ALL AROUND

4209373/A  03/08

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Refer to IPC7351 for alternate board design.
        D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
            contact their board assembly site for stencil design recommendations.  Refer to IPC−7525
        E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R−PDIP−T**)                                    PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A   MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A   MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

$\oplus$ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option
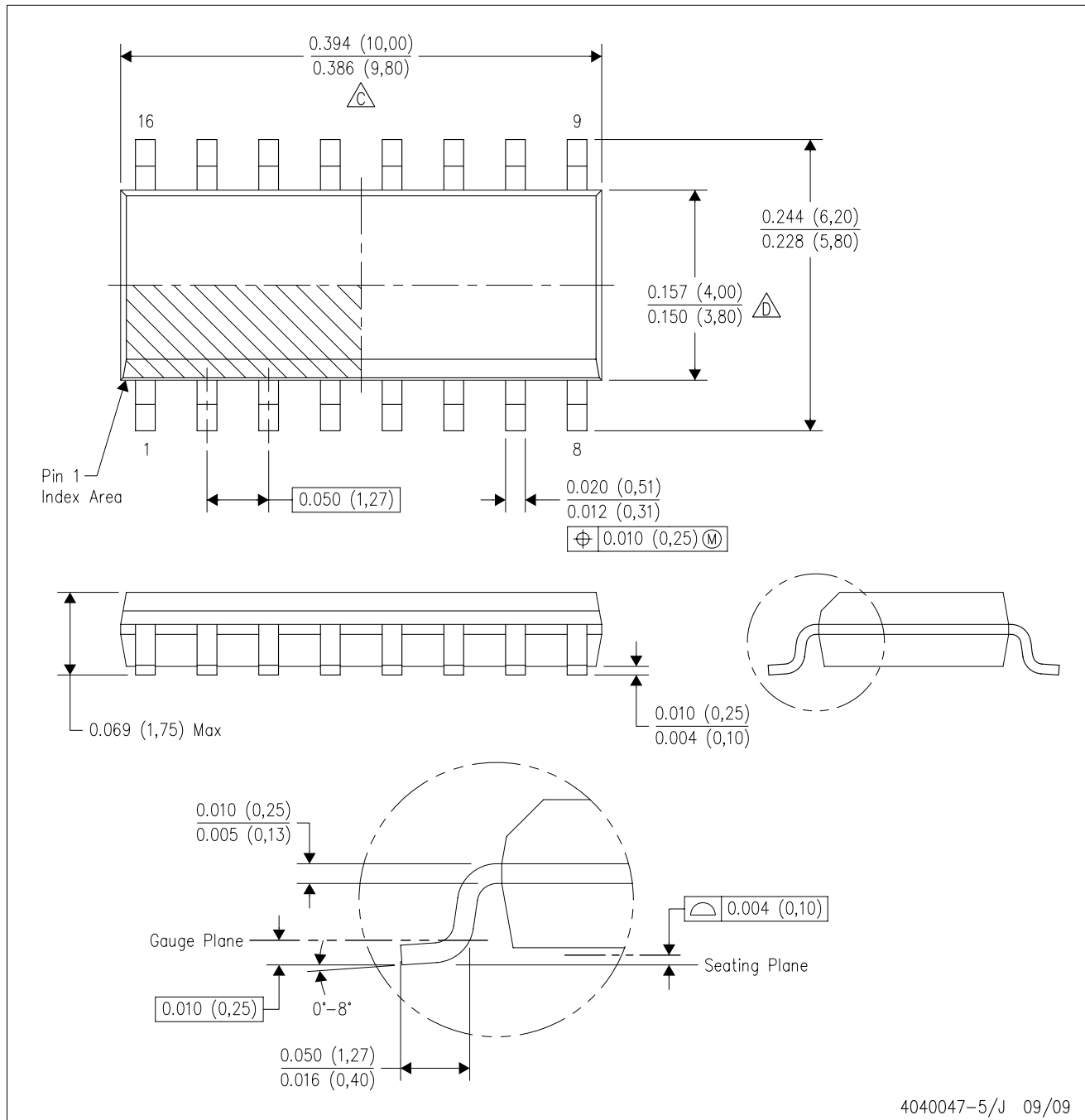
4040049/E  12/2002

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         C.  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54AC257F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54AC257F3A | Samples |
| CD54ACT257F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54ACT257F3A | Samples |
| CD74AC257E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC257E | Samples |
| CD74AC257M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC257M | Samples |
| CD74AC257M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC257M | Samples |
| CD74AC257MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC257M | Samples |
| CD74ACT257E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT257E | Samples |
| CD74ACT257EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT257E | Samples |
| CD74ACT257M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT257M | Samples |
| CD74ACT257M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT257M | Samples |
| CD74ACT257M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT257M | Samples |
| CD74ACT257MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT257M | Samples |
| CD74ACT258M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ACT258M | Samples |
| CD74ACT258M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ACT258M | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC257, CD54ACT257, CD74AC257, CD74ACT257 :**

● Catalog: CD74AC257, CD74ACT257

● Military: CD54AC257, CD54ACT257

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT258M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC257M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| CD74ACT257M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74ACT258M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14    8

C

1    7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  This package is hermetically sealed with a ceramic lid using glass frit.
        D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E.  Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

## N (R−PDIP−T**)                    PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

A

16                    9

0.260 (6,60)
0.240 (6,10)

1                    8

0.070 (1,78)
0.045 (1,14) △D

| DIM ＼ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A    MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A    MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| △C MS−001 VARIATION | AA | BB | AC | AD |

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)
⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E  12/2002

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
      △C  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      △D  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)                                                         PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
/C\

16                                                9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  /D\

1                                                8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
      /C\ C.  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
      /D\ D.  Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
          E.  Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

←16x0,55

←14x1,27

5,40

16x1,50─

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

─0,60

1,55

Example
Solder Mask Opening
(See Note E)

─0,07

All Around

4211283−4/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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