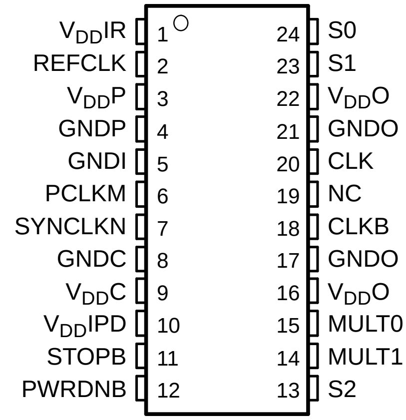
DIRECT RAMBUS™ CLOCK GENERATOR

FEATURES

- 400-MHz Differential Clock Source for Direct Rambus™ Memory Systems for an 800-MHz Data Transfer Rate
- Fail-Safe Power Up Initialization
- Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock
- Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications
- Operates From a Single 3.3-V Supply and 120 mW at 300 MHz (Typ)
- Packaged in a Shrink Small-Outline Package (DBQ)
- Supports Frequency Multipliers: 4, 6, 8, 16/3
- No External Components Required for PLL
- Supports Independent Channel Clocking
- Spread Spectrum Clocking Tracking Capability to Reduce EMI
- Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921
- Cycle-Cycle Jitter Is Less Than 50 ps at 400 MHz
- Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement
- Supports Industrial Temperature Range of –40°C to 85°C

DBQ PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

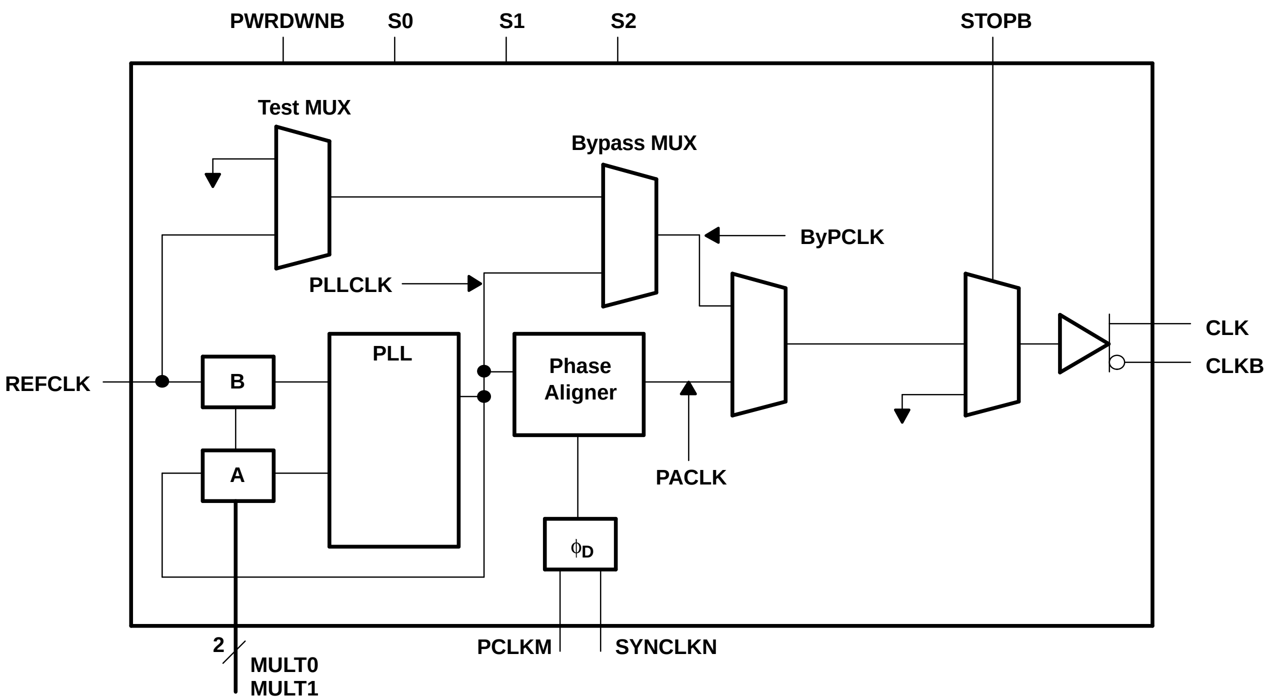
The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLKN is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 400 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCR83A has a fail-safe power up initialization state-machine which supports proper operation under all power up conditions.

The CDCR83A is characterized for operation over free-air temperatures of –40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE(1)

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output test (OE)	0	1	x	Hi-Z	Hi-Z
Reserved	0	0	1	–	–
Reserved	1	0	1	–	–
Reserved	1	1	1	Hi-Z	Hi-Z

(1) X = don't care, Hi-Z = high impedance

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
V_{DD}C	9		V_{DD} for phase aligner
V_{DD}IPD	10		Reference voltage for phase detector inputs and STOPB
V_{DD}IR	1		Reference voltage for REFCLK
V_{DD}O	16, 22		V_{DD} for clock outputs
V_{DD}P	3		V_{DD} for PLL

PLL DIVIDER SELECTION

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 400 MHz) and (33 MHz < REFCLK < 100 MHz).

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK(1) (MHz)
0	0	67	4	267
0	1	50	6	300
0	1	67	6	400
1	1	33	8	267
1	1	50	8	400
1	0	67	16/3	356

(1) BUSCLK will be undefined until a valid reference clock is available at REFCLK. After applying REFCLK, the PLL requires stabilization time to achieve phase lock.

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK stop	1	0	$V_{X, STOP}$	$V_{X, STOP}$
Normal	1	1	PACLK/PLLCLK/REFCLK(1)	PACLKB/PLLCLKB/REFCLKB

(1) Depending on the state of S0, S1, and S2

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}	Supply voltage range(2)	–0.5 V to 4 V
V_O	Output voltage range at any output terminal	–0.5 V to V_{DD} + 0.5 V
V_I	Input voltage rangeat any input terminal	–0.5 V to V_{DD} + 0.5 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C(1)	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.135	3.3	3.465	V
V_{IH}	High-level input voltage (CMOS)	$0.7 \times V_{DD}$			V
V_{IL}	Low-level input voltage (CMOS)			$0.3 \times V_{DD}$	V
	Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_{c(PD)}$		$0.5 \times t_{c(PD)}$	V
V_{IL}	REFCLK low-level input voltage			$0.3 \times V_{DD}IR$	V
V_{IH}	REFCLK high-level input voltage	$0.7 \times V_{DD}IR$			V
V_{IL}	Input signal low voltage (STOPB)			$0.3 \times V_{DD}IPD$	V
V_{IH}	Input signal high voltage (STOPB)	$0.7 \times V_{DD}IPD$			V
	Input reference voltage for (REFCLK) (VDDIR)	1.235		3.465	V
	Input reference voltage for (PCLKM and SYSCLKN) (VDDIPD)	1.235		3.465	V
I_{OH}	High-level output current			–16	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature	–40		85	°C

TIMING REQUIREMENTS

		MIN	MAX	UNIT
$t_{c(in)}$	Input cycle time	10	40	ns
	Input cycle-to-cycle jitter		250	ps
	Input duty cycle over 10,000 cycles	40%	60%	
f_{mod}	Input frequency modulation,	30	33	kHz
	Modulation index, nonlinear maximum 0.5%		0.6%	
	Phase detector input cycle time (PCLKM and SYNCLKN)	30	100	ns
SR	Input slew rate	1	4	V/ns
	Input duty cycle (PCLKM and SYNCLKN)	25%	75%	

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
$V_{O(STOP)}$	Output voltage during CLK Stop (STOPB = 0)		See Figure 1		1.1		2	
$V_{O(X)}$	Output crossing-point voltage		See Figure 1 and Figure 6		1.3		1.8	V
V_O	Output voltage swing		See Figure 1		0.4		0.6	V
V_{IK}	Input clamp voltage		VDD = 3.135 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		See Figure 1				2	V
			V_{DD} = min to max,	I_{OH} = –1 mA	V_{DD}– 0.1			
			V_{DD} = 3.135 V,	I_{OH} = –16 mA	2.4			
V_{OL}	Low-level output voltage		See Figure 1		1			V
			V_{DD} = min to max,	I_{OH} = 1 mA			0.1	
			V_{DD} = 3.135 V,	I_{OH} = 16 mA			0.5	
I_{OH}	High-level output current		V_{DD} = 3.135 V,	V_O = 1 V	–32	–52		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		–51		
			V_{DD} = 3.465 V,	V_O = 3.135 V		–14.5	–21	
I_{OL}	Low-level output current		V_{DD} = 3.135 V,	V_O = 1.95 V	43	61.5		mA
			V_{DD} = 3.3 V,	V_O = 1.65 V		65		
			V_{DD} = 3.465 V,	V_O = 0.4 V		25.5	36	
I_{OZ}	High-impedance-state output current		S0 = 0, S1 = 1				±10	µA
$I_{OZ(STOP)}$	High-impedance-state output current during CLK stop		Stop = 0, V_O = GND or V_{DD}				±100	µA
$I_{OZ(PD)}$	High-impedance-state output current in power-down state		PWRDNB = 0, V_O = GND or V_{DD}		–10		100	µA
I_{IH}	High-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V,	V_I = V_{DD}			10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1					10	
I_{IL}	Low-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V,	V_I = 0			–10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1					–10	
Z_O	Output impedance	High state	R_I at I_O– 14.5 mA to –16.5 mA		15	35	50	Ω
		Low state	R_I at I_O 14.5 mA to 16.5 mA		11	17	35	
	Reference current	VDDIR, VDDIPD	V_{DD} = 3.465 V	PWRDNB = 0			50	µA
				PWRDNB = 1			0.5	mA
C_I	Input capacitance		V_I = V_{DD} or GND			2		pF
C_O	Output capacitance		V_O = V_{DD} or GND			3		pF
$I_{DD(PD)}$	Supply current in pwoer-down state		REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1				100	µA
$I_{DD(CLKSTOP)}$	Supply current in CLK stop state		BUSCLK configured for 400 MHz				30	mA
$I_{DD(NORMAL)}$	Supply current in normal state		BUSCLK = 400 MHz				70	mA

(1) V_{DD} refers to any of the following; V_{DD}, V_{DD}IPD, V_{DD}IR, V_{DD}O, V_{DD}C, and V_{DD}P
(2) All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
$t_{c(out)}$	Clock output cycle time				2.5		3.75	ns
$t_{(jitter)}$	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	Infinite and stopped phase alignment	267 MHz	See Figure 3			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
$t_{(phase)}$	Phase detector phase error for distributed loop			Static phase error[(2)]	–100		100	ps
$t_{(phase,\ SSC)}$	PLL output phase error when tracking SSC			Dynamic phase error[(2)]	–100		100	ps
	Output duty cycle over 10,000 cycles			See Figure 4	45%		55%	
$t_{(DC,\ err)}$	Output cycle-to-cycle duty cycle error	Infinite and stopped phase alignment	267 MHz	See Figure 5			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
t_r, t_f	Output rise and fall times (measured at 20%–80% of output voltage)			See Figure 7	160		400	ps
Δt	Difference between rise and fall times on a single device (20%–80%) $\lvert t_f - t_r \rvert$			See Figure 7			100	ps

(1) All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
(2) Assured by design

STATE TRANSITION LATENCY SPECIFICATIONS

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB↑ to CLK/CLKB output settled (excluding $t_{(DISTLOCK)}$)	Powerdown	Normal	See Figure 8			3	ms
	Delay time, PWRDNB↑ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, power up to CLK/CLKB output settled	V_{DD}	Normal	See Figure 8			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLK/CLKB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 9			1	ms
$t_{(CLKON)}$	STOPB↑ to CLK/CLKB glitch-free clock edges	CLK Stop	Normal	See Figure 10			10	ns
$t_{(CLKSETL)}$	STOPB↑ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 10			20	cycles
$t_{(CLKOFF)}$	STOPB↓ to CLK/CLKB output disabled	Normal	CLK Stop	See Figure 10			5	ns
$t_{(powerdown)}$	Delay time, PWRDNB↓ to the device in the power-down mode	Normal	Powerdown	See Figure 8			1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 10			100	µs
$t_{(ON)}$	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK Stop	See Figure 10	100			ms
$t_{(DISTLOCK)}$	Time from when CLK/CLKB output is settled to when the phase error between SYNCLKN and PCLKM falls within $t_{(phase)}$	Unlocked	Locked				5	ms

(1) All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

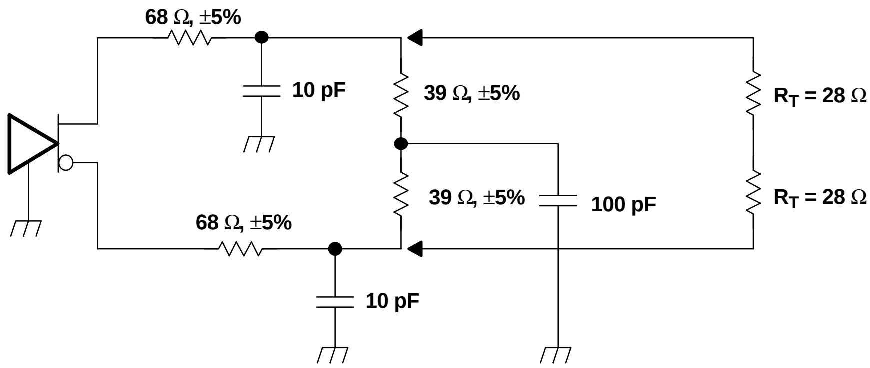
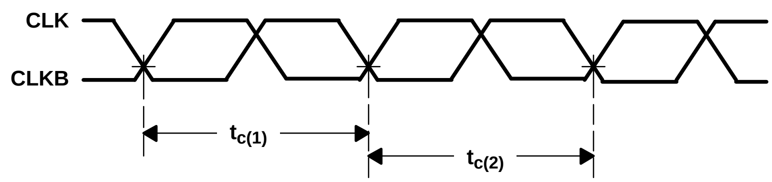
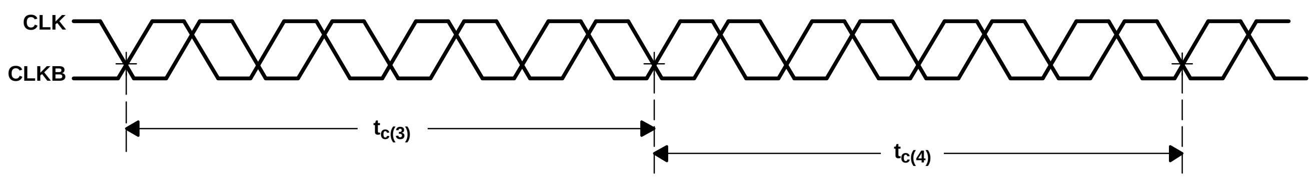


Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, $V_{O(X)}$, V_O, V_{OH}, V_{OL})



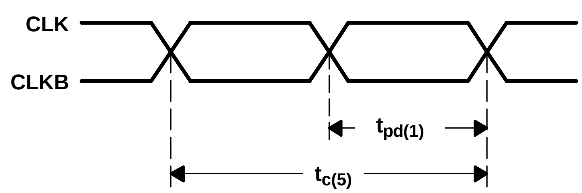
Cycle-to-cycle jitter = | $t_{c(1)} - t_{c(2)}$| over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



Cycle-to-cycle jitter = | $t_{c(3)} - t_{c(4)}$| over 10000 consecutive cycles

Figure 3. Short Term Cycle-to-Cycle Jitter Over Four Cycles



Duty cycle = ($t_{pd(1)}/t_{c(5)}$)

Figure 4. Output Duty Cycle

PARAMETER MEASUREMENT INFORMATION (continued)

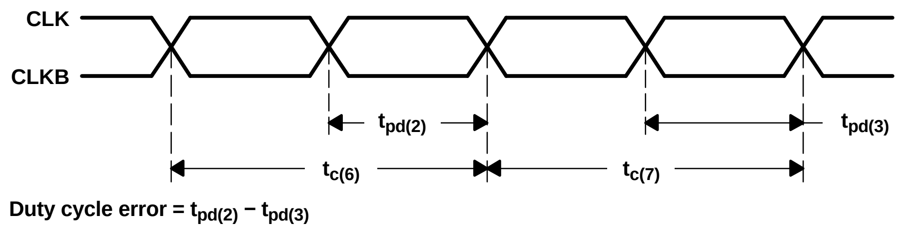


Figure 5. Duty Cycle Error (Cycle-to-Cycle)

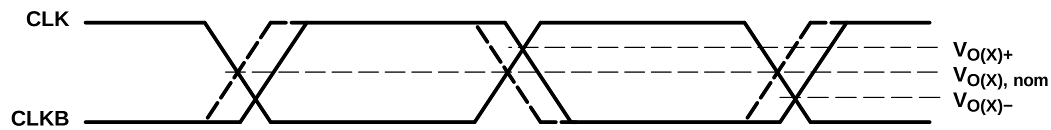


Figure 6. Crossing-Point Voltage

Figure 7. Voltage Waveforms

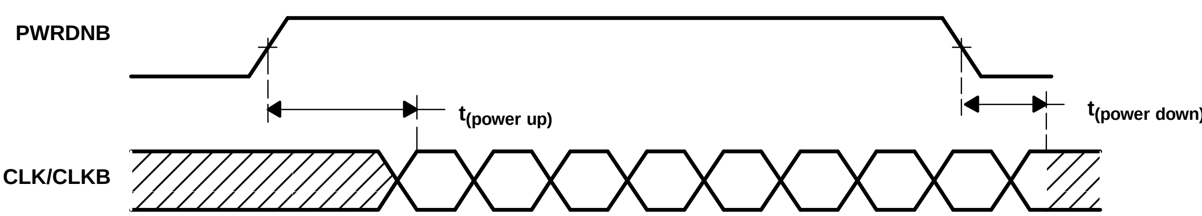


Figure 8. PWRDNB Transition Timings

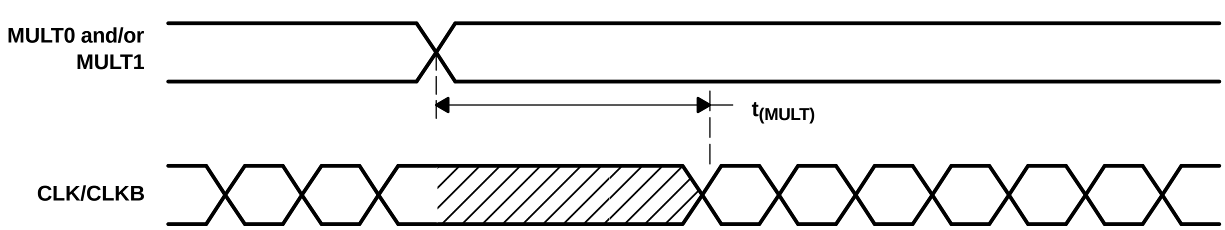
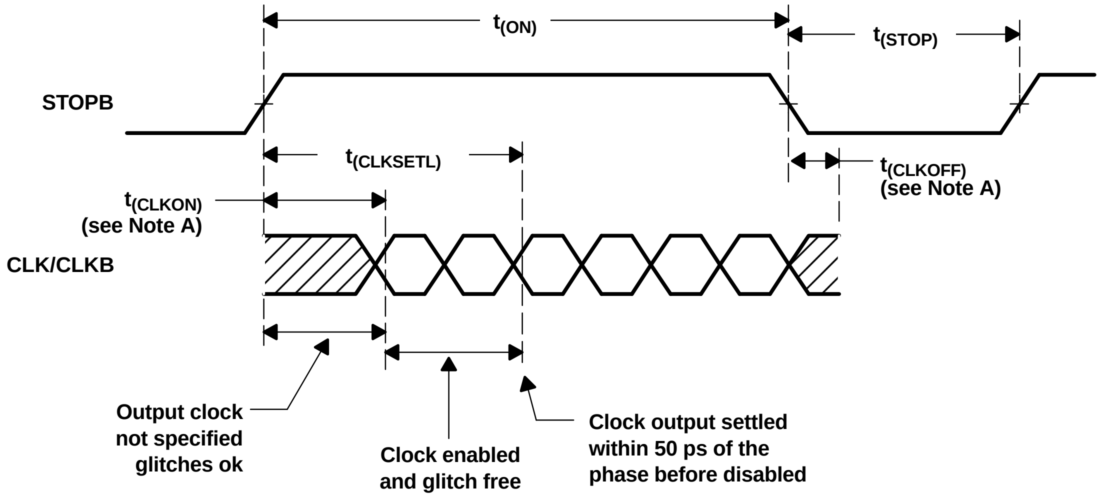


Figure 9. MULT Transition Timings

PARAMETER MEASUREMENT INFORMATION (continued)



A. $V_{ref} = V_O \pm 200$ mV

Figure 10. STOPB Transition Timings

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCR83ADBQ	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCR83A	Samples
CDCR83ADBQG4	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCR83A	Samples
CDCR83ADBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCR83A	Samples
CDCR83ADBQRG4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCR83A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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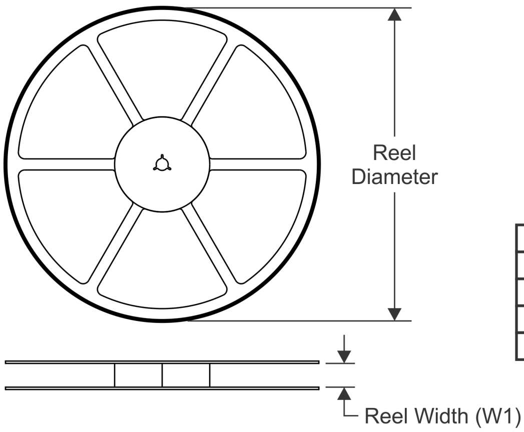
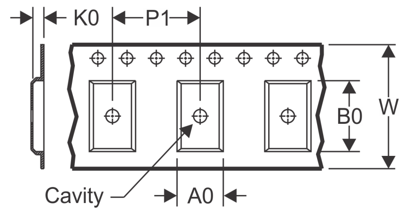
TAPE AND REEL INFORMATION

REEL DIMENSIONS

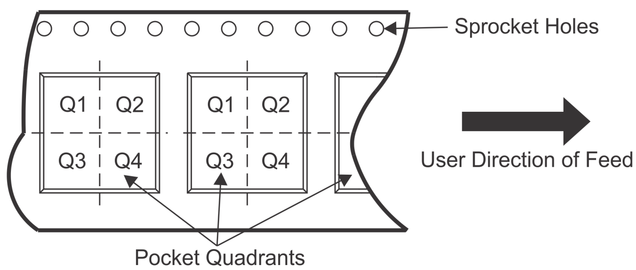


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

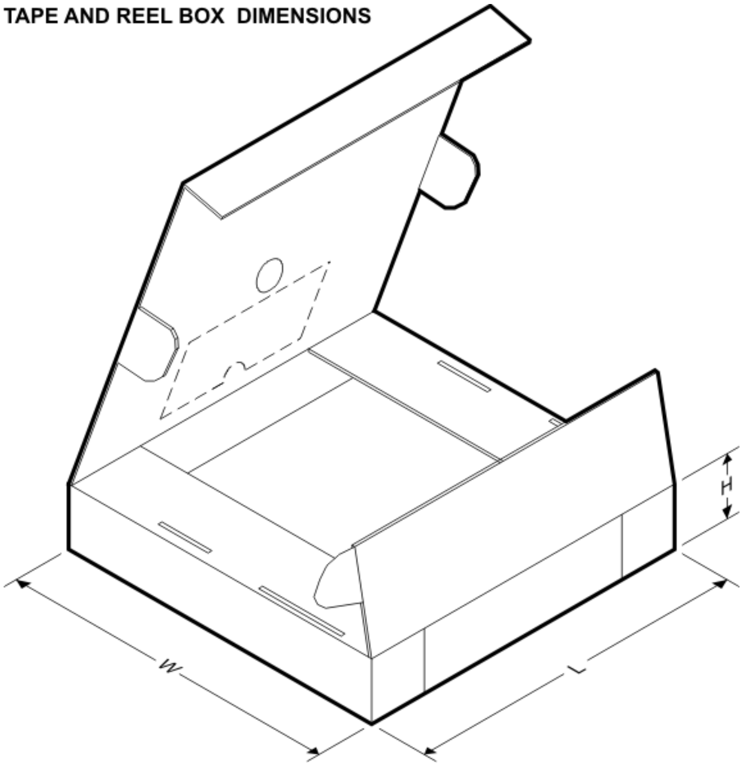
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCR83ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

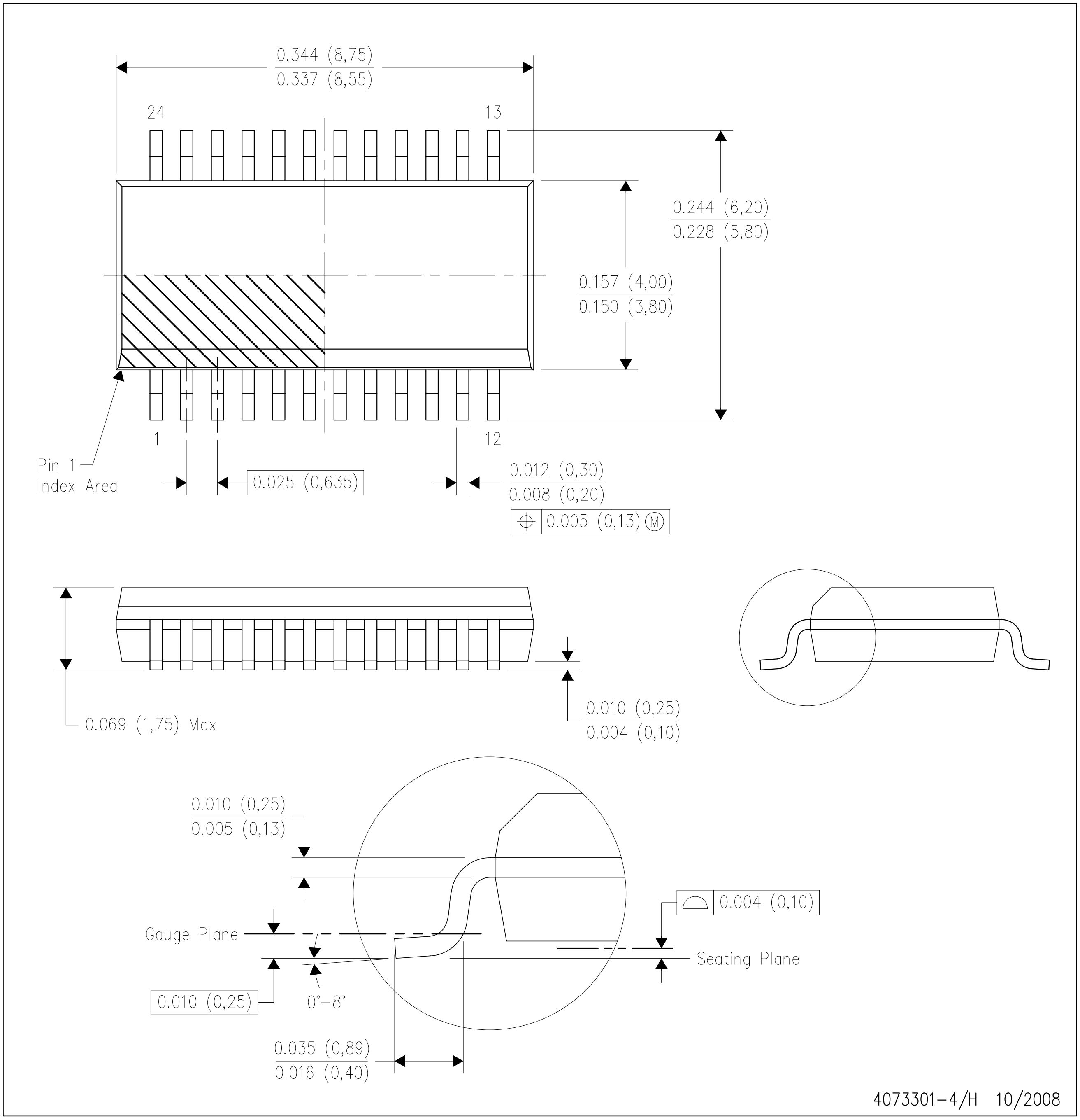
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

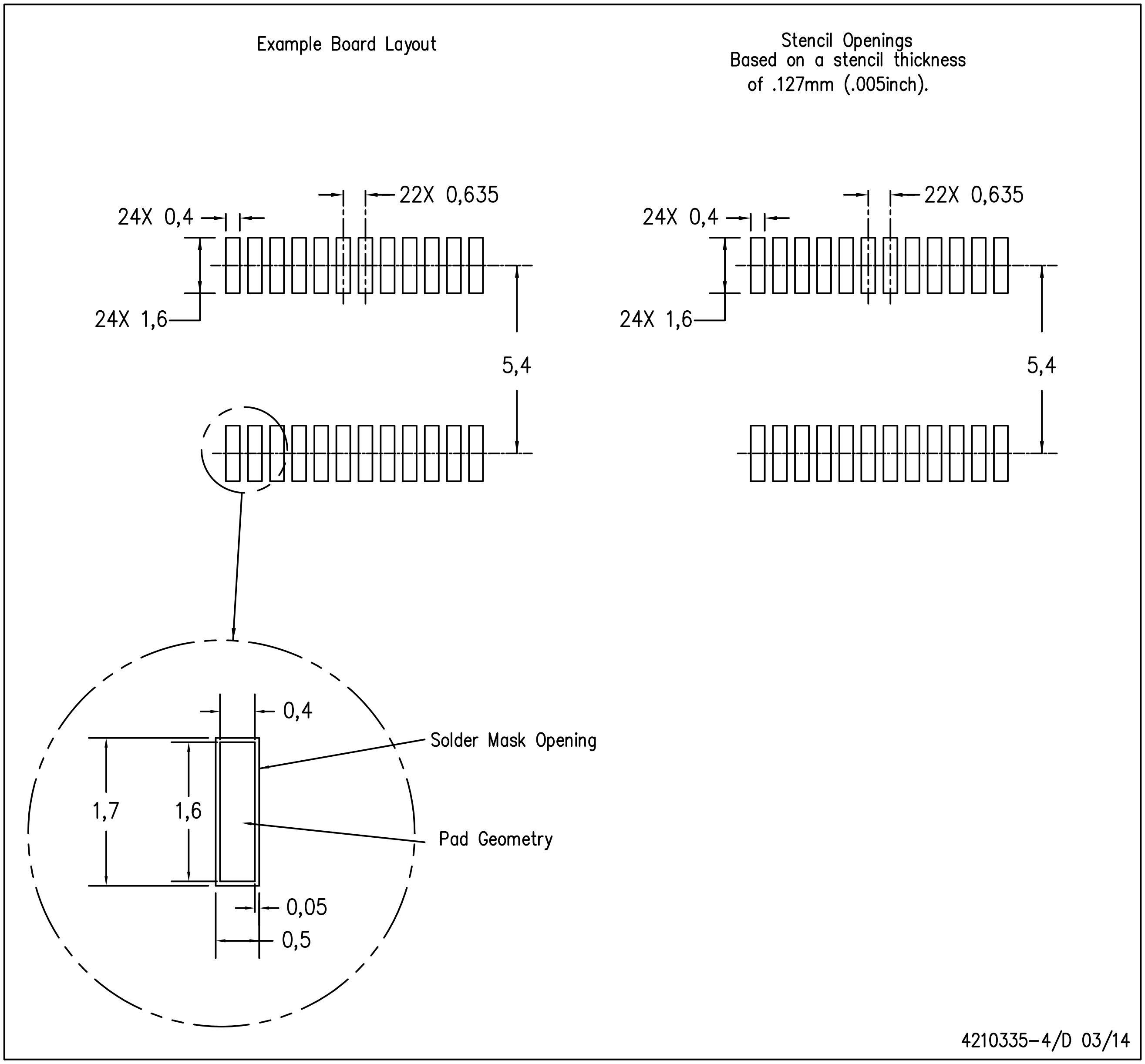
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCR83ADBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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