CDCUN1208LP 400 MHz Low Power 2:8 Fan-Out Buffer with Universal Inputs and Outputs

1 Features

- Support PCIE gen1, gen2, gen3
- Configuration Options (via pins or SPI/I^{2}C):
  - Input Type (HCSL, LVDS, LVCMOS)
  - Output Type (HCSL, LVDS, LVCMOS)
  - Signal Edge Rate (Slow, Medium, Fast)
  - Clock Input Divide Value (/1, /2, /4, /8) – IN2 Only
- Low Power Consumption and Power Management Features Including 1.8V Operation and Output Enable Control
- Integrated Voltage Regulators Improve PSNR
- Excellent Additive Jitter Performance
  - 200 fs RMS (10 kHz to 20 MHz), LVDS at 100 MHz
  - 160 fs RMS (10 kHz to 20 MHz), HCSL at 100 MHz
- Maximum Operating Frequency:
  - Differential Mode: up to 400 MHz
  - LVCMOS Mode: up to 250 MHz
- ESD Protection Exceeds 2 kV HBM, 500 V CDM
- Industrial Temperature Range (–40°C to 85°C)
- Wide Supply Range (1.8 V, 2.5 V, or 3.3 V)

2 Applications

- Communications Systems (Ethernet, PCI Express)
- Computing Systems (Ethernet, PCIe, USB)
- Consumer (Set top boxes, video equipment)
- Office Automation

3 Description

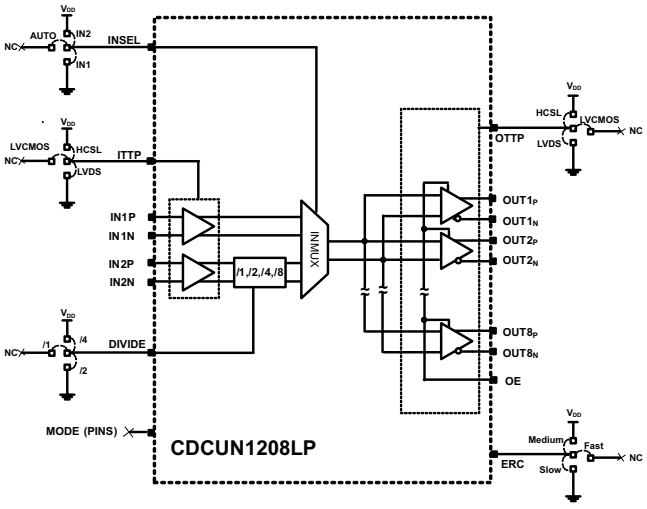
The CDCUN1208LP is a 2:8 fan-out buffer featuring a wide operating supply range, two universal differential/single-ended inputs, and universal outputs (HCSL, LVDS, or LVCMOS) with edge rate control. The clock buffer supports PCIE gen1, gen2 and gen3. One of the device inputs includes a divider that provides divide values of /1, /2, /4, or /8. The CDCUN1208LP is offered in a 32 pin QFN package reducing the solution footprint. The device is flexible and easy to use. The state of certain pins determines device configuration at power up. Alternately, the CDCUN1208LP provides a SPI/I^{2}C port with which a host processor controls device settings. The CDCUN1208LP delivers excellent additive jitter performance, and low power consumption. The output section includes four dedicated supply pins enabling the operation of output ports from different power supply domains. This provides the ability to clock devices switching at different LVCMOS levels without the need for external logic level translation circuitry.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCUN1208LP	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Pin Configuration Overview



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2013) to Revision C **Page**

- Changed Added *Device Information Table*, *ESD Ratings* table*Application and Implementation*; *Power Supply Recommendations*; *Layout; Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Added $\Delta V/\Delta T^2$ to the *Recommended Operating Conditions* table. ... 6
- Added text "note that CDCUN1208LP supports only single-device" to the first paragraph of *SPI Communication* ... 30
- Added text "At no time should the clock be toggled while SCS is high. CDCUN1208LP should always be used in single-slave SPI configuration." to *Writing to the CDCUN1208LP* ... 31
- Added text "At no time should the clock be toggled while SCS is high. CDCUN1208LP should always be used in single-slave SPI configuration." to *Reading from the CDCUN1208LP* ... 31

Changes from Revision A (January 2013) to Revision B **Page**

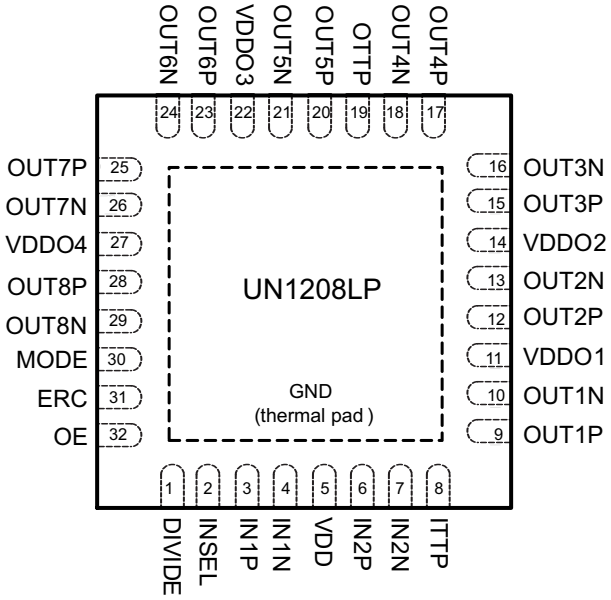
- Added slew rate note to RECOMMENDED OPERATING CONDITIONS ... 6
- Changed $V_{IOPEN1.8}$ from 0.9 V to 0.75 V in *Digital Input Electrical Characteristics – OE (SCL), INSEL, ITTP, OTTP, DIVIDE (SDA/MOSI), ERC(ADDR/CS), Mode* ... 7
- Changed Fast to Medium and Medium to Fast in *Figure 28* ... 24

Changes from Original (May 2012) to Revision A **Page**

- Added Feature:160 fs RMS (10kHz-20MHz), HCSL at 100MHz ... 1
- Added *Features*: Support PCIE gen1, gen2, gen3 ... 1
- Added text to the Description: "The clock buffer supports PCIE gen1, gen2 and gen3." ... 1
- Added text to the Clock Output Buffer Characteristics table: "Supporting PCIE gen1, gen2, gen3." ... 10
- Changed Table 4 From: DISABLED To: DISABLED in Tri_State ... 25
- Changed Table 11 From: Disabled To: Disabled in Tri_State for OUTx_PD ... 37
- Added text and Figure 41 to the *PCI Express Applications* section. ... 39

5 Pin Configuration and Functions

RHB Package
VQFN 32-Pin
Top View



Pin Functions[1]

PIN		I/O	DESCRIPTION
NAME	NUMBER		
GND	Thermal Pad		Power supply ground and thermal relief
VDD	5		Device Power Supply, Provides power to the input section and clock distribution section. Use a power supply voltage that corresponds to the switching levels of clock input(s) (i.e. 1.8V, 2.5V, or 3.3V).
MODE	30		**Device Control Mode Select** OPEN = Device Configured via pins (Pin Mode) HIGH = Device Configured via I^2C LOW = Device Configured via SPI Note: For information on control via the serial interface (I^2C/ SPI), see DEVICE CONTROL USING THE HOST INTERFACE section.
DIVIDE	1		**Input Divider Pin Control** (HIGH = /4, LOW = /2, OPEN = /1)
OE	32		**Device Output Enable** HIGH = Enable, LOW = Disable
ERC	31		**Output Edge Rate Control** HIGH = Medium, LOW = Slow, OPEN = Fast
INSEL	2		Input Multiplexer Control
ITTP	8		Input Type Select (HIGH = HCSL, LOW = LVDS, OPEN = LVCMOS)
IN1P	3		Universal Input 1 – Positive Terminal
IN1N	4		Universal Input 1 – Negative Terminal, Ground if using IN1 in single-ended mode
IN2P	6		Universal Input 2 – Positive Terminal
IN2N	7		Universal Input 2 – Negative Terminal, Ground if using IN2 in single-ended mode
OTTP	19		Output Type Select (HIGH = HCSL, LOW = LVDS, OPEN = LVCMOS)
OUT1P	9		Output 1 – Positive Terminal
OUT1N	10		Output 1 – Negative Terminal

(1) This pin list applies to operation of the device in pin mode. In host mode, certain pins take on an alternate function as outlined in Table 8.

Pin Functions[1] (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VDDO1	11		Output Power Supply – OUT1, OUT2
OUT2P	12		Output 2 – Positive Terminal
OUT2N	13		Output 2 – Negative Terminal
VDDO2	14		Output Power Supply – OUT3, OUT4; Output bank OUT1 – OUT4 regulator power supply (apply power if any of OUT1 – OUT4 are needed)
OUT3P	15		Output 3 – Positive Terminal
OUT3N	16		Output 3 – Negative Terminal
OUT4P	17		Output 4 – Positive Terminal
OUT4N	18		Output 4 – Negative Terminal
OUT5P	20		Output 5 – Positive Terminal
OUT5N	21		Output 5 – Negative Terminal
VDDO3	22		Output Power Supply - OUT5, OUT6
OUT6P	23		Output 6 – Positive Terminal
OUT6N	24		Output 6 – Negative Terminal
OUT7P	25		Output 7 – Positive Terminal
OUT7N	26		Output 7 – Negative Terminal
VDDO4	27		Output Power Supply – OUT7, OUT8 Output bank OUT5 – OUT8 regulator power supply (apply power if any of OUT5 – OUT8 are needed)
OUT8P	28		Output 8 – Positive Terminal
OUT8N	29		Output 8 – Negative Terminal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DDxx}	Supply voltage range (2)	–0.5	4.6	V
V_{IN}	Input voltage range (3)	–0.5	V_{DDIx} + 0.5	V
V_{OUT}	Output voltage range (3)	–0.5	V_{DDOx} + 0.5	V
I_{IN}	Input current	20		mA
I_{OUT}	Output current	50		°C mA
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages must be supplied simultaneously
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = –40°C TO 85°C

			MIN	NOM	MAX	UNIT
POWER SUPPLIES (1) (2)						
V_{DD}	DC Power Supply - Core	1.8V Mode	1.7	1.8	1.9	V
V_{DDOx}	DC Power Supply - Output	1.8V Mode	1.7	1.8	1.9	V
V_{DD}	DC Power Supply - Core	2.5V Mode	2.375	2.5	2.625	V
V_{DDOx}	DC Power Supply - Output	2.5V Mode	2.375	2.5	2.625	V
V_{DD}	DC Power Supply - Core	3.3V Mode	2.97	3.3	3.63	V
V_{DDOx}	DC Power Supply - Output	3.3V Mode	2.97	3.3	3.63	V
$\Delta V/\Delta T^2$	Core Power Supply Slew Rate	0.4V to 1.8V × 0.8 (in all Voltage Modes)	6500			V/s
TEMPERATURE						
T_A	Free- Air Temperature		–40		85	°C

(1) For proper device operation, the core power supply voltage (pin 5) must be applied either before the application of any output power supply or simultaneously with the application of the output power supplies. The application of an output power supply prior to the application of the core power supply could result in improper device behavior.
(2) A minimum V_{DD} slew rate of 6500V/s should be obtained to ensure proper device functionality in Pin Mode. If the ambient temperature of the device is >0°C, the slew rate can be as slow as 5000V/s. In Host Mode (I^2C/SPI), the V_{DD} slew rate is not limited, if the Reset bit gets toggled after V_{DD} ramp.

6.4 Thermal Information

THERMAL METRIC(1)		CDCUN1208LP RHB Package 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Digital Input Electrical Characteristics – OE (SCL), INSEL, ITTP, OTTP, Divide (SDA/MOSI), ERC(ADDR/CS), Mode

T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS INPUT						
$V_{IL1.8}$	Low level LVCMOS input voltage	V_{DD} = 1.8 V			0.7	V
$V_{IH1.8}$	High level LVCMOS input voltage	V_{DD} = 1.8 V	1.35			V
$V_{IOPEN1.8}$	OPEN level LVCMOS input voltage	V_{DD} = 1.8 V	0.75		1.2	V
$V_{IL2.5}$	Low level LVCMOS input voltage	V_{DD} = 2.5 V			0.7	V
$V_{IH2.5}$	High level LVCMOS input voltage	V_{DD} = 2.5 V	1.71			V
$V_{IOPEN2.5}$	OPEN level LVCMOS input voltage	V_{DD} = 2.5 V	1.0		1.6	V
$V_{IL3.3}$	Low level LVCMOS input voltage	V_{DD} = 3.3 V			1.0	V
$V_{IH3.3}$	High level LVCMOS input voltage	V_{DD} = 3.3 V	2.3			V
$V_{IOPEN3.3}$	OPEN level LVCMOS input voltage	V_{DD} = 3.3 V	1.3		1.9	V
I_{IL}	Low level LVCMOS input current	$V_{DD} = V_{DDmax}$, V_{ILCMOS} = 0 V			–120	µA
I_{IH}	High level LVCMOS input current	$V_{DD} = V_{DDmax}$, V_{IHCMOS} = 1.9 V			65	µA
C_I	LVCMOS Input capacitance			6		pF
V_{IK}	Digital input clamp voltage	V_{DD} = 1.7V, I_I = –18 mA			–1.2	V

6.6 Universal Input (IN1, IN2) Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINGLE-ENDED MODE						
$f_{IN1,2}$	Input frequency	Single ended(1)	0.008		250	MHz
V_{IH}	Input voltage - high	250 MHz	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage - low	250 MHz			0.2 × V_{DD}	V
DIFFERENTIAL MODE						
f_{INDIFF}	Input frequency		0.008		400	MHz
$\lvert V_{IN-DIFF} \rvert$	Input swing	V_{DD} = 2.5 V, 3.3 V	0.15		1.6	V
		V_{DD} = 1.8 V	0.15		1	V
V_{CM}	Input common mode voltage	ITTP = LVDS, V_{DD} = 3.3 V	0.8		2.5	V
		ITTP = LVDS, V_{DD} = 2.5 V, 1.8 V	0.8		V_{DD} – 0.3	
		ITTP = HCSL	–0.15		0.75	
GENERAL CHARACTERISTICS						
I_{IH}	Input current - high	V_{DD} = 3.63 V, V_{IH} = 3.63 V			30	µA
I_{IL}	Input current - low	V_{DD} = 3.63 V, V_{IL} = 0 V			–30	µA
ΔV/ΔT	Input edge rate	20%–80%	0.75			V/ns
DC_{IN}	Input duty cycle		40		60%	
C_{IN}	Input capacitance			3.5		pF

(1) When using an input in single-ended mode, ground the negative terminal (IN1N and/or IN2N) and drive the positive terminal (IN1P and/or IN2P).

6.7 Clock Output Buffer Characteristics (Output Mode = LVDS)

Unless otherwise noted, V_{DDOX} = 1.8V, 2.5V, 3.3V; T_A = –40°C to 85°C. See Figure 15, Figure 16, and Figure 17.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		0.008		400	MHz
V_{CM}	Output common mode voltage, VDDOx = 2.5/3.3 V	R_L = 100 Ω	1.125	1.2	1.275	V
	Output common mode voltage, VDDOx = 1.8 V	R_L = 100 Ω		0.9		V
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω, single-ended Pk-Pk	250	400	550	mV
ΔV_{OD}	Change in magnitude of VOD for complementary output states	R_L = 100 Ω	–50		50	mV
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude VOD			20%	
V_{OS}	Output AC common mode	$V_{IN, DIFF, PP}$ = 0.9V, R_L = 100 Ω, 2 pF			150	mVP-P
T_{ADDJIT}	Additive jitter(1)	f_{out} = 100 MHz, 10k-20M integration bandwidth, R_L = 100Ω			200	fs, rms
		f_{out} = 400 MHz, 10k-20M integration bandwidth, R_L = 100Ω			180	
t_R/t_F	Output rise/fall time	ERC = Slow, 20% to 80%, Z_L = 100Ω, 1pF, V_{DDOx} = 3.3V		800		ps
		ERC = Slow, 20% to 80%, Z_L = 100Ω, 1pF, V_{DDOx} = 1.8V		700		
		ERC = Medium., 20% to 80%, Z_L = 100Ω, 1pF, V_{DDOx} = 3.3V		600		
		ERC = Medium., 20% to 80%, Z_L = 100Ω, 1pF, V_{DDOx} = 1.8V		500		
		ERC = Fast, 20% to 80%, Z_L = 100Ω, 1 pF		300		
ODC	Output Duty Cycle	50/50 Input duty cycle	45%		55%	
I_{SP} I_{SN}	Output Short Circuit Current (single ended)	Shorted to GND	-24		24	mA
$\|I_{PN}\|$	Output Short Circuit Current (differential)	Complementary outputs shorted together			12	mA
T_{DLYO}	Propagation Delay	ERC set to high rate. Input t_r, t_f > 0.6 V/ns, R_L = 100Ω, V_{DD} = 2.5V, 3.3V			3.3	ns
		ERC set to high rate. Input t_r, t_f > 0.6 V/ns, R_L = 100Ω, V_{DD} = 1.8V			3.8	
t_{SKEW}	Skew between outputs	ERC set to high rate. Input t_r, t_f > 0.6 V/ns, Equal VDDOx, R_L = 100Ω		35	50	ps
t_{OE}	Output enable to stable clock output	Pin mode. f_{out} = 100 MHz, device in active mode with outputs disabled, OE asserted		20		µs
t_{PD}	PD de-asserted to stable clock output	Host mode, f_{out} = 100 MHz, device in power down mode, PD de-asserted		20		µs
t_{PU}	Time from power applied to stable clock output(2)	Pin mode, f_{out} = 100 MHz, OE asserted, measured from time V_{DD} is valid to stable output.		1		ms

(1) t_{Rfin} = t_{Ffin} > 0.6 V/ns.
(2) Parameter depends significantly on power supply design and supply voltage rise time.

6.8 Clock Output Buffer Characteristics (Output Mode = HCSL)

Unless otherwise noted, V_{DDOx} = 1.8V, 2.5V, 3.3V; T_A = –40°C to 85°C. See Figure 18, Figure 19, and Figure 20. Supporting PCIE gen1, gen2, gen3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		0.008		400	MHz
Vmax	Absolute maximum output voltage(1)	See Figure 1			1.15	V
Vmin	Absolute minimum output voltage(2)	See Figure 1	–0.3			V
V_{OH}	Single ended output voltage – high(3)	R_L = single ended to GND = 50 Ω, C_L = 2pF, VDDOx = 2.5V, 3.3V See Figure 18	600			mV
		R_L = single ended to GND = 50 Ω, C_L = 2pF, VDDOx = 1.8V See Figure 18	550			
V_{OL}	Single ended output voltage – low(3)	R_L = single ended to GND = 50 Ω, C_L = 2pF, See Figure 18			150	mV
V_{CROSS}	Output crossing point voltage(3)	See Figure 1	250		550	mV
$V_{CROSS\Delta}$	V_{CROSS} Total variation(3)	See Figure 2			140	mV
V_{RB}	Ring back voltage margin(3)	See Figure 3	–100		100	mV
T_{STABLE}	Time before V_{RB} is Allowed(3),(4)	See Figure 3	500			ps
V_{OS}	Output AC common mode	$V_{IN, DIFF, PP}$ = 0.9V, R_L = single ended to GND = 50 Ω, 2 pF		75	125	mV_{P-P}
$T_{jitHCSL}$	Additive jitter, input set to HCSL(5)	f_{OUT} = 100 MHz, 10k-20M integration bandwidth. Differential Measurement			380	fs, rms
$T_{jitLVDS}$	Additive jitter, input set to LVDS(5)	f_{OUT} = 100 MHz, 10k-20M integration bandwidth. Differential Measurement			280	fs, rms
t_R/t_F	Output rise/fall time(6)	Slow, +150mV differential, See Figure 4, V_{DDOx} = 3.3V		300		ps
		Slow, +150mV differential, See Figure 4, V_{DDOx} = 1.8V		230		
		Med., +150mV differential, See Figure 4, V_{DDOx} = 3.3V		240		
		Med., +150mV differential, See Figure 4, V_{DDOx} = 1.8V		180		
		Fast, +150mV differential, See Figure 4		140		
TM_{RF}	Output rise/fall time matching	See Figure 5			20%	
ODC	Output duty cycle(7)	Differential Measurement, See Figure 6	45%		55%	
T_{DLYO}	Propagation delay	ERC set to high rate. Input t_r, t_f > 0.6 V/ns, V_{DD} = 2.5V, 3.3V			3.8	ns
		ERC set to high rate. Input t_r, t_f > 0.6 V/ns, V_{DD} = 1.8V			4.3	
t_{SKEW}	Skew between outputs(8)	Differential Measurement, Input t_r, t_f > 0.6 V/ns		35	50	ps
t_{OE}	Output enable to stable clock output	Pin mode, f_{out} = 100 MHz, device in active mode with outputs disabled, OE asserted		2		µs
t_{PD}	PD de-asserted to stable clock output	Host mode, f_{out} = 100 MHz, device in power down mode, PD de-asserted		15		µs
t_{PU}	Time from power applied to stable clock output(9)	Pin mode, f_{out} = 100 MHz, OE asserted, measured from time V_{DD} is valid to stable output		1		ms

(1) Single-ended measurement includes overshoot. Measurement is taken at load capacitors C_L (see Figure 18).
(2) Single-ended measurement, includes undershoot Measurement is taken at load capacitors C_L (see Figure 18).
(3) Measurement is taken at load capacitors C_L (see Figure 18). If VDDOx = 1.8V, the specified minimum V_{OH} is 550 mV.
(4) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range. See Figure 3.
(5) $t_{Rfin} = t_{Ffin} \geq 0.6$ V/ns.
(6) Measured from –150 mV to +150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. Slow is 0.53V/ns, medium is 1.05V/ns, and fast is 2.1V/ns. The PCIe CEM spec. has a window of 0.6V/ns to 4V/ns.
(7) Assumes input duty cycle = 50%.
(8) Skew measured between identical output types with identical loads, identical output power supplies, and identical edge rate settings.
(9) Parameter depends significantly on power supply design and supply voltage rise time.

6.9 Clock Output Buffer Electrical Characteristics (Output Mode = LVCMOS)

Unless otherwise noted, V_{DDOx} as shown in Table sections, T_A = –40°C to 85°C. ERC = Fast. For test configurations, see Figure 21 and Figure 22.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3V MODE						
f_{out}	Output frequency range		0.0008		250	MHz
V_{OH}	LVCMOS High-level output voltage	V_{DDOx} = 2.97 V, I_{OH} = –0.1 mA (All ERC Settings)	2.9			V
		V_{DDOx} = 2.97 V, I_{OH} = –5 mA (ERC = SLOW)	2.4			V
		V_{DDOx} = 2.97 V, I_{OH} = –8 mA (ERC = MED, FAST)				
		V_{DDOx} = 2.97 V, I_{OH} = –6 mA (ERC = SLOW)	2.2			V
		V_{DDOx} = 2.97 V, I_{OH} = –10 mA (ERC = MED)				
		V_{DDOx} = 2.97 V, I_{OH} = –12 mA (ERC = FAST)				
V_{OL}	LVCMOS Low-level output voltage	V_{DDOx} = 2.97 V, I_{OL} = 0.1 mA (All ERC Settings)			0.1	V
		V_{DDOx} = 2.97 V, I_{OL} = 5 mA (ERC = SLOW)			0.5	V
		V_{DDOx} = 2.97 V, I_{OL} = 8 mA (ERC = MED, FAST)				
		V_{DDOx} = 2.97 V, I_{OL} = 6 mA (ERC = SLOW)			0.8	V
		V_{DDOx} = 2.97 V, I_{OL} = 10 mA (ERC = MED)				
		V_{DDOx} = 2.97 V, I_{OL} = 12 mA (ERC = FAST)				
I_{OH}	LVCMOS High-level output current	V_{DDOx} = 3.3 V, V_O = 0.5 V; T_A = 25°C		–73		mA
		V_{DDOx} = 3.3 V, V_O = 1.0 V; T_A = 25°C		–64		
		V_{DDOx} = 3.3 V, V_O = 1.65 V; T_A = 25°C		–49		
I_{OL}	LVCMOS Low-level output current	V_{DDOx} = 3.3 V, V_O = 2.8 V; T_A = 25°C		78		mA
		V_{DDOx} = 3.3 V, V_O = 2.3 V; T_A = 25°C		72		
		V_{DDOx} = 3.3 V, V_O = 1.65 V; T_A = 25°C		58		
t_{PLH}, t_{PHL}	Propagation Delay			5		ns
$t_{SLEW-RATE}$	Output rise/fall slew rate	ERC = Slow, 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		1.2		V/ns
		ERC = Medium 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		3		
		ERC = Fast, 20% to 80%, f_{out} = 250 MHz, C_L = 8 pF		6		
$t_{jitt-add}$	Additive Jitter	f_{OUT} = 100 MHz, 10k-20M integration bandwidth			280	fs
$t_{sk(o)}$	Output Skew(1)				90	ps
odc	Output Duty Cycle(2), (3)	f_{OUT} = 100 MHz; Pdiv = 1	45%		55%	
t_{OE}	Output enable to stable clock output	Pin mode. f_{out} = 100 MHz, device in active mode with outputs disabled, OE asserted		2		µs
t_{PD}	PD de-asserted to stable clock output	Host mode, f_{out} = 100 MHz, device in power down mode, PD de-asserted		10		µs
t_{PU}	Time from power applied to stable clock output(4)	Pin mode, f_{out} = 100 MHz, OE asserted, measured from time V_{DD} is valid to stable output.		1		ms

(1) The $t_{sk(o)}$ specification is only valid for equal loading with identical edge rates and output supply voltages..
(2) Assumes 50% duty cycle at the input(s)
(3) odc depends on output rise and fall time (t_R/t_F).
(4) Parameter depends significantly on power supply design and supply voltage rise time.

6.10 Clock Output Buffer Electrical Characteristics (Output Mode = LVCMOS) (Continued)

Unless otherwise noted, V_{DDOx} as shown in Table sections, T_A = –40°C to 85°C. ERC = Fast. For test configurations, see Figure 21 and Figure 22.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.5V MODE						
f_{out}	Output frequency range		0.0008		250	MHz
V_{OH}	LVCMOS High-level output voltage	V_{DDOx} = 2.375 V, I_{OH} = -0.1 mA (All ERC Settings)	2.2			
		V_{DDOx} = 2.375 V, I_{OH} = -4 mA (ERC = SLOW)	1.7			V
		V_{DDOx} = 2.375 V, I_{OH} = - 6 mA (ERC = MED, FAST)				
		V_{DDOx} = 2.375 V, I_{OH} = -5 mA (ERC = SLOW)	1.6			V
		V_{DDOx} = 2.375 V, I_{OH} = - 8 mA (ERC = MED, FAST)				
V_{OL}	LVCMOS Low-level output voltage	V_{DDOx} = 2.375 V, I_{OL} = 0.1 mA (All ERC Settings)			0.1	V
		V_{DDOx} = 2.375 V, I_{OH} = 4 mA (ERC = SLOW)			0.5	V
		V_{DDOx} = 2.375 V, I_{OH} = 6 mA (ERC = MED, FAST)				
		V_{DDOx} = 2.375 V, I_{OH} = 5 mA (ERC = SLOW)			0.7	V
		V_{DDOx} = 2.375 V, I_{OL} = 10 mA (ERC = MED, FAST)				
I_{OH}	LVCMOS High-level output current	V_{DDOx} = 2.5 V, V_O = 0.5 V; T_A = 25°C		–45		mA
		V_{DDOx} = 2.5 V, V_O = 0.9 V; T_A = 25°C		–39		
		V_{DDOx} = 2.5 V, V_O = 1.25 V; T_A = 25°C		–32		
I_{OL}	LVCMOS Low-level output current	V_{DDOx} = 2.5 V, V_O = 2.0 V; T_A = 25°C		50		mA
		V_{DDOx} = 2.5 V, V_O = 1.65 V; T_A = 25°C		47		
		V_{DDOx} = 2.5 V, V_O = 1.25 V; T_A = 25°C		40		
t_{PLH}, t_{PHL}	Propagation delay			5.5		ns
$t_{SLEW-RATE}$	Output rise/fall slew rate	ERC = Slow, 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		0.8		V/ns
		ERC = Medium 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		1.4		
		ERC = Fast, 20% to 80%, f_{out} = 250 MHz, C_L = 8 pF		4		
$t_{jitt-add}$	Additive jitter	f_{OUT} = 100 MHz, 10k-20M integration bandwidth			280	fs
$t_{sk(o)}$	Output skew(1)				90	ps
odc	Output Duty Cycle(2)(3)	f_{OUT} = 100 MHz; Pdiv = 1	45%		55%	
t_{OE}	Output enable to stable clock output	Pin mode. f_{out} = 100 MHz, device in active mode with outputs disabled, OE asserted		2		µs
t_{PD}	PD de-asserted to stable clock output	Host mode, f_{out} = 100 MHz, device in power down mode, PD de-asserted		10		µs
t_{PU}	Time from power applied to stable clock output(4)	Pin mode, f_{out} = 100 MHz, OE asserted, measured from time V_{DD} is valid to stable output.		1		ms

(1) The $t_{sk(o)}$ specification is only valid for equal loading with identical edge rates and output supply voltages..
(2) Assumes 50% duty cycle at the input(s)
(3) odc depends on output rise and fall time (t_R/t_F).
(4) Parameter depends significantly on power supply design and supply voltage rise time.

6.11 Clock Output Buffer Electrical Characteristics (Output Mode = LVCMOS) (Continued)

Unless otherwise noted, V_{DDOx} as shown in Table sections, T_A = –40°C to 85°C. ERC = Fast. For test configurations, see Figure 21 and Figure 22.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
1.8V MODE						
f_{out}	Output Frequency Range		0.0008		250	MHz
V_{OH}	LVCMOS High-level output voltage	V_{DDOx} = 1.7 V, I_{OH} = –0.1 mA (All ERC Settings)	1.6			
		V_{DDOx} = 1.7 V, I_{OH} = –1.5 mA (ERC = SLOW)	1.4			V
		V_{DDOx} = 1.7 V, I_{OH} = –3 mA (ERC = MED)				
		V_{DDOx} = 1.7 V, I_{OH} = –4 mA (ERC = FAST)				
		V_{DDOx} = 1.7 V, I_{OH} = –3 mA (ERC = SLOW)	1.1			V
		V_{DDOx} = 1.7 V, I_{OH} = –5 mA (ERC = MED)				
		V_{DDOx} = 1.7 V, I_{OH} = –8 mA (ERC = FAST)				
V_{OL}	LVCMOS Low-level output voltage	V_{DDOx} = 1.7 V, I_{OL} = 0.1 mA (All ERC Settings)			0.1	V
		V_{DDOx} = 1.7 V, I_{OL} = 2 mA (ERC = SLOW)			0.3	V
		V_{DDOx} = 1.7 V, I_{OL} = 3 mA (ERC = MED)				
		V_{DDOx} = 1.7 V, I_{OL} = 4 mA (ERC = FAST)				
		V_{DDOx} = 1.7 V, I_{OL} = 3 mA (ERC = SLOW)			0.6	V
		V_{DDOx} = 1.7 V, I_{OL} = 5 mA (ERC = MED)				
		V_{DDOx} = 1.7 V, I_{OL} = 8 mA (ERC = FAST)				
I_{OH}	LVCMOS High-level output current	V_{DDOx} = 1.8 V, V_O = 0.5 V; T_A = 25°C		–23		mA
		V_{DDOx} = 1.8 V, V_O = 0.9 V; T_A = 25°C		–18		
I_{OL}	LVCMOS Low-level output current	V_{DDOx} = 1.8 V, V_O = 1.4 V; T_A = 25°C		27		mA
		V_{DDOx} = 1.8 V, V_O = 0.9 V; T_A = 25°C		23		
t_{PLH}, t_{PHL}	Propagation delay			6.8		ns
$t_{SLEW-RATE}$	Output rise/fall slew rate	ERC = Slow, 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		0.5		V/ns
		ERC = Medium 20% to 80%, f_{out} = 100 MHz, C_L = 8 pF		0.8		
		ERC = Fast, 20% to 80%, f_{out} = 250 MHz, C_L = 8 pF		2.7		
$t_{jitt-add}$	Additive jitter	f_{OUT} = 100 MHz, 10k-20M integration bandwidth			350	fs
$t_{sk(o)}$	Output skew(1)				130	ps
odc	Output duty cycle(2),(3)	f_{OUT} = 100 MHz; Pdiv = 1, ERC = MED, FAST	45%		55%	
t_{OE}	Output enable to stable clock output	Pin mode. f_{out} = 100 MHz, device in active mode with outputs disabled, OE asserted		2		µs
t_{PD}	PD de-asserted to stable clock output	Host mode, f_{out} = 100 MHz, device in power down mode, PD de-asserted		10		µs
t_{PU}	Time from power applied to stable clock output(4)	Pin mode, f_{out} = 100 MHz, OE asserted, measured from time V_{DD} is valid to stable output.		1		ms

(1) The $t_{sk(o)}$ specification is only valid for equal loading with identical edge rates and output supply voltages.
(2) Assumes 50% duty cycle at the input(s)
(3) odc depends on output rise and fall time (t_R/t_F).
(4) Parameter depends significantly on power supply design and supply voltage rise time.

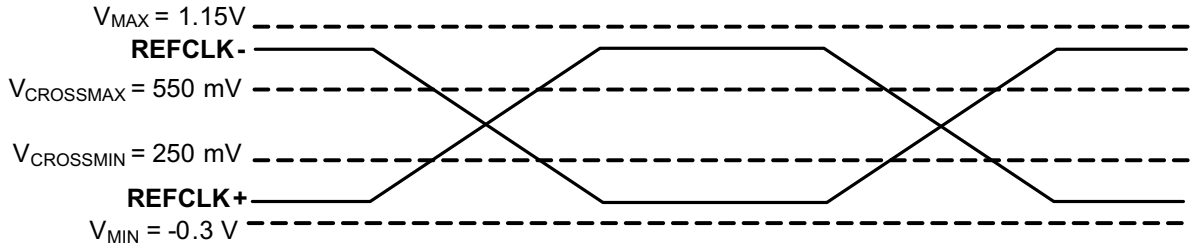


Figure 1. HCSL Crossing Point Voltage

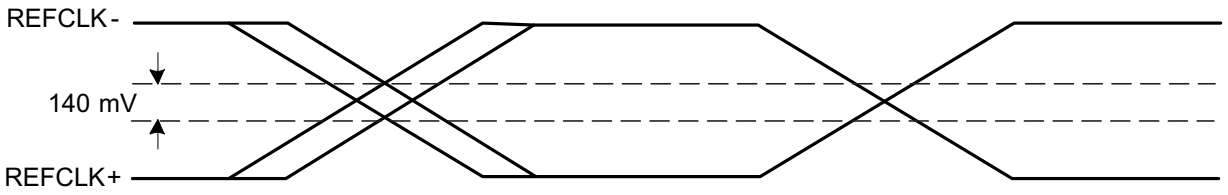


Figure 2. HCSL Variation of VCROSS over all Rising Clock Edges

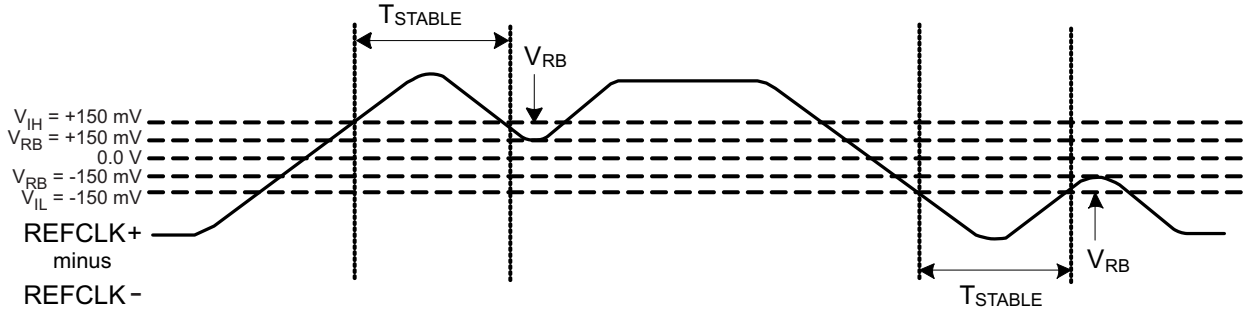


Figure 3. HCSL Ring Back Margin and Timing

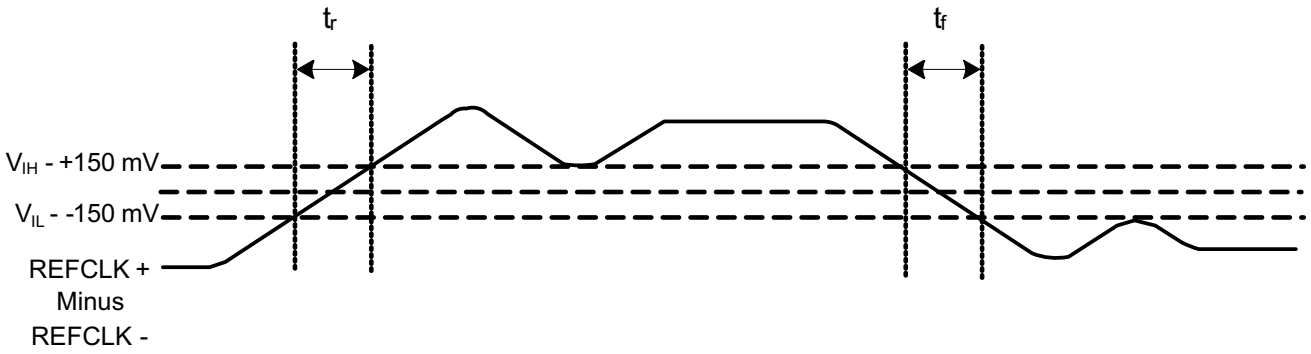


Figure 4. HCSL Rise Fall Time and Edge Speed

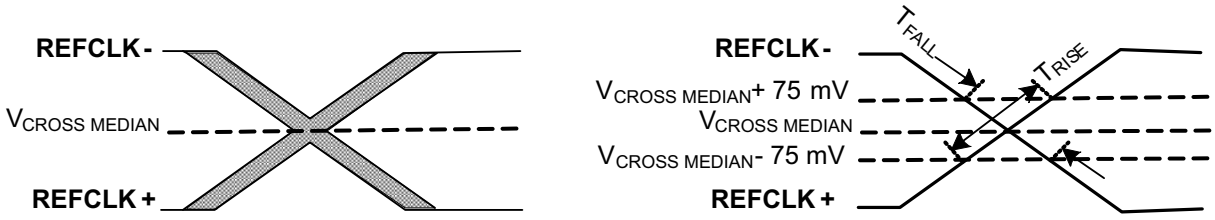


Figure 5. HCSL Rise Fall Time Matching

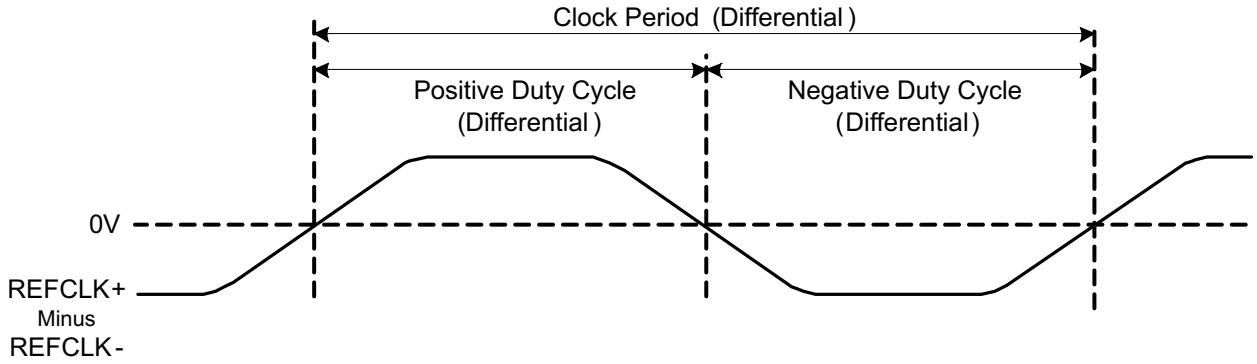


Figure 6. HCSL Duty Cycle

6.12 Typical Characteristics

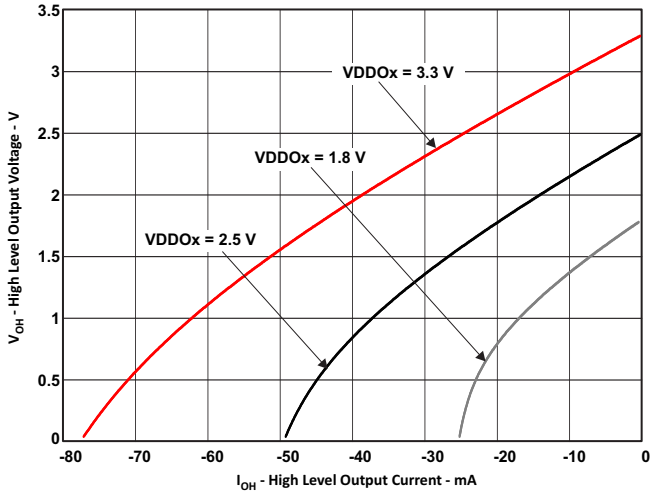


Figure 7. High Level Output Voltage vs. Current - LVCMOS Mode

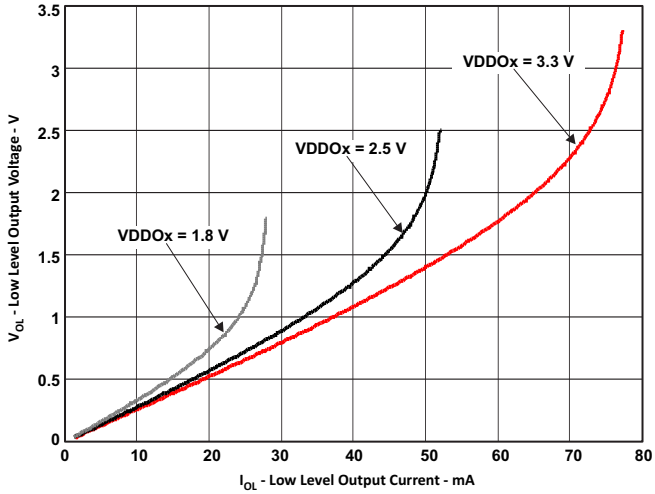


Figure 8. Low Level Output Voltage vs. Current - LVCMOS Mode

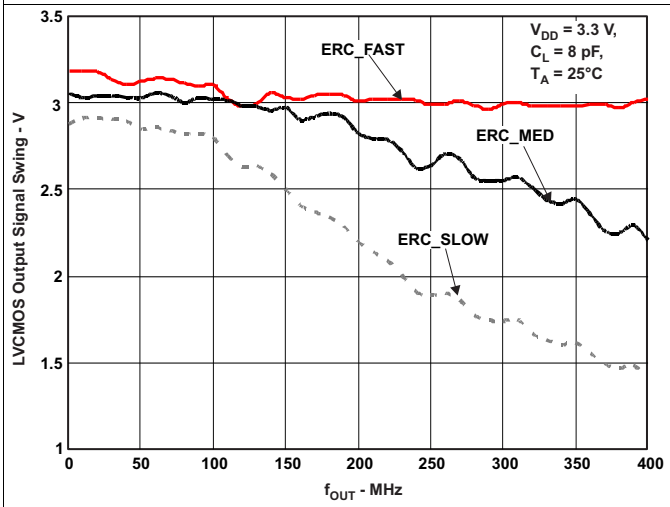


Figure 9. CDCUN1208LP LVCMOS Signal Swing Characteristics (3.3V Mode)

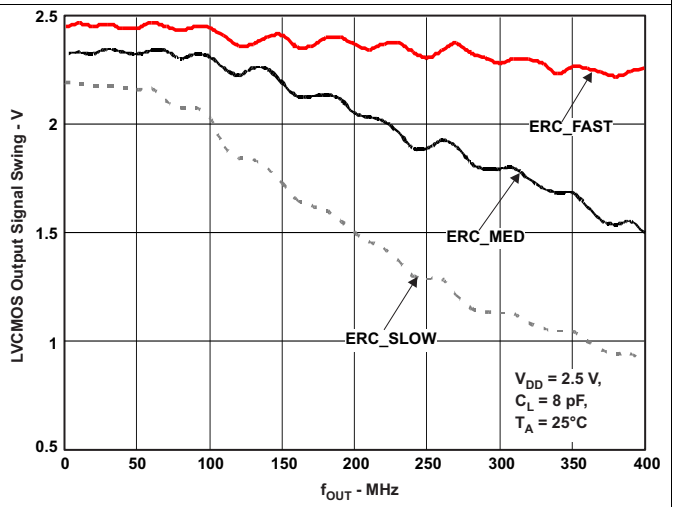


Figure 10. CDCUN1208LP LVCMOS Signal Swing Characteristics (2.5V Mode)

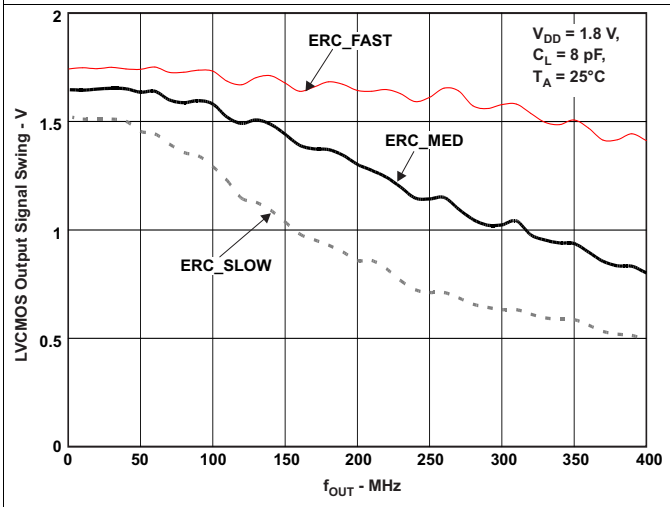


Figure 11. CDCUN1208LP LVCMOS Signal Swing Characteristics (1.8V Mode)

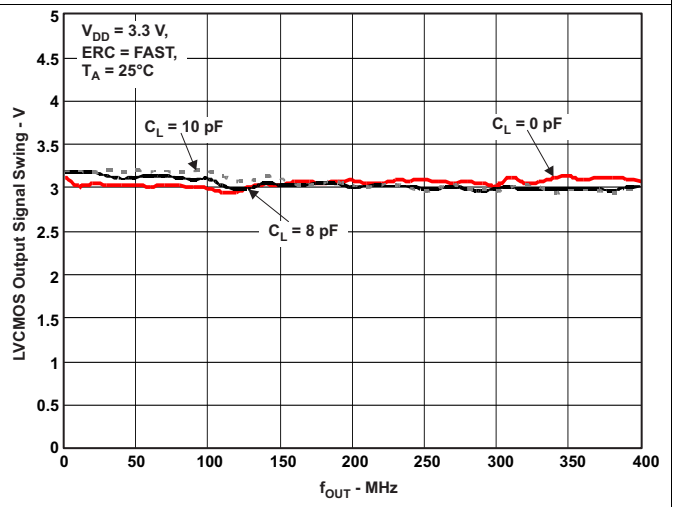


Figure 12. CDCUN1208LP LVCMOS Capacitive Load Drive Characteristics (3.3V Mode)

Typical Characteristics (continued)

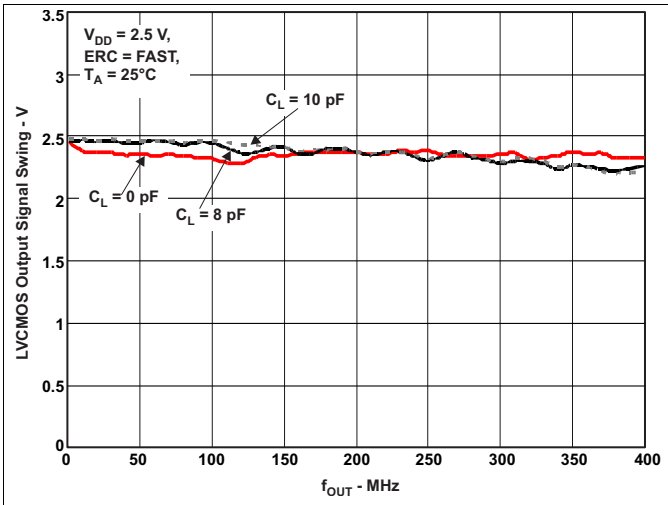


Figure 13. CDCUN1208LP LVCMOS Capacitive Load Drive Characteristics (2.5V Mode)

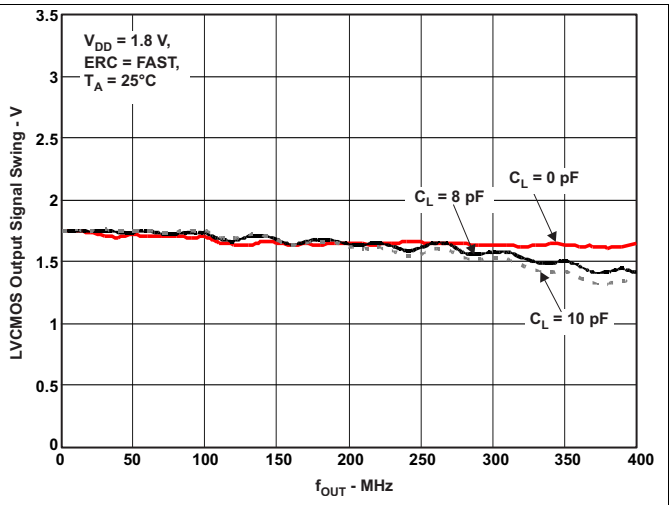


Figure 14. CDCUN1208LP LVCMOS Capacitive Load Drive Characteristics (1.8V Mode)

7 Parameter Measurement Information

7.1 Test Configurations

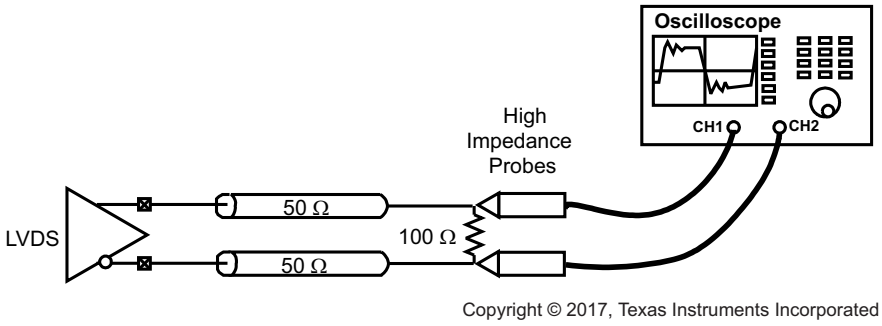


Figure 15. CDCUN1208LP LVDS Output - Test Setup

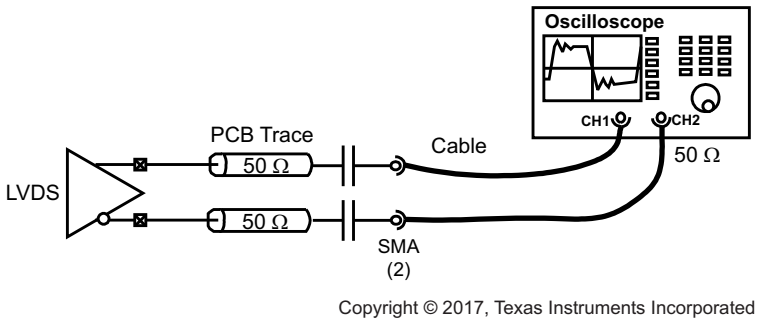


Figure 16. CDCUN1208LP LVDS Output - Propagation Delay/Skew Measurement Setup

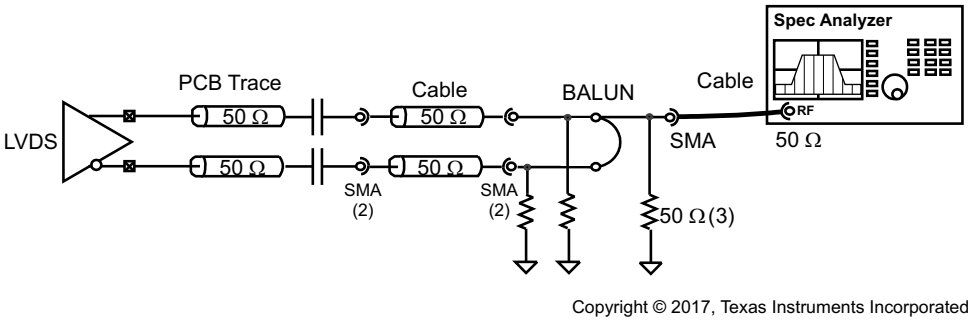


Figure 17. CDCUN1208LP LVDS Output - Phase Noise/Jitter Measurement Setup

Figure 18 shows the configuration used to measure the HCSL buffer characteristics. Either single ended probes with math or differential probes can be used for differential measurements. The 50Ω differential trace length is up to 15 inches.

Test Configurations (continued)

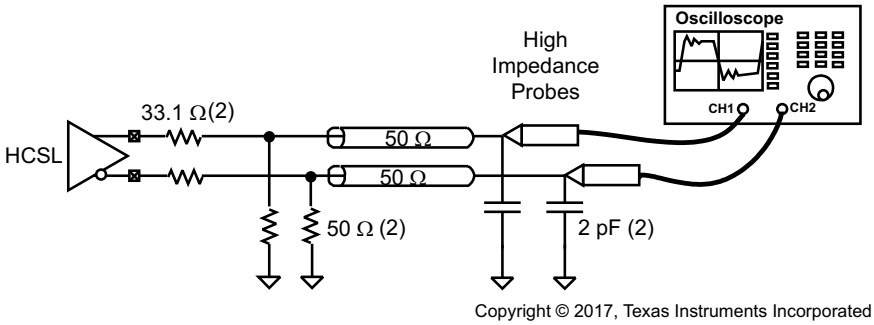


Figure 18. CDCUN1208LP HCSL Output – Measurement Configuration with Load

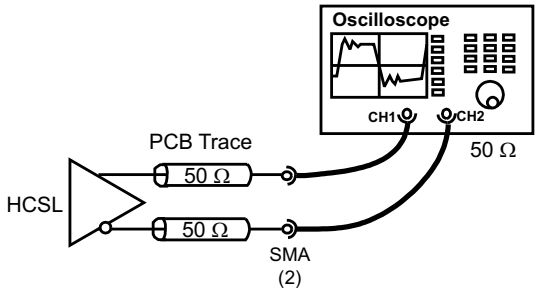


Figure 19. CDCUN1208LP HCSL Output – Propagation Delay/Skew Measurement

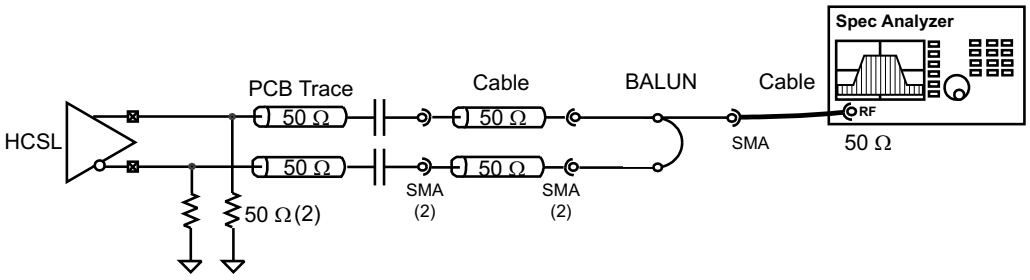


Figure 20. CDCUN1208LP HCSL Output – Phase Noise/Jitter Measurement Configuration

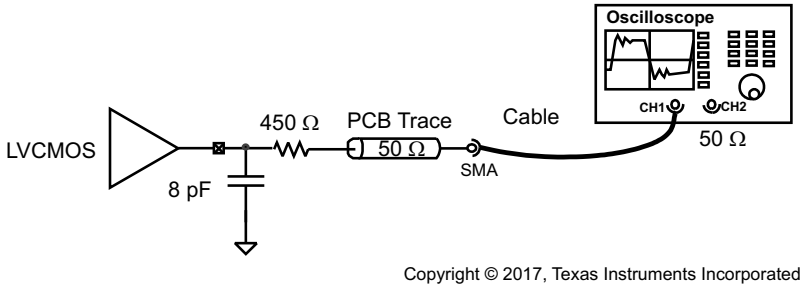


Figure 21. CDCUN1208LP LVCMOS Output – Measurement Configuration

Test Configurations (continued)

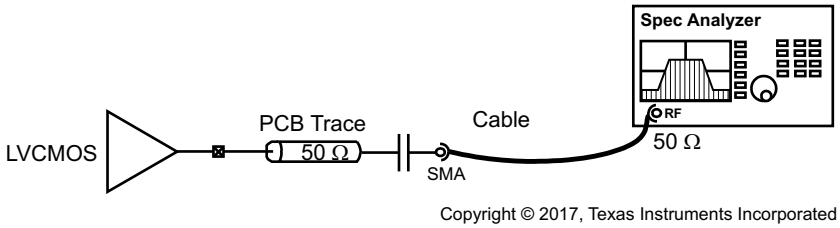


Figure 22. CDCUN1208LP LVCMOS Output – Phase Noise/Jitter Measurement Setup

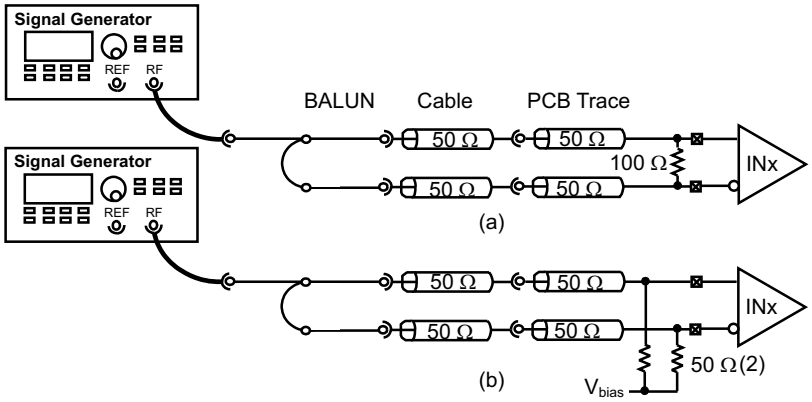


Figure 23. CDCUN1208LP Universal Input - Differential Mode Measurement Setup

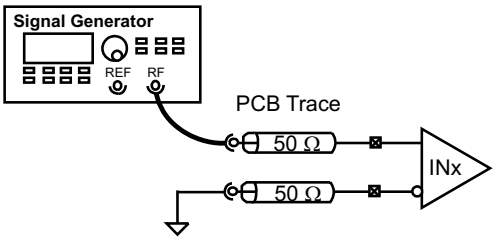


Figure 24. CDCUN1208LP Universal Input - Single-Ended Mode Measurement Setup

Test Configurations (continued)

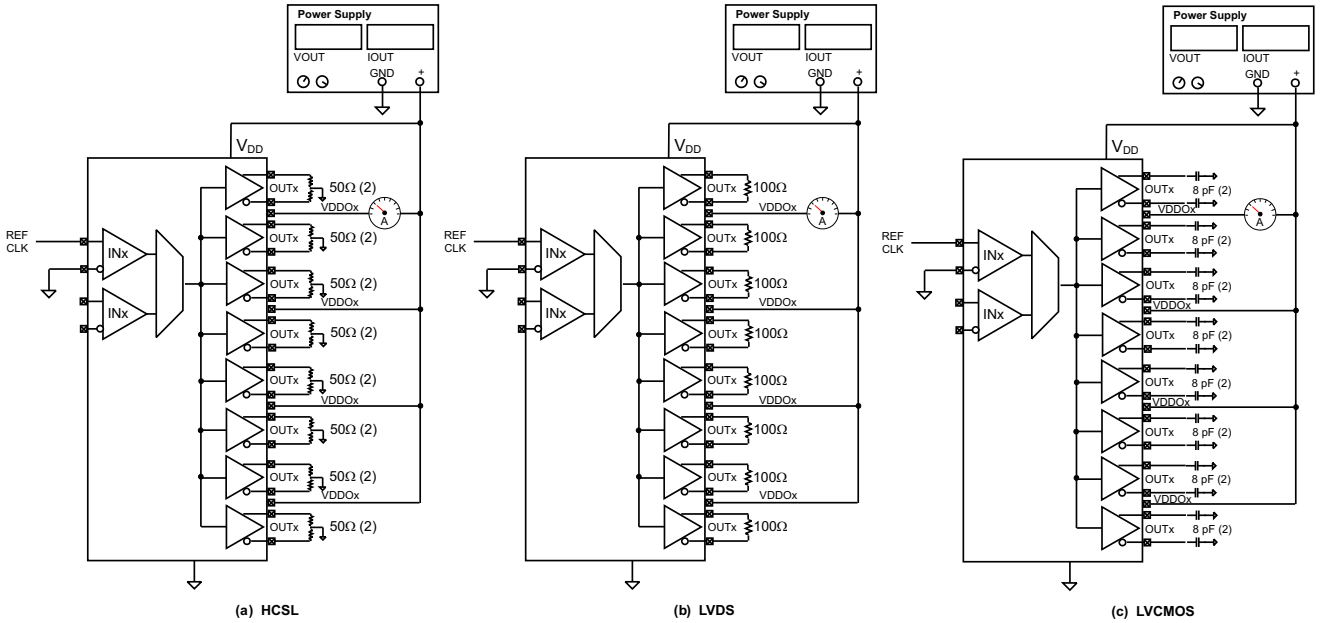


Figure 25. CDCUN1208LP Power Consumption Measurement Setup

8 Detailed Description

8.1 Overview

The CDCUN1208LP is a 2:8 fan-out buffer featuring a wide operating supply range, two universal differential/single-ended inputs, and universal outputs (HCSL, LVDS, or LVCMOS) with edge rate control. The clock buffer supports PCIE gen1, gen2 and gen3. One of the device inputs includes a divider that provides divide values of /1, /2, /4, or /8. The device is flexible and easy to use. The state of certain pins determines device configuration at power up. Alternately, the CDCUN1208LP provides a SPI/I2C port with which a host processor controls device settings. The CDCUN1208LP delivers excellent additive jitter performance, and low power consumption. The device can run in mixed output supply mode with dedicated supply pin for each group of outputs. This allows the device to work as an LVCMOS level translator as well.

8.2 Functional Block Diagrams

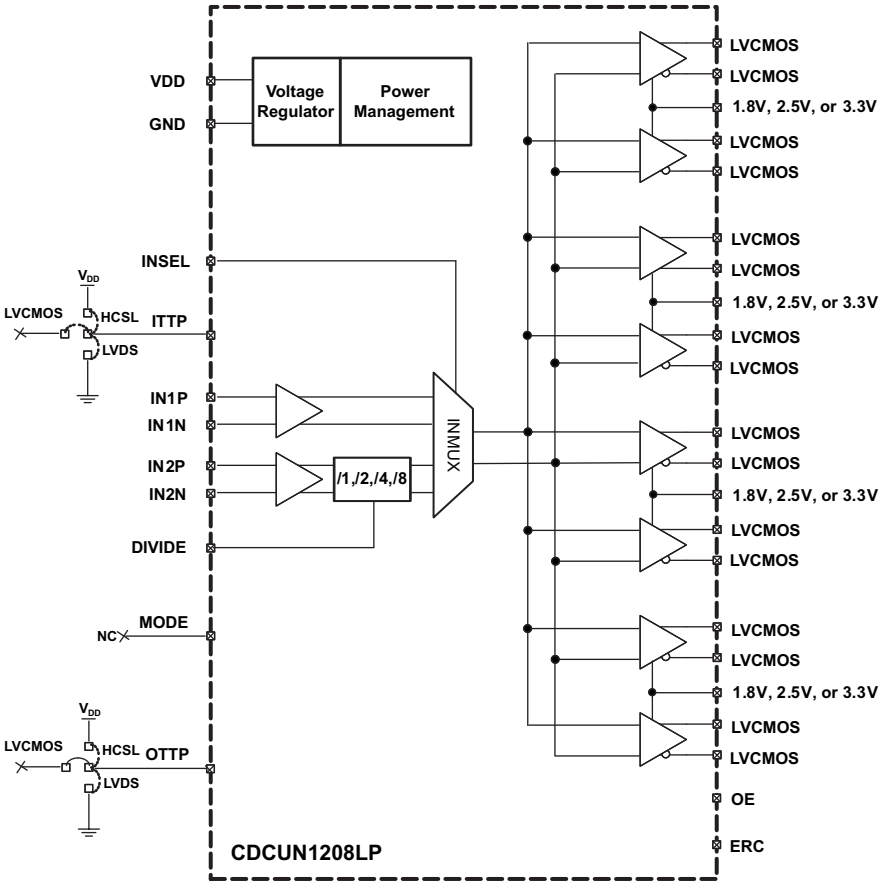


Figure 26. CDCUN1208LP Typical Application Example – LVCMOS Output Mode

Functional Block Diagrams (continued)

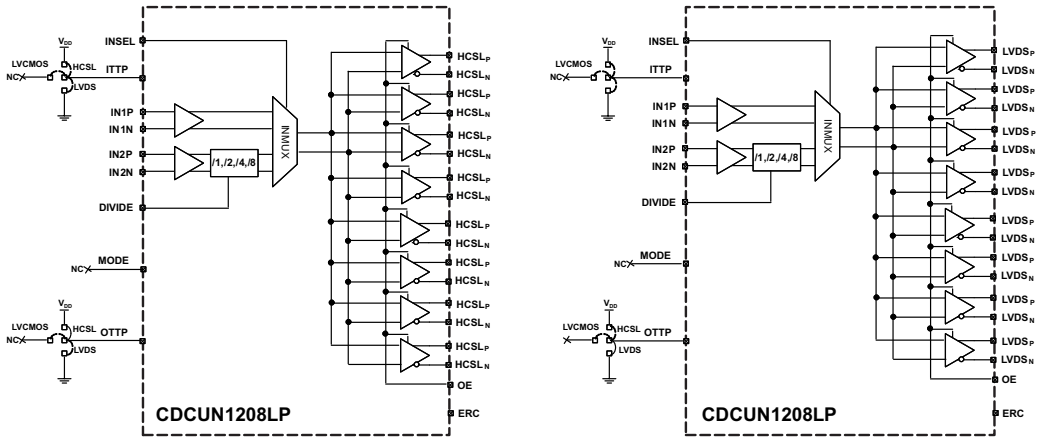


Figure 27. CDCUN1208LP Applications – HCSL and LVDS Fan-Out Buffer Mode

8.3 Feature Description

8.3.1 Device Control Using Configuration Pins

Figure 28 illustrates and Table 1 lists the CDCUN1208LP device settings using the configuration pins. Some pins sense three different states (HIGH, LOW, OPEN) according to Figure 28 and *Digital Input Electrical Characteristics – OE (SCL), INSEL, ITTP, OTTP, Divide (SDA/MOSI), ERC(ADDR/CS), Mode*. The device samples the state of the pins at power up and configures the device accordingly. Certain pins including INSEL and OE are sampled continuously; thus changes of state of INSEL or OE controls the device instantly.

Feature Description (continued)

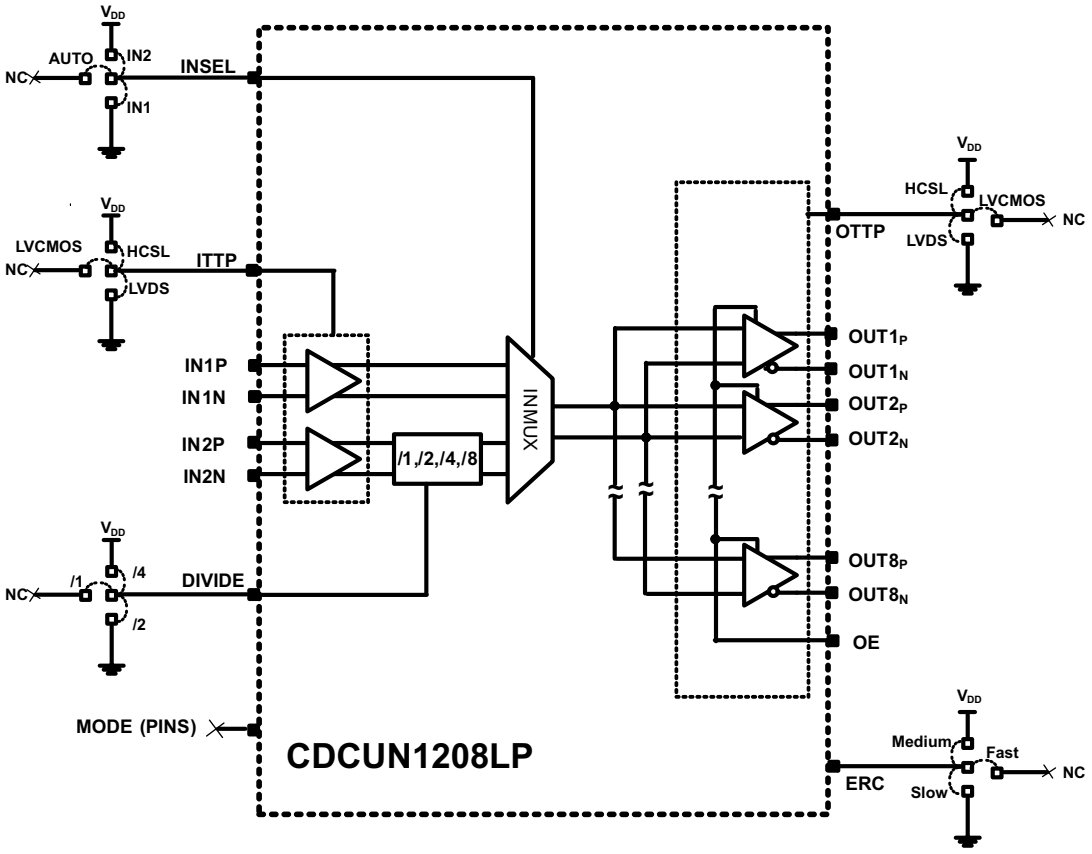


Figure 28. CDCUN1208LP Pin Configuration Overview

Table 1. CDCUN1208LP Pin Configuration Summary

PIN NAME	PIN NUMBER	DEFINITION	DEVICE CONFIGURATION DETAILS
DEVICE OUTPUTS			
OTTP	19	Output Type Setting	See Table 2
ERC	31	Edge Rate Control	See Table 3
OE	32	Device Global Output Enable	See Table 4
DEVICE INPUTS			
ITTP	8	Input Type Setting	See Table 5
DIVIDE	1	IN2 Input Divider Control	See Table 6
INSEL	2	Input Multiplexer Setting	See Table 7

8.3.1.1 Configuration of Output Type (OTTP)

Table 2 shows how to set the output buffer type using the OTTP pin. This setting affects all device outputs equally. Certain combinations of output buffers include a dedicated power supply pin which must be properly bypassed. If the device output configuration is set to LVCMOS, then the supply voltage applied establishes the switching thresholds corresponding to the supply provided according to *Clock Output Buffer Electrical Characteristics (Output Mode = LVCMOS)*. For example, if OUT1 and OUT2 are supplied with a 1.8V power supply via the VDDO1 pin, the switching thresholds are set to the 1.8V logic domain. The system may have other logic supplies (1.8V, 2.5V, or 3.3V) connected to the device on different output buffer supply domains simultaneously. This enables the device to clock devices operating on different supplies without the need for external logic level translation buffers. The CDCUN1208LP automatically adjusts the switching thresholds corresponding to these common logic power supply voltages. For more information regarding the power supplies for the output section, see *Device Power Supply Connections and Sequencing*.

Table 2. CDCUN1208LP Pin Configuration of Output Type

OTTP (Pin 19)	OUTPUT TYPE
LOW	LVDS
HIGH	HCSL
OPEN	LVCMOS

8.3.1.2 Configuration of Edge Rate Control (ERC)

The CDCUN1208LP supports Edge Rate Control (ERC) used to tailor jitter and EMI performance from device outputs. Table 3 shows the edge rate control setting. This setting affects all device outputs equally. Each edge rate setting is unique to the output buffer type selected as described in *Clock Output Buffer Characteristics (Output Mode = LVDS)*, *Clock Output Buffer Characteristics (Output Mode = HCSL)*, and *Clock Output Buffer Electrical Characteristics (Output Mode = LVCMOS)*.

Table 3. CDCUN1208LP Pin Configuration of Output Edge Rate

ERC (Pin 31)	OUTPUT EDGE RATE
LOW	SLOW
HIGH	MEDIUM
OPEN	FAST

8.3.1.3 Control of Output Enable (OE)

Table 4 shows how the output enable pin controls the device outputs. The OE pin is sampled continuously so that the application may turn on/off the output buffers at any time.

Table 4. CDCUN1208LP Pin Control of Output Enable

OE (Pin 32)	OUTPUT ENABLE
LOW	DISABLED in Tri-State
HIGH	ENABLED
OPEN	RESERVED (1)

(1) Leaving the Output Enable pin OPEN will cause the CDCUN1208LP to malfunction. This pin must be driven high or low at all times

8.3.2 Input Ports (IN1, IN2)

8.3.2.1 Configuration of the Input Type (ITTP)

Table 5 describes how to set the input buffers to the appropriate switching levels using the ITTP pin. For proper input termination, see Figure 46.

Table 5. CDCUN1208LP Pin Control of Input Type (ITTP)

ITTP (Pin 8)	ITTP SETTING
LOW	LVDS
HIGH	HCSL
OPEN	LVCMOS

8.3.2.2 Configuration of the IN2 Divider (INDIV)

Table 6 describes how to set the input divider using the DIVIDE pin. If the /8 setting is desired, then this feature is accessed via the host configuration method only refer to section *Device Control Using The Host Interface*.

Table 6. CDCUN1208LP Pin Control of INDIV Divider

DIVIDE (Pin 1)	INDIV DIVIDER SETTING
LOW	/2
HIGH	/4
OPEN	/1

8.3.3 Smart Input Multiplexer (INMUX)

The Smart Multiplexer supports manual and automatic switching between IN1 and IN2. If enabled, the Smart Multiplexer switches automatically between clock inputs based on a prioritization scheme shown in Table 7. If using the Smart Multiplexer Auto Mode, the frequencies of the clocks applied to the smart multiplexer via IN1 and IN2 (via the divider) may differ by up to 20%. The phase relationship between clock inputs has no restriction. The smart multiplexer includes signal conditioning that provides glitch suppression.(1)

Upon the detection of a loss of signal on the input with higher priority, the smart multiplexer switches over to the other clock input on the first incoming rising edge. During this switching operation, the output of the smart multiplexer is low. Upon restoration of the higher priority clock, the smart multiplexer waits until it detects four complete cycles from the higher priority clock prior to switching the output of the smart multiplexer back to the higher priority clock. During this switching operation, the output of the smart multiplexer remains high until the next falling edge as shown in Figure 29.

8.3.3.1 Pin Configuration of the Smart Input Multiplexer (INMUX)

Table 7 shows how to control the Smart Input Multiplexer. In Pin Configuration mode, the INSEL pin is sampled continuously so that the application may select the input clock at any time.

Table 7. Control of INMUX via the INSEL Pin

INSEL(Pin 2)	IN1 BUFFER SETTING	IN2 BUFFER SETTING
LOW	ON and selected by INSEL Multiplexer	OFF
HIGH	OFF	ON and selected by INSEL Mux
OPEN	Smart Multiplexer selects input. IN1 is the primary input (it has the highest priority, therefore if it is available, the smart multiplexer selects IN1)	

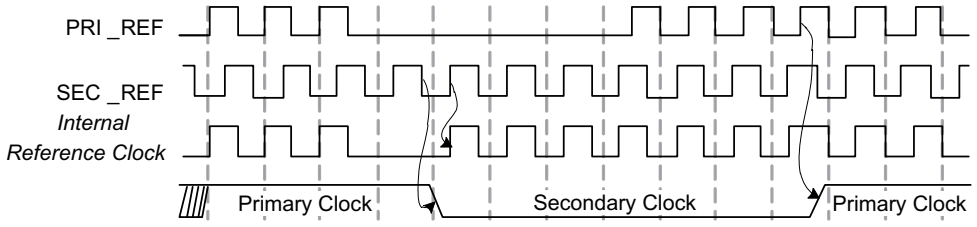


Figure 29. CDCUN1208LP Smart Multiplexer Operation

(1) This implementation does not implement a phase build-out mechanism; rather, analog filtering insuring a smooth transition at device outputs.

8.4 Device Functional Modes

8.4.1 Device Control Using The Host Interface

Host configuration mode affords a greater degree of flexibility. Unlike pin configuration mode in which the pin settings affect the entire device, host configuration mode enables the user to apply different settings to each input and output port as depicted in Figure 30. This includes the ability to mix and match output type, edge rate control, and output enable settings. The host interface is enabled/selected by strapping the MODE pin either high (for I^2C) or low (for SPI) and resetting the device. Additional device features are accessible only through the host interface as well. For instance, the user can configure the input divider (IDIV) to /8 in host configuration mode only. Additionally, the system can power down the device through device registers.

8.4.1.1 OE and INSEL in Host Configuration Mode

In host configuration mode, the OE pin is no longer available; therefore buffers are controlled individually via the host interface. The input multiplexer can be controlled either via the pin or via the device registers in accordance with Table 12.

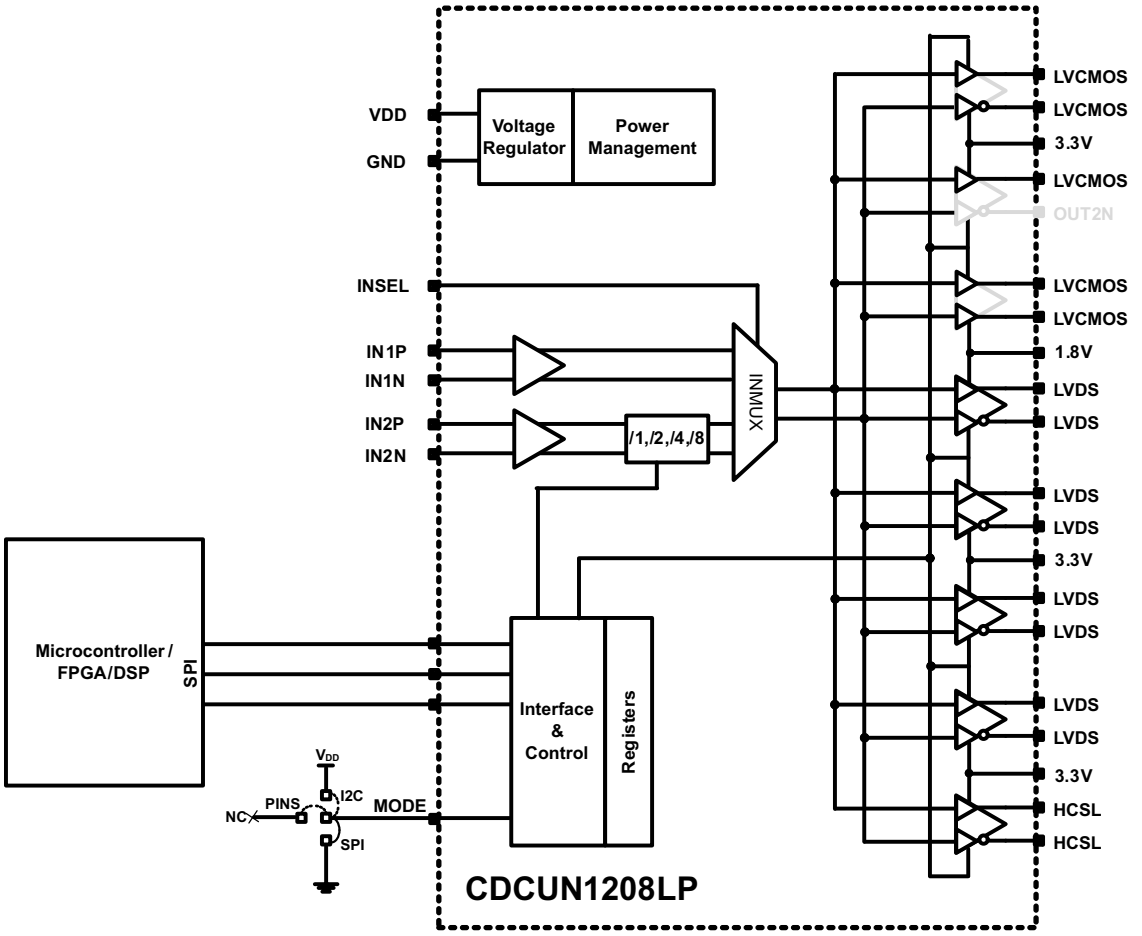


Figure 30. CDCUN1208LP Host Configuration – Typical Application

Device Functional Modes (continued)

When the host interface is enabled, certain pins take on alternative functions according to Table 8.

Table 8. CDCUN1208LP Host Configuration Pins

PIN NAME IN HOST MODE	ALT PIN NAME IN PIN MODE (MODE = OPEN)	PIN NUMBER	PIN NAME IN HOST PROGRAMMING MODE (MODE/Pin 30 is tied high or low)	PIN NAME IN PIN CONFIGURATION MODE (only if MODE/Pin 30 is OPEN)
MODE		30	Programming Mode 1 = I^2C, 0 = SPI,OPEN = Pins (alternative description applies)	
SDA/MOSI	DIVIDE	1	Host Interface Data (I^2C), SPI MasterOutput Slave Input (Data In)	Input Divider Pin Control
MISO	OTTP	19	SPI Master Input Slave Output (DataOut)	Output Type (OTTP) Pin Control
SCL	OE	32	Host Interface Clock	Device Output Enable 1 = Enable, 0 = Disable
ADDR/CS	ERC	31	Host Interface Address (I^2C)/Chip Select (SPI)	Output Edge Rate Control 1 = Fast, 0 = Slow, OPEN = Medium

The CDCUN1208LP samples the MODE pin after the device exits the power on reset (POR) state. The device is placed in the RESET state in one of two ways: a power on reset (POR) circuit automatically resets the device after power is applied; or through the RESET bit (R15[1]) in register memory (see Table 12). This RESET bit is only accessable in host configuration mode. If the MODE pin (pin 11) is open (no connection), then the device is placed in the pin configuration mode and all settings are determined by the state of various pins according to Table 1 and Figure 28. If the MODE pin is low, then device enables the SPI interface; and, if MODE is high, then I^2C is enabled.

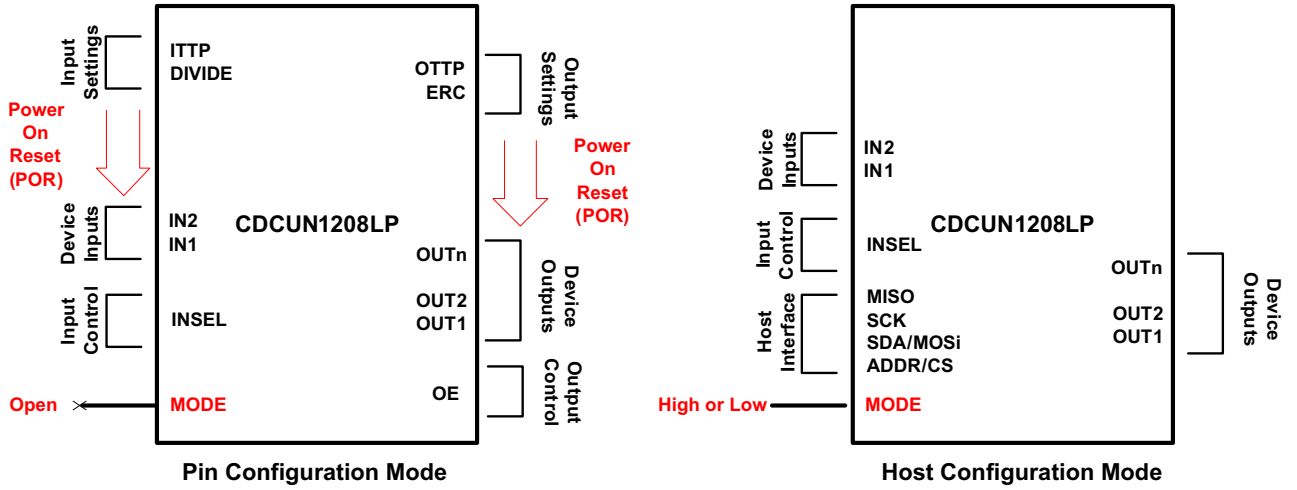


Figure 31. CDCUN1208LP Pin and Host Configuration Mode

8.5 Programming

8.5.1 Host Interface Hardware Information

8.5.1.1 SPI Communication

A SPI communication link includes a master and one or more slaves (note that CDCUN1208LP supports only single-device). Table 8 lists the four signal lines that form a SPI communication link. Figure 32 shows the format for SPI messages. The SPI master (host) initiates communication by asserting SCS low. Information on SDI/SDO is latched on each rising edge of SCL. The first bit transmitted on SDI establishes the direction of the SPI transfer. Next, the master transmits the address to be written/read (up to 15 bits). If the operation is a write, the master transmits 16 data bits on SDI. If the transfer is a read, the slave transmits 16 data bits on SDO (the master continues to clock the transfer via SCL). Figure 34 and Table 9 show the timing specifications for SPI.

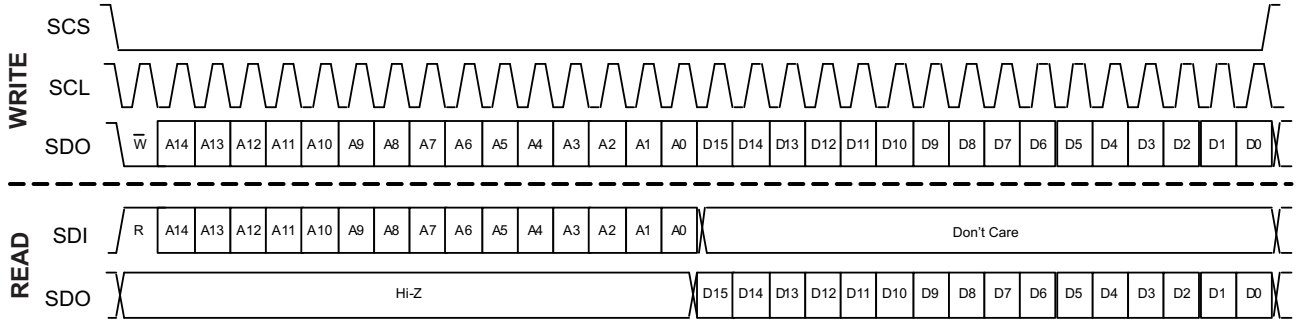


Figure 32. SPI Message Format

8.5.1.1.1 CDCUN1208LP SPI Addressing

Figure 33 shows how to construct the address field for SPI messages to/from the CDCUN1208LP. The device is assigned a 4-bit fixed address (0001b). In order for the host to communicate with the CDCUN1208LP, the address must include this fixed value in the correct position for the device to recognize the message.

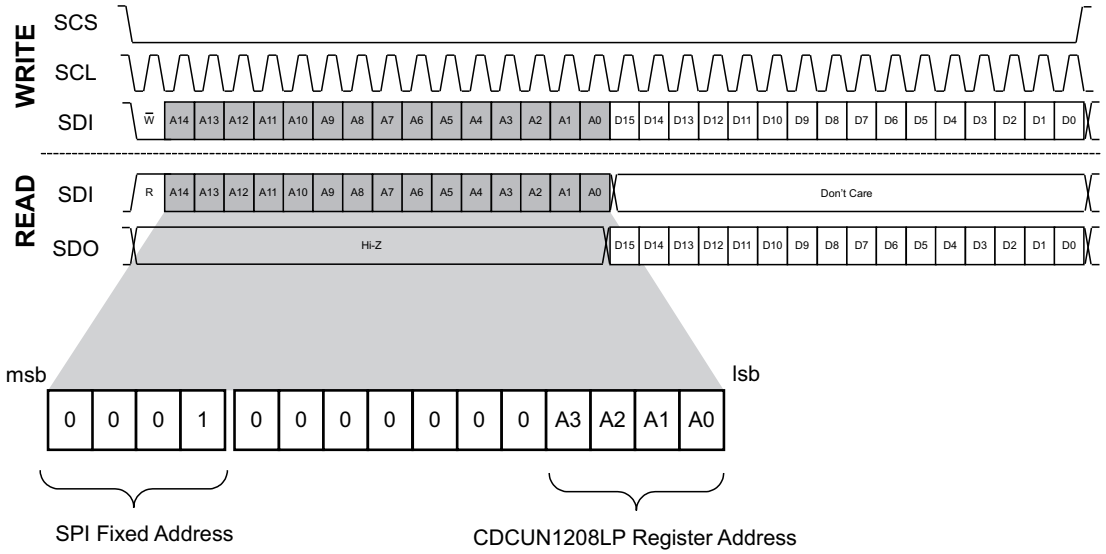


Figure 33. CDCUN1208LP Device Addressing - SPI Mode

Programming (continued)

8.5.1.1.2 Writing to the CDCUN1208LP

To initiate a SPI data transfer, the master (host) asserts the SCS (serial chip select) pin low (see Figure 32). The first rising edge of the clock signal (SCL) transfers the bit presented on the SDI pin of the CDCUN1208LP. This bit signals if a read (first bit high) or a write (first bit low) will transpire. The master shifts data to the slave with each rising edge of SCL. Following the W/R bit are 4 fixed bits followed by 11 bits that specify the address of the target register in the register file (see Figure 33). The 16 bits that follow are the data payload. If the master sends an incomplete message, (i.e. the master de-asserts the SCS pin high prior to a complete message transmission), then the slave aborts the transfer, and device makes no changes to the register file or the hardware. The master signals the slave of the completed transfer and disables the SPI port by de-asserting the SCS pin high. At no time should the clock be toggled while SCS is high. CDCUN1208LP should always be used in single-slave SPI configuration.

8.5.1.1.3 Reading from the CDCUN1208LP

As with the write operation, the master first initiates a SPI transfer by asserting the SCS pin low. The host signals a read operation by shifting a logical high in the first bit position, signaling the slave that the master is initiating a read data transfer from the slave. Thereafter, the master specifies the address of interest according to Figure 33. During the 16 clock cycles that follow, the slave presents the data from the register specified in the first half of the message on the SDO pin. The master signals the slave that the transfer is complete by de-asserting the SCS pin high. At no time should the clock be toggled while SCS is high. CDCUN1208LP should always be used in single-slave SPI configuration.

8.5.1.1.4 Block Write/Read Operation

The CDCUN1208LP supports a block write and block read operation. The master need only specify the lowest address of the sequence of addresses that the host needs to access. The CDCUN1208LP will automatically increment the internal register address pointer if the SCS pin remains active low after the SPI port finishes the initial 32-bit transmission sequence. Each transmission of 16 bits (a data payload width) results in the slave automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

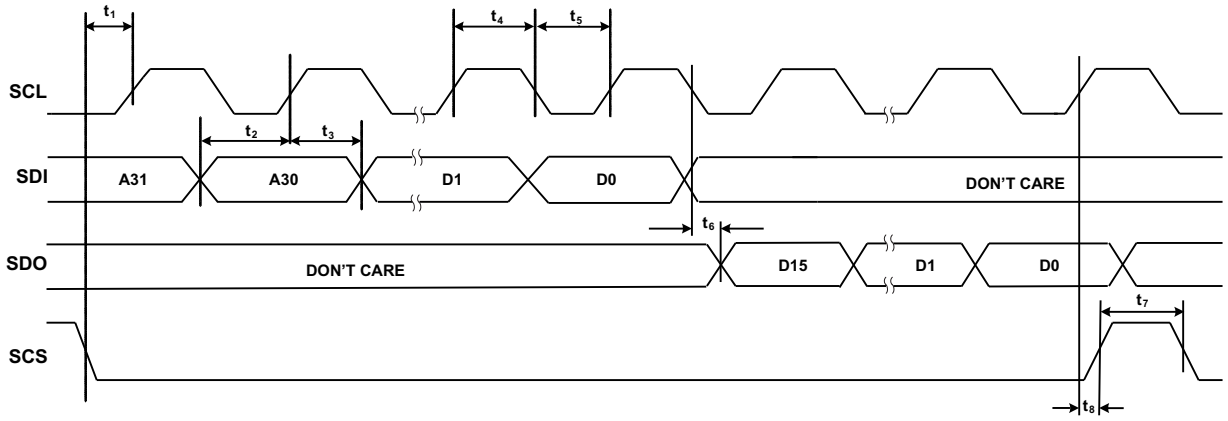


Figure 34. SPI Timing Diagram

Programming (continued)

Table 9. SPI Timing Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
f_{Clock}	Clock frequency for the SCL			20	MHz
t_1	SCS to SCL setup time	10			ns
t_2	SDI to SCL setup time	10			ns
t_3	SDO to SCL hold time	10			ns
t_4	SCL high duration	25			ns
t_5	SCL low duration	25			ns
t_6	SCL to SDO Setup time	10			ns
t_7	SCS pulse width	20			ns
t_8	SCL to SCS release time	10			ns

8.5.1.2 I^2C Communication

The CDCUN1208LP incorporates an I^2C port compliant with I^2C Bus Specification V2.1 (7-bit addressing). Some highlights are contained herein to provide clarity with respect to how communication between the host and the CDCUN1208LP is facilitated. The I^2C bus comprises two signals (clock – SCL, and data – SDA). I^2C implements a master-slave protocol and supports multi-master implementations. Unlike SPI that implements a chip select signal for device level addressing and separate data signals for transmit and receive, I^2C embeds the device address in the serial data stream. Because of this, devices that reside on the I^2C must have a unique bus address. I^2C also uses the protocol to control the direction of data flow through the data signaling line.

8.5.1.2.1 Message Transmission

8.5.1.2.1.1 Data and Address Bits

When transmitting address or data bits, the transmitter must only change the state of SDA when SCL is low. During the time that SCL is high, SDA must be stable (no transitions).

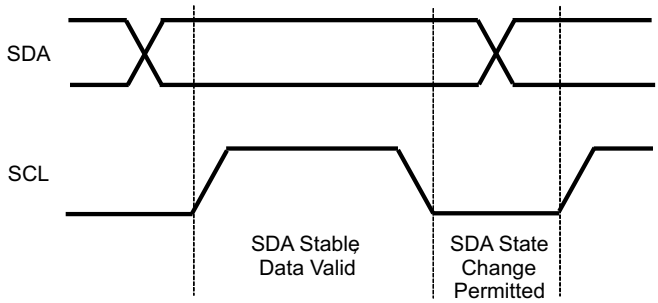


Figure 35. I²C Data/Address Bit Transmission

8.5.1.2.1.2 Special Symbols – Start (S) and Stop (P)

Messages are framed by the master by generating a START and a STOP symbol. The START symbol is signaled by transitioning the SDA line from high to low while the SCL line is high. The STOP symbol is signaled by transitioning the SDA line from low to high while the SCL line is high.

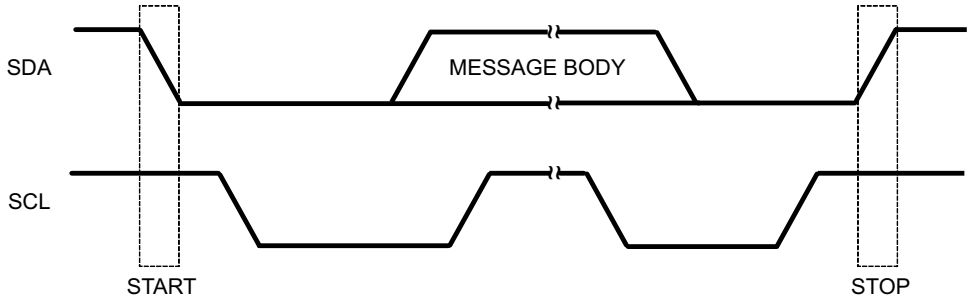


Figure 36. I²C Bus START and STOP Symbol Generation

8.5.1.2.1.3 Special Symbols – Acknowledge (ACK)

The acknowledge symbol must be sent by the receiver during the 9th clock cycle after the transmitter sends a byte of data. The transmitter allows the SDA pin to go high and the receiver pulls the line low to acknowledge the receipt of the byte (leaving the SDA high indicates that the byte was not received). If this occurs the transmitter issues a STOP and retransmits the message. If the receiver is not prepared to receive another byte, it can suspend transmission by holding the SDA line low during the ACK time slot. When the receiver is ready to receive another byte, it releases the SDA line.

8.5.1.2.1.4 Generic Message Frame

Figure 37 shows a typical format for I²C messages. The message frame is bracketed by the START and STOP symbols (both generated by the master). If a START symbol has not been transmitted, then the bus is considered 'available'. If a START symbol has been transmitted and a STOP symbol has not been transmitted, the bus is considered 'busy'. The first 8 bits transmitted include the R/W bit and a 7-bit I²C address field. The reception of each byte grouping that is transmitted must be acknowledged by the receiver. Next, the high byte of the data pay load is transmitted (MSB first) followed by an acknowledgement by the receiver. Finally the low byte is sent. After acknowledgement, the master sends a STOP symbol to end the message frame.

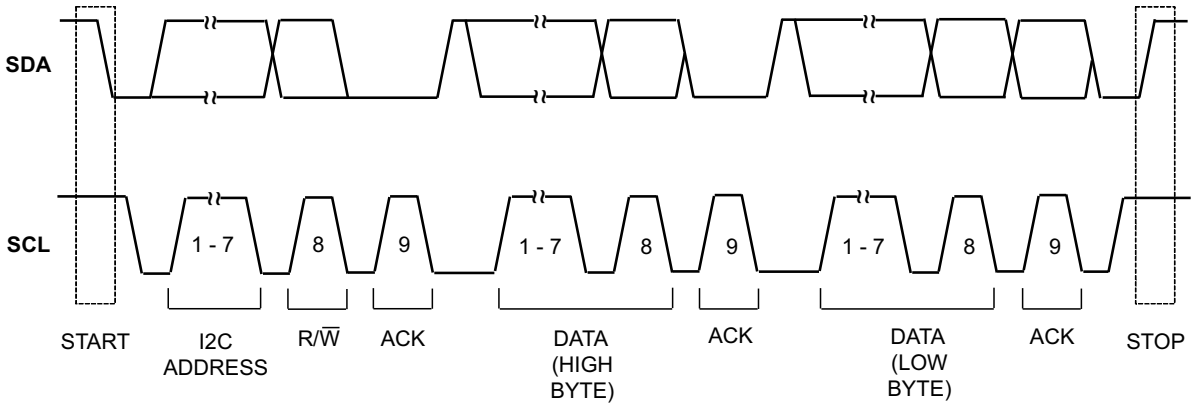


Figure 37. I²C Message Format

8.5.1.2.1.5 CDCUN1208LP Message Format

Figure 38 shows the format of addressing and flow control for I²C messages to/from the CDCUN1208LP. A message includes two address fields. The I²C Address is used to support multiple devices on the bus (each device must have a unique I²C address). The Register Address specifies which register of the device identified by the I²C Address is to be written/read.

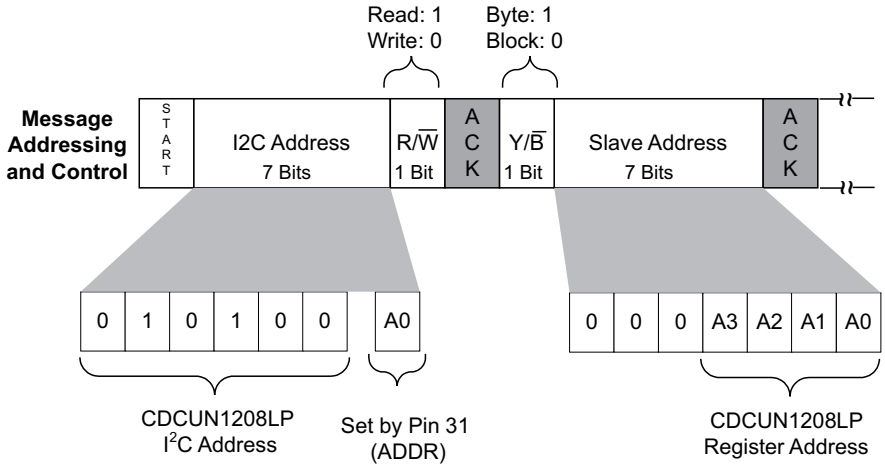


Figure 38. CDCUN1208LP I²C Message - Addressing

8.5.1.2.1.6 CDCUN1208LP Device Addressing (I²C Address)

Figure 38 outlines the construction of the I²C Address shown in Figure 37. The highest 6 bits are assigned to the target device family (are unique to a specific target device family) and are 'hard wired'. The lowest address bit (A0) corresponds to address bit that can be set via pin 31 on the CDCUN1208LP (see Table 8). This allows up to two CDCUN1208LPs to reside on the same I²C bus. The next 8 bits transmitted is called the Register Address.

8.5.1.2.1.7 CDCUN1208LP Device Addressing (Register Address)

Likewise, Figure 38 shows the format of the register address field of the I^2C message. The first bit determines if the transfer is a byte or a block (more than one byte). The CDCUN1208LP register width is 16 bits (2 bytes), therefore, generally block addressing is used to access each register in its entirety. Because the I^2C protocol requires that the slave address is a 7-bit field, the leading 3-bits are all '0' while the trailing 4-bits specify the device register of interest.

8.5.1.2.2 I^2C Master/Slave Handshaking

Figure 39 shows the handshaking between the master (host) and the slave (CDCUN1208LP) that the I^2C protocol supports. In all cases, the master drives the SCL (clock line); however, depending on the direction of transfer/acknowledgement, the master or the slave device drives SDA (data line).

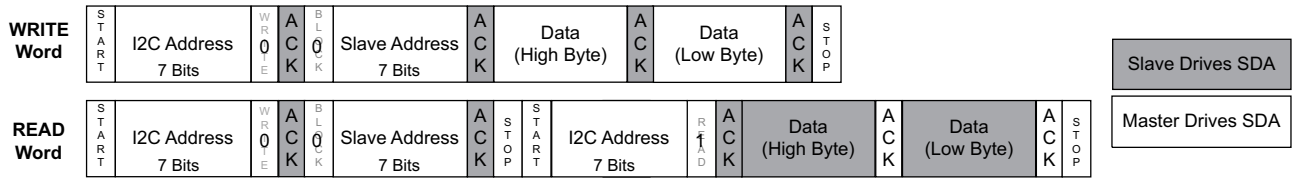


Figure 39. I^2C Master/Slave Handshaking Example

8.5.1.2.3 Block Read/Write

For "Block Write/Read" operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The start address of the transfer is specified in the same way a single word transfer is initiated.

8.5.1.2.4 I²C Timing

Figure 40 and Table 10 provide details regarding the timing requirements for I²C:

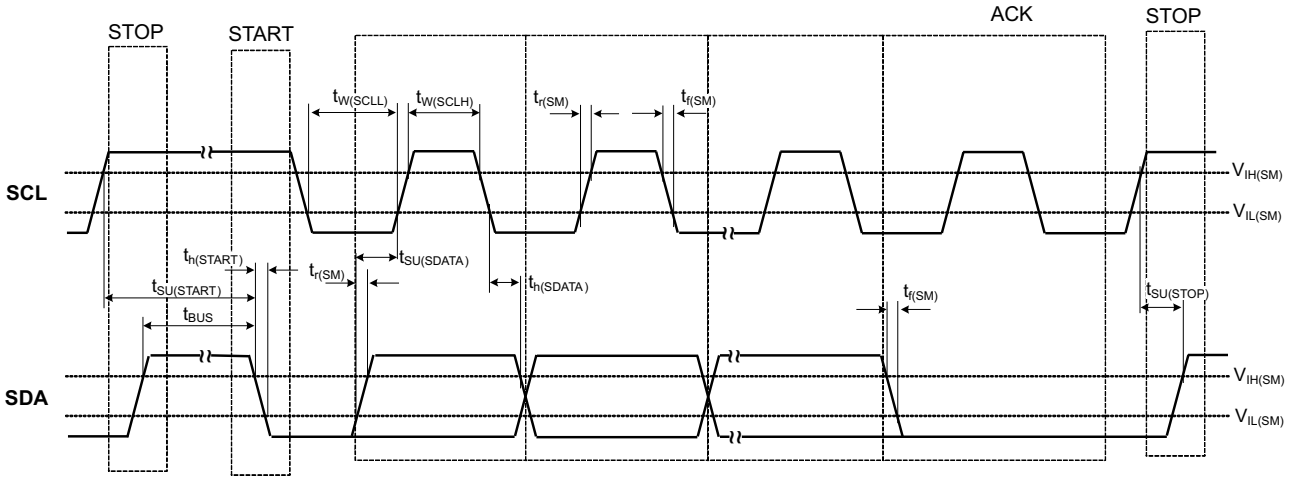


Figure 40. I²C Timing Diagram

Table 10. I²C Timing Requirements

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4.0		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4.0		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	µs
$t_{su(SDA)}$	SDA setup time	250		ns
t_r	SCL / SDA input rise time		1000	ns
t_f	SCL / SDA input fall time		300	ns
$t_{su(STOP)}$	STOP setup time	4.0		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		µs

8.6 Register Maps

8.6.1 Device Registers

8.6.1.1 Device Registers: Register 00-07

Register 00: OUT1
Register 01: OUT2
Register 02: OUT3
Register 03: OUT4
Register 04: OUT5
Register 05: OUT6
Register 06: OUT7
Register 07: OUT8

Table 11. CDCUN1208LP Register 0–7 Bit Definitions

RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION / FUNCTION	POWER UP CONDITION
15	TI RESERVED		**TI RESERVED**	
14				
13				
12				
11				
10	OUTx_CMOS_MODE	Reg 00: OUT1 Reg 01: OUT2 Reg 02: OUT3 Reg 03: OUT4 Reg 04: OUT5 Reg 05: OUT6 Reg 06: OUT7 Reg 07: OUT8	**OUTx CMOS MODE** 1 – both sides pseudo differential 0 – both sides in phase	0
9	OUTx_ERC[2:0]		**OUTx Edge Rate Control** 111 – Medium 100 - Fast 000 - Slow	0
8				0
7				0
6	TI RESERVED		**TI RESERVED**	0
5				0
4	OUTx_OE[1:0]		**OUTx Output Enable** OTTP = LVCMOS 11 – OUT1P: ON | OUT1N: ON 10 – OUT1P: ON |OUT1N: OFF 01 – OUT1P: OFF| OUT1N: ON 00 – OUT1P: OFF| OUT1N: OFF	0
3			OTTP = Differential (LVDS, HCSL) 00 – OFF 11 - ON	0
2	OUTx_OTTP[1:0]		**OUTx Output Type** 11 – HCSL 10 – Reserved 01 – LVCMOS 00 - LVDS	0
1				0
0	OUTx_PD		**OUTx Buffer** 1 – Disabled in Tri-State 0 - Enabled	0

Table 12. CDCUN1208LP Registers 11–15 Bit Definitions

REGISTER ADDRESS	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION / FUNCTION	POWER UP CONDITION
11	15	TI RESERVED			
	14	TI RESERVED			
	13	TI RESERVED			
	12	TI RESERVED			
	11	TI RESERVED			
	10	TI RESERVED			
	9	TI RESERVED			
	8	TI RESERVED			0
	7	TI RESERVED			0
	6	TI RESERVED			0
	5	IN_DIV[1]	Input (IN2 – Divider)	**Input Divider Control** 1 1 = /8 1 0 = /4 0 1 = /2 0 0 = /1	0
	4	IN_DIV[0]			0
	3	IN_TYPE[1]	Input[(1)] (IN1 and IN2 Type)	**Input Type** 1 1 = HCSL 1 0 = LVCMOS 0 1 = LVCMOS 0 0 = LVDS	0
	2	IN_TYPE[0]			0
	1	INSEL[1]	Input (Multiplexer)	**Input Multiplexer Control** 1 1 = Control via INSEL pin 1 0 = Smart MUX Enabled, IN 1=Primary 0 1 = IN2 Buffer Selected 0 0 = IN1 Buffer Selected	0
	0	INSEL[0]			0
12-14	ALL	TI RESERVED			
15	2-15	TI RESERVED			
	1	RESET		**Device Reset** 1 = Reset Device 0 = Run Device	0
	0	PD		**Device Power Down** 1 = Device is powered down 0 = Device is active	0

(1) When configuring device inputs as LVCMOS, apply the signal-ended clock signal to INxP and leave INxN either floating or ground it. The power supply voltage (1.8V, 2.5V, or 3.3V) applied to V_{DD} (pin 5) establishes the switching thresholds for IN1 and IN2 in LVCMOS mode.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 PCI Express Applications

Texas Instruments offers a complete clock solution for PCI Express applications. The CDCUN1208LP can be used to fan out the 100MHz clock signal provided by the CDCM9102 as depicted in Figure 41.

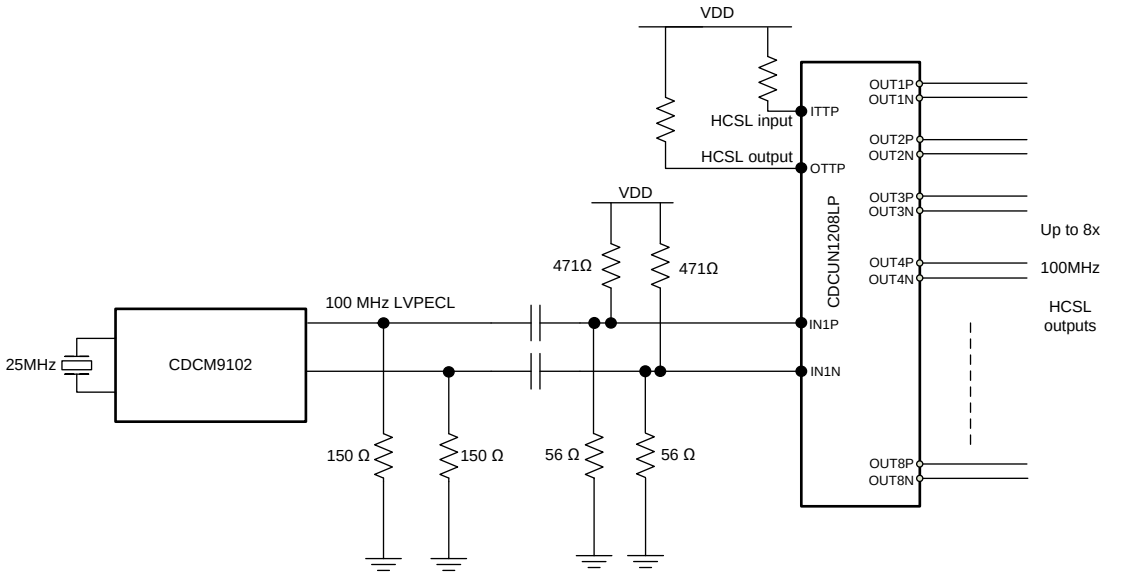


Figure 41. Clock Solution for PCIE Express Applications

9.1.1.1 Design Requirements

For this design example, use the parameters shown in Table 13.

Table 13. Design Parameters

PARAMETER	VALUE
Voltage	TBD
Current	TBD
TBD	TBD

9.1.1.2 Detailed Design Procedure

The CDCUN1208LP is a simple to use device. The user determines the following parameters in order:

In Control mode:

- Pin control mode or SPI mode (Host Interface) : this is done by externally pull up or pull down of the MODE pin.

In Pin control mode:

- The input type, optional input divider ratio and input multiplexer selection should be set.
- The output type, optional output edge rate control, and output enable should be set This is described in detail in *Device Control Using Configuration Pins*.

In Host control mode:

- SPI interface should be connected to the host (Note that only one CDCUN1208LP device can be connected to the bus).
- Communication should follow the procedure described in *Device Control Using The Host Interface*.

9.1.1.3 Application Curves

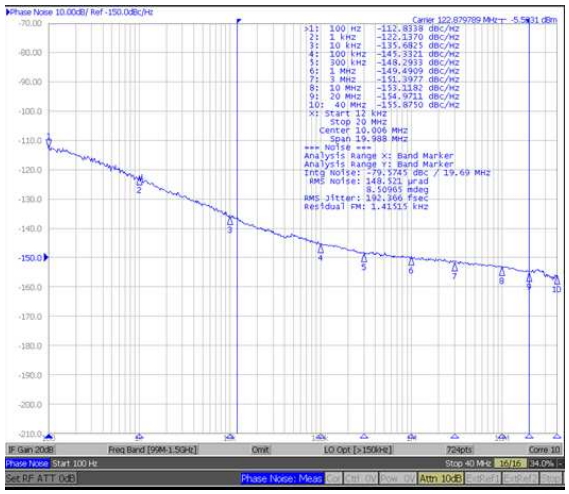


Figure 42. Output 1 (LVCMOS) Phase Noise with Clean 122.88 MHz Source

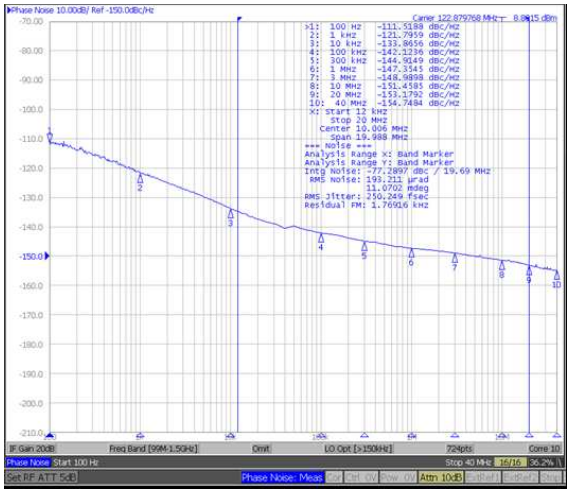


Figure 43. Output 2 (LVCMOS) Phase Noise with Clean 122.88 MHz Source
(PN is slightly worse due to the mux and the divider)

9.2 Systems Examples

Figure 44 shows a typical application in which the receiver is off board. The PCIe Specification (CEM2.0) requires that all source termination is on the motherboard (not on the daughter card). For this reason, the termination resistors are placed as shown. Additionally, source resistors are employed to eliminate ringing. In this case, Z_L can vary between 40Ω and 60Ω and R_S can range from 22Ω to 33Ω.

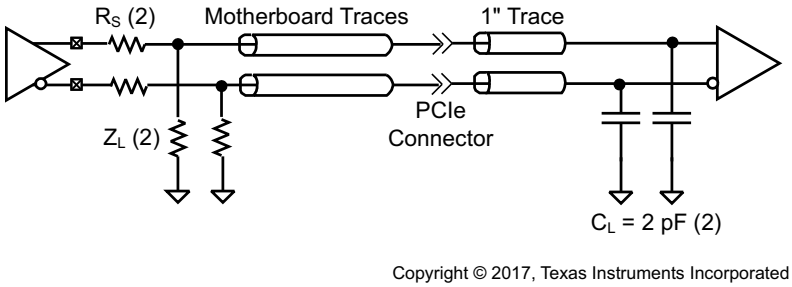


Figure 44. Typical Configuration – Off Board Receiver

Figure 45 shows a typical application in which the receiver is on-board. In this case, series resistors are not required to eliminate ringing as proper termination is achieved. In this case two termination resistors, Z_L = 49.9Ω are placed close to the receiver.

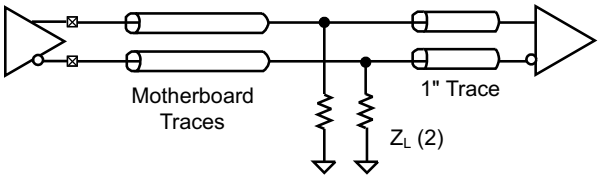


Figure 45. Typical Configuration – On Board Connection

10 Power Supply Recommendations

10.1 CDCUN1208LP Power Consumption

Table 14. CDCUN1208LP Power Consumption (T_A = –40°C to 85°C)

PARAMETER	DEVICE SETTINGS (See Table 1)(1)							TEST CONFIGURATION	DESCRIPTION	MAX CURRENT V_{DD}= 1.8V $f_{OUT} = f_{in}$ = 100 MHz	MAX CURRENT V_{DD} = 3.3V $f_{OUT} = f_{in}$ = 100MHz	UNIT
	MODE	OE	ERC	OTTP	INSEL	ITTP	PD Bit					
$I_{PD1.8,3.3}$	L or H	L	X	X	X	L	H	Host Configuration Mode (see Host Configuration Mode)	Device Power Down	3	4	mA
$I_{CORE1.8,3.3}$	O	L	X	X	X	L	X	Figure 25a,b,c	Device Outputs Off	26	35	mA
$I_{HCSL1.8,3.3}$	O	H	O	H	L	O	X	Figure 25a	HCSL Buffer Current Consumption(2)	23	23	mA
$I_{LVDS1.8,3.3}$	O	H	O	L	L	O	X	Figure 25b	LVDS Buffer Current Consumption(2)	9	9	mA
$I_{LVCMOS1.8,3.3}$	O	H	O	O	L	O	X	Figure 25c	LVCMOS Buffer Current Consumption (one side)(2)	8	11	mA
$I_{DEV-HCSL1.8,3.3}$	O	H	O	H	L	O	X	Figure 25a	Device Current Consumption – HCSL Mode	200	200	mA
$I_{DEV-LVDS1.8,3.3}$	O	H	O	L	L	O	X	Figure 25b	Device Current Consumption – LVDS Mode	80	90	mA
$I_{DEV-LVCMOS1.8,3.3}$	O	H	O	O	L	O	X	Figure 25c	Device Current Consumption – LVCMOS Mode	130	210	mA

(1) H = Input High, L = Input Low; O = Input Open
(2) Buffer current consumption values represent the average of the current drawn by V_{DDO1}, V_{DDO2}, V_{DDO3}, and V_{DDO4} divided by 8 (differential mode) or 16 (single-ended mode).

10.2 Device Power Supply Connections and Sequencing

VDD (pin 5) is the core power supply of the device while VDDOx (pins 11, 14, 22, and 27) provide power for the output sections. The core supply must be present either before the application of the output power supplies or be present simultaneously. Applying an output power supply voltage on any of the VDDOx pins prior to the application of power to the core supply pin will potentially result in improper device operation.

VDDO2 (pin 14) and VDDO4 (pin 27) provide power for OUT1/OUT2 and OUT7/OUT8 respectively. Additionally, these pins provide power to integrated voltage regulators that condition power for two banks of outputs. For example, the regulator associated with OUT1–OUT4 receives power from the VDDO2 pin. Consequently, if the application requires one or two outputs from a bank of four, then the application must use OUT3/OUT4 and apply power via VDDO2 (1). Likewise, the regulator that conditions power for OUT5–OUT8 receives power from VDDO4 (pin 27). If the application uses subset of OUT5–OUT8, then OUT7/OUT8 must be used. For example, if the application will use 6 of the 8 output channels, then VDDO1, VDDO2, and VDDO4 (along with OUT1–OUT4, and OUT7–OUT8) must be used. If the application requires the use of 7 of the 8 output channels, the VDDO1–VDDO4 are used, and OUT1–OUT7 or OUT1–OUT6 and OUT8 could be used.

(1) If OUT1 or OUT2 are used and VDDO1 is powered but not VDDO2, the CDCUN1208LP will not function properly. Likewise, if OUT5 or OUT6 are used and VDDO3 is powered but not VDDO4, then the device will not function properly either.

10.3 Device Inputs (IN1, IN2)

Figure 46 shows how to interface certain common signaling formats to the device inputs of the CDCUN1208LP. This entails both proper signal termination as well as input buffer configuration via the input type (ITTP) pin.

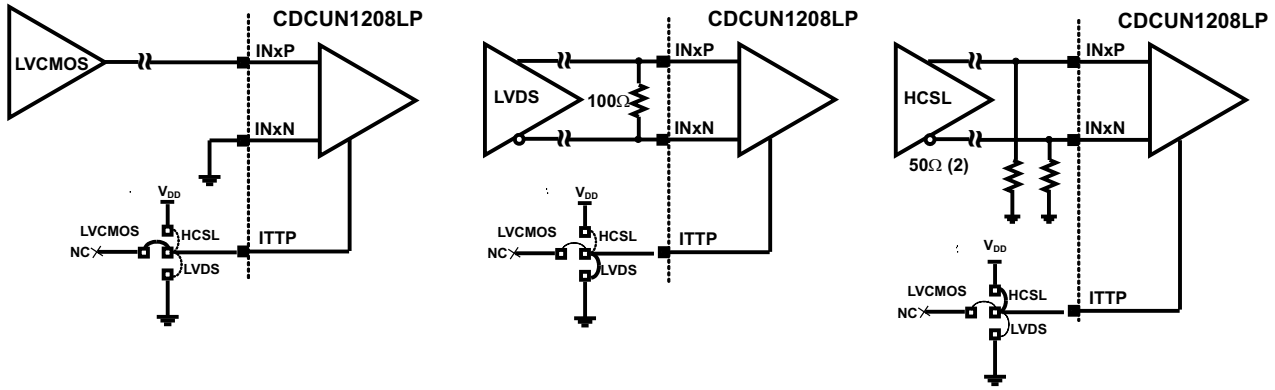


Figure 46. Common Interfaces to Device Inputs – DC Coupling

11 Layout

11.1 Layout Guidelines

- Keep the connections between the bypass capacitors and the power supply on the device as short as possible.
- Ground the other side of the capacitor using a low impedance connection to the ground plane.
- If the capacitors are mounted on the back side, 0402 components can be employed.
- For component side mounting, use 0201 body size capacitors to facilitate signal routing.
- Use a matrix of ground vias to connect the thermal pad to the ground layer.

11.2 Layout Example

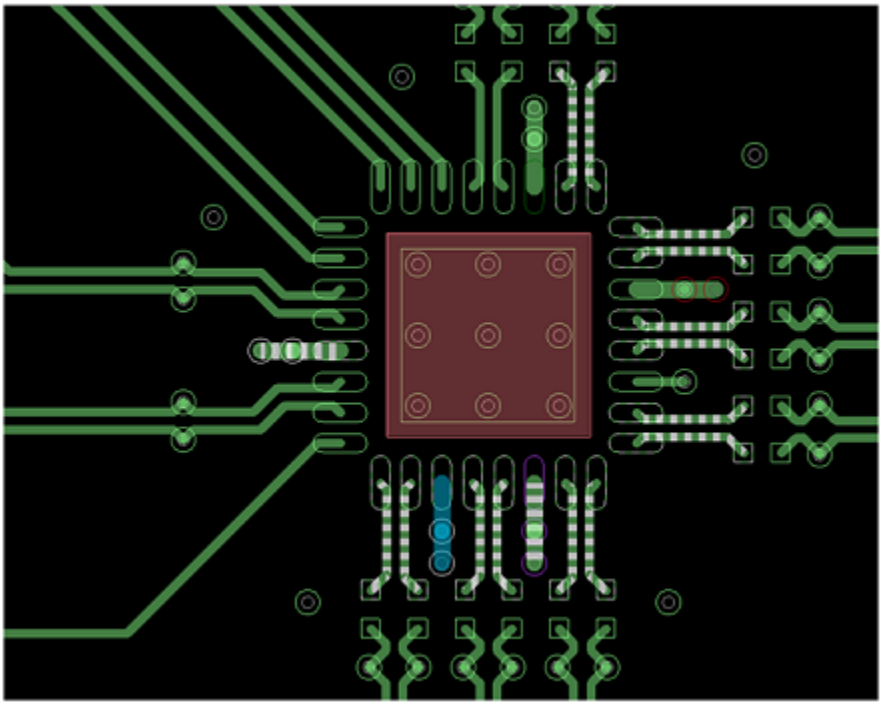


Figure 47. Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCUN1208LPRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UN 1208LP	Samples
CDCUN1208LPRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UN 1208LP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

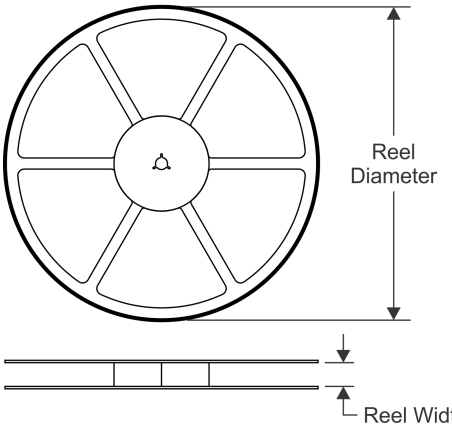
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

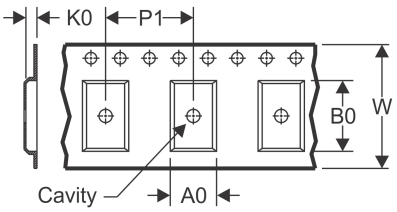
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

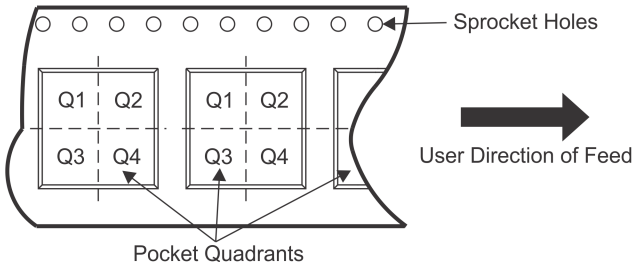


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

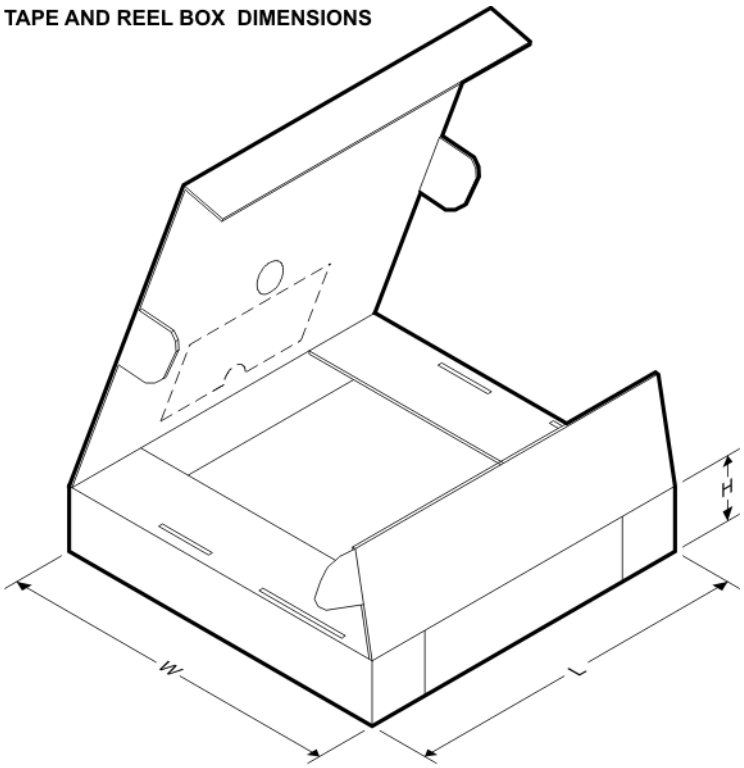
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCUN1208LPRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CDCUN1208LPRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

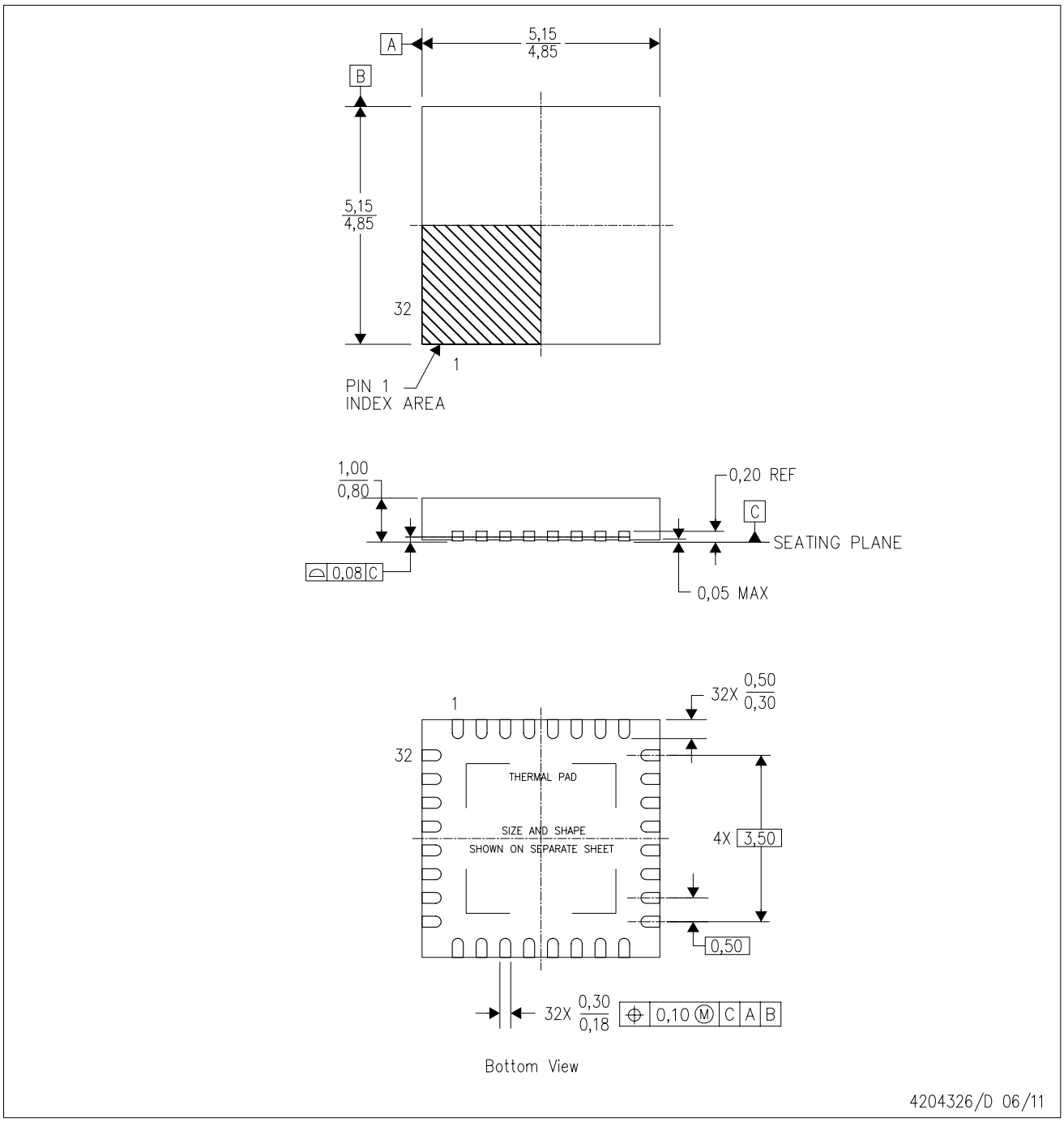
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCUN1208LPRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CDCUN1208LPRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

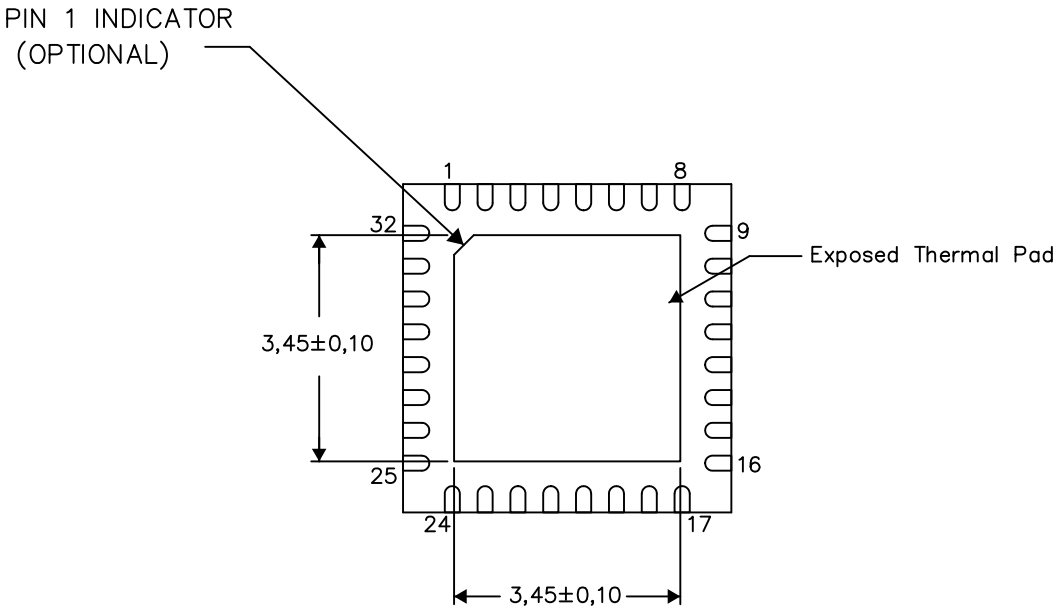
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



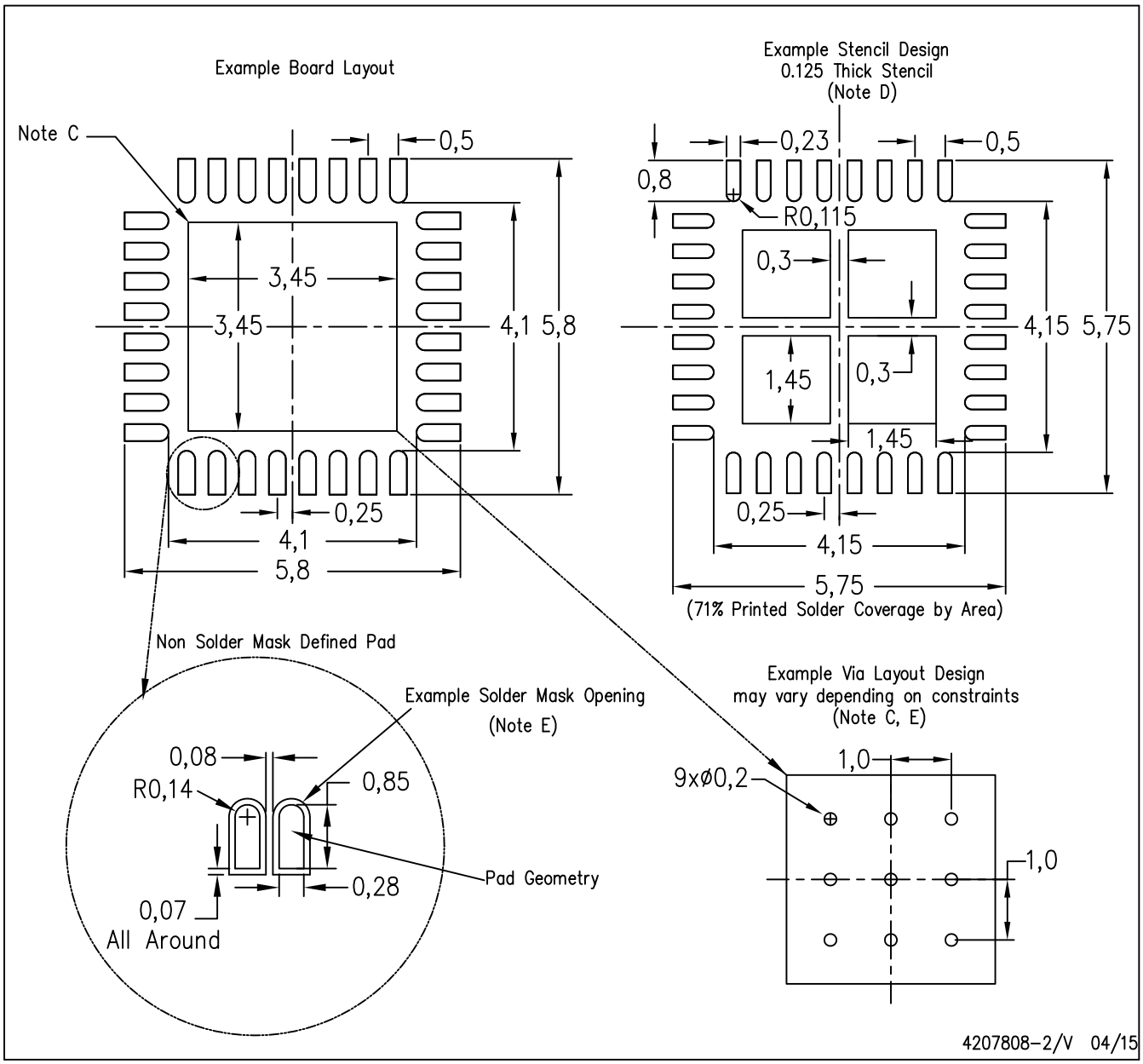
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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