

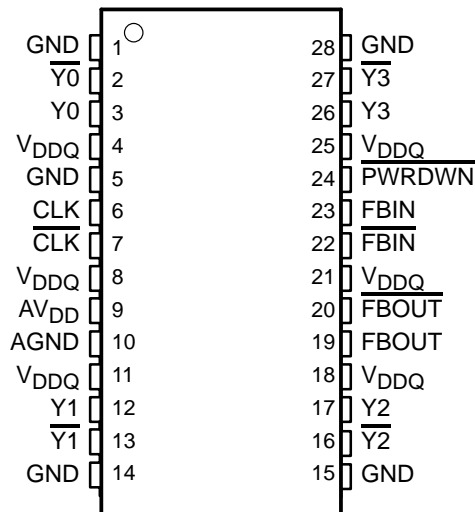
CDCV855, CDCV855I

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 180 MHz
- Low Jitter (cyc–cyc): ± 50 ps
- Distributes One Differential Clock Input to Four Differential Clock Outputs
- Enters Low Power Mode and Three-State Outputs When Input CLK Signal Is Less Than 20 MHz or PWRDWN Is Low
- Operates From Dual 2.5-V Supplies
- 28-Pin TSSOP Package
- Consumes < 200- μ A Quiescent Current
- External Feedback PIN (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks

PW PACKAGE
(TOP VIEW)



description

The CDCV855 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to four differential pairs of clock outputs (Y[0:3], $\overline{\text{Y}}[0:3]$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state), and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low-frequency condition and after applying a >20-MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When AV_{DD} is tied to GND, the PLL is turned off and bypassed for test purposes. The CDCV855 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV855 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES |
|----------------|------------------|
| | TSSOP (PW) |
| 0°C to 70°C | CDCV855PW |
| -40°C to 85°C | CDCV855IPW |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CDCV855, CDCV855I

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

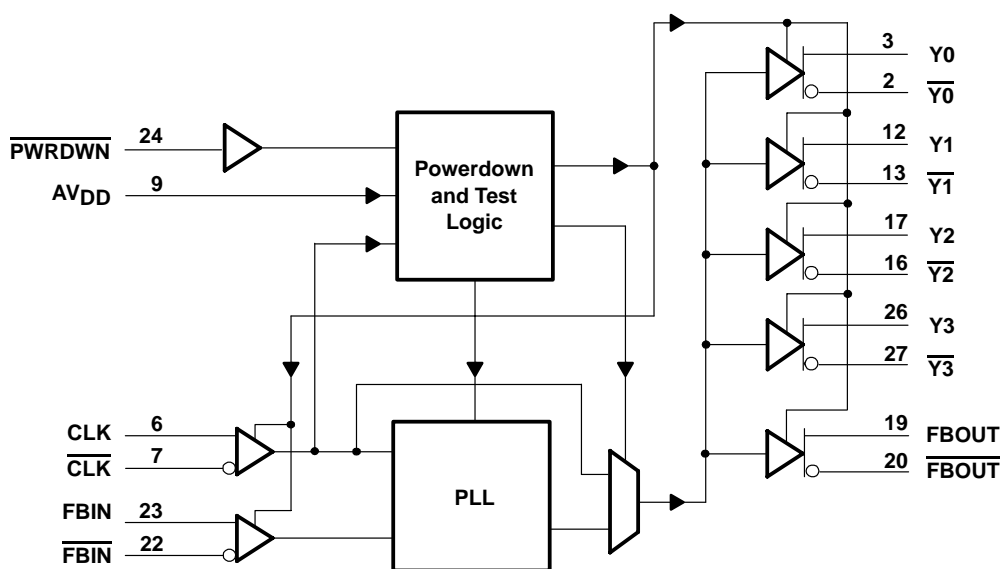
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FUNCTION TABLE
(Select Functions)

| INPUTS | | | | OUTPUTS | | | | PLL |
|-------------|--------|----------|----------|---------|--------|-------|-------|--------------|
| AVDD | PWRDWN | CLK | CLK | Y[0:3] | Y[0:3] | FBOUT | FBOUT | |
| GND | H | L | H | L | H | L | H | Bypassed/Off |
| GND | H | H | L | H | L | H | L | Bypassed/Off |
| X | L | L | H | Z | Z | Z | Z | Off |
| X | L | H | L | Z | Z | Z | Z | Off |
| 2.5 V (nom) | H | L | H | L | H | L | H | On |
| 2.5 V (nom) | H | H | L | H | L | H | L | On |
| 2.5 V (nom) | X | <20 MHz† | <20 MHz† | Z | Z | Z | Z | Off |

† Typically 10 MHz

functional block diagram



Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---------------|----------------------|-----|---|
| AGND | 10 | | Ground for 2.5-V analog supply |
| AVDD | 9 | | 2.5-V analog supply |
| CLK, CLK | 6, 7 | I | Differential clock input |
| FBIN, FBIN | 23, 22 | I | Feedback differential clock input |
| FBOUT, FBOUT | 19, 20 | O | Feedback differential clock output |
| GND | 1, 5, 14, 15, 28 | | Ground |
| PWRDWN | 24 | I | Control input to turn device in the power-down mode |
| VDDQ | 4, 8, 11, 18, 21, 25 | | 2.5-V supply |
| Y[0:3] | 3, 12, 17, 26 | O | Buffered output copies of input clock, CLK |
| Y[0:3] | 2, 13, 16, 27 | O | Buffered output copies of input clock, CLK |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

CDCV855, CDCV855I

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

| | |
|---|-----------------------------|
| Supply voltage range, V_{DDQ} , AV_{DD} | -0.5 V to 3.6 V |
| Input voltage range, V_I (see Notes 1 and 2) | -0.5 V to $V_{DDQ} + 0.5$ V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{DDQ} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DDQ}$) | ±50 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{DDQ}) | ±50 mA |
| Continuous current to GND or V_{DDQ} | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): PW package | 105.8°C/W |
| Storage temperature range T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

| | | MIN | TYP | MAX | UNIT | |
|--|---|--------------------|-------------------|-------------------|------|------|
| Supply voltage, V_{DDQ} , AV_{DD} | | 2.3 | | | 2.7 | V |
| Low-level input voltage, V_{IL} | CLK, \overline{CLK} , FBIN, \overline{FBIN} | $V_{DDQ}/2 - 0.18$ | | | V | |
| | \overline{PWRDWN} | -0.3 | 0.7 | | | |
| High-level input voltage, V_{IH} | CLK, \overline{CLK} , FBIN, \overline{FBIN} | $V_{DDQ}/2 + 0.18$ | | | V | |
| | \overline{PWRDWN} | 1.7 | $V_{DDQ} + 0.3$ | | | |
| DC input signal voltage (see Note 5) | | -0.3 | V_{DDQ} | | V | |
| Differential input signal voltage, V_{ID} (see Note 6) | CLK, FBIN | 0.36 | $V_{DDQ} + 0.6$ | | V | |
| Output differential cross-voltage, $V_{O(X)}$ (see Note 7) | | $V_{DDQ}/2 - 0.2$ | $V_{DDQ}/2$ | $V_{DDQ}/2 + 0.2$ | V | |
| Input differential pair cross-voltage, $V_{I(X)}$ (see Note 7) | | $V_{DDQ}/2 - 0.2$ | $V_{DDQ}/2 + 0.2$ | | V | |
| High-level output current, I_{OH} | | | | | -12 | mA |
| Low-level output current, I_{OL} | | | | | 12 | mA |
| Input slew rate, SR (see Figure 7) | | 1 | | | 4 | V/ns |
| Operating free-air temperature, T_A | Commercial | 0 | | | 85 | °C |
| | Industrial | -40 | | | 85 | |

- NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
 5. DC input signal voltage specifies the allowable dc execution of differential input.
 6. Differential input signal voltage specifies the differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level.
 7. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.



CDCV855, CDCV855I

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---------------------|---|--|--|---------------------|---------------------------|------|
| V _{IK} | Input voltage | All inputs V _{DDQ} = 2.3 V, I _I = -18 mA | | | -1.2 | V |
| V _{OH} | High-level output voltage | V _{DDQ} = min to max, I _{OH} = -1 mA | V _{DDQ} - 0.1 | | | V |
| | | V _{DDQ} = 2.3 V, I _{OH} = -12 mA | 1.7 | | | |
| V _{OL} | Low-level output voltage | V _{DDQ} = min to max, I _{OL} = 1 mA | | | 0.1 | V |
| | | V _{DDQ} = 2.3 V, I _{OL} = 12 mA | | | 0.6 | |
| I _{OH} | High-level output current | V _{DDQ} = 2.3 V, V _O = 1 V | -18 | -32 | | mA |
| I _{OL} | Low-level output current | V _{DDQ} = 2.3 V, V _O = 1.2 V | 26 | 35 | | mA |
| V _{OD} | Output voltage swing | Differential outputs are terminated with 120 Ω | 1.1 | | V _{DDQ} - 0.4 | V |
| V _{OX} | Output differential cross-voltage‡ | | V _{DDQ} /2 - 0.2 | V _{DDQ} /2 | V _{DDQ} /2 + 0.2 | |
| I _I | Input current | V _{DDQ} = 2.7 V, V _I = 0 V to 2.7 V | | | ±10 | μA |
| I _{OZ} | High-impedance-state output current | V _{DDQ} = 2.7 V, V _O = V _{DDQ} or GND | | | ±10 | μA |
| I _{DD(PD)} | Power-down current on V _{DDQ} + AV _{DD} | CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I _{DD} and AI _{DD} | | 100 | 200 | μA |
| I _{DD} | Dynamic current on V _{DDQ} | Differential outputs are terminated with 120 Ω / CL = 14 pF f _O = 167 MHz | | 150 | 180 | mA |
| | | | Differential outputs are terminated with 120 Ω / CL = 0 pF | | 130 | |
| AI _{DD} | Supply current on AV _{DD} | f _O = 167 MHz | | 8 | 10 | mA |
| C _I | Input capacitance | V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND | 2 | 2.5 | 3 | pF |
| C _O | Output capacitance | V _{DDQ} = 2.5 V, V _O = V _{DDQ} or GND | 2.5 | 3 | 3.5 | pF |

† All typical values are at respective nominal V_{DDQ}.

‡ Differential cross-point voltage is expected to track variation of V_{DDQ} and is the voltage at which the differential signals must be crossing.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | MIN | MAX | UNIT |
|------------------|-----------------------------------|-----|-----|------|
| f _{CLK} | Operating clock frequency | 60 | 180 | MHz |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time (PLL mode)¶ | | 10 | μs |
| | Stabilization time (Bypass mode)§ | | 30 | ns |

§ Recovery time required when the device goes from power-down mode into bypass mode (test mode with AV_{DD} at GND).

¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.



switching characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT | |
|-------------------------|--|-----------------------------|-------------|------|-----|------|----|
| t_{PLH}^{\ddagger} | Low-to-high level propagation delay time | Test mode/CLK to any output | | 4.5 | | ns | |
| t_{PHL}^{\ddagger} | High-to-low level propagation delay time | Test mode/CLK to any output | | 4.5 | | ns | |
| $t_{jit(per)}^{\S}$ | Jitter (period), See Figure 5 | 66 MHz | -55 | | 55 | ps | |
| | | 100/133/167/180 MHz | -35 | | 35 | ps | |
| $t_{jit(cc)}^{\S}$ | Jitter (cycle-to-cycle), See Figure 2 | 66 MHz | -60 | | 60 | ps | |
| | | 100/133/167/180 MHz | -50 | | 50 | | |
| $t_{jit(hper)}^{\S}$ | Half-period jitter, See Figure 6 | 66 MHz | -130 | | 130 | ps | |
| | | 100 MHz | -90 | | 90 | | |
| | | 133/167/180 MHz | -75 | | 75 | | |
| $t_{slr(o)}$ | Output clock slew rate, See Figure 7 | Load = 120 Ω / 14 pF | | 1 | 2 | V/ns | |
| | | Load = 120 Ω / 4 pF | | 1 | 3 | V/ns | |
| $t_{d(\emptyset)}^{\S}$ | Dynamic phase offset (this includes jitter), See Figure 3(b) | SSC off | 66 MHz | -180 | | 180 | ps |
| | | | 100/133 MHz | -130 | | 130 | |
| | | | 167/180 MHz | -90 | | 90 | |
| | | SSC on | 66 MHz | -230 | | 230 | |
| | | | 100/133 MHz | -170 | | 170 | |
| | | | 167/180 MHz | -100 | | 100 | |
| $t_{(\emptyset)}$ | Static phase offset, See Figure 3(a) | 66 MHz | -150 | | 150 | ps | |
| | | 100/133/167/180 MHz | -100 | | 100 | | |
| $tsk(o)^{\parallel}$ | Output skew, See Figure 4 | | | | 50 | ps | |
| t_r, t_f | Output rise and fall times (20% – 80%) | Load: 120 Ω /14 pF | | 650 | 900 | ps | |

† All typical values are at a respective nominal V_{DDQ} .

‡ Refers to transition of noninverting output

§ This parameter is assured by design but can not be 100% production tested.

¶ All differential output pins are terminated with 120 Ω /14 pF.

CDCV855, CDCV855I 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

PARAMETER MEASUREMENT INFORMATION

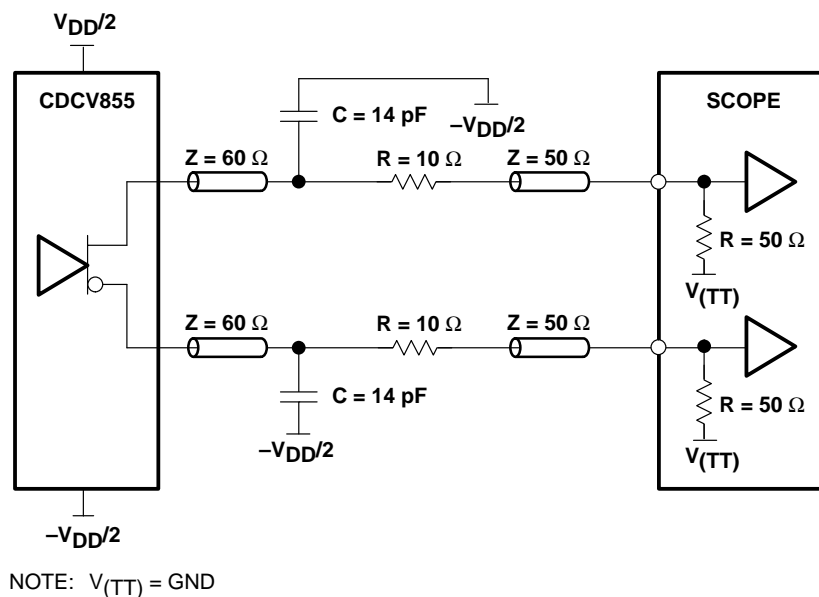


Figure 1. Output Load Test Circuit

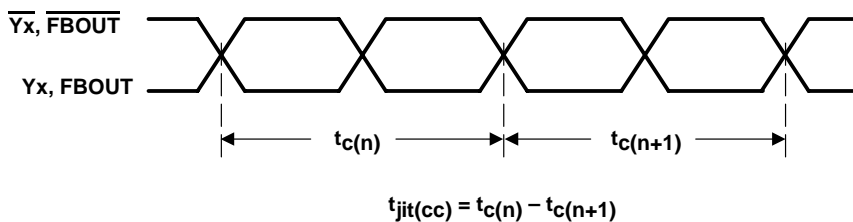


Figure 2. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

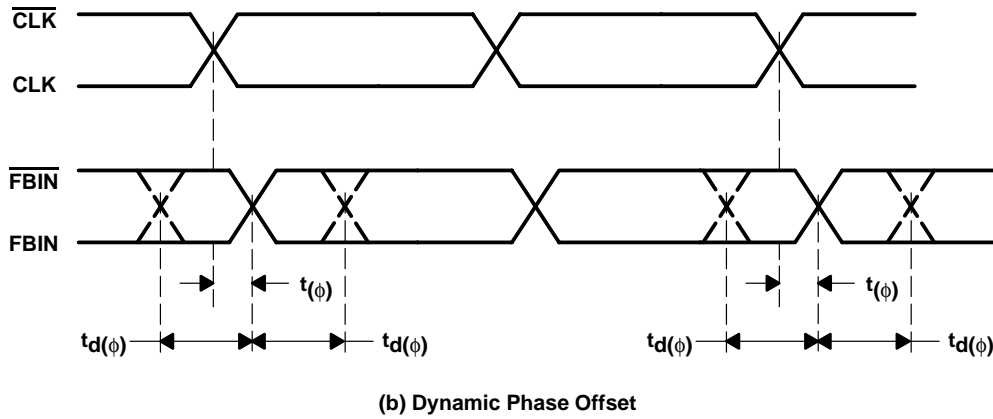
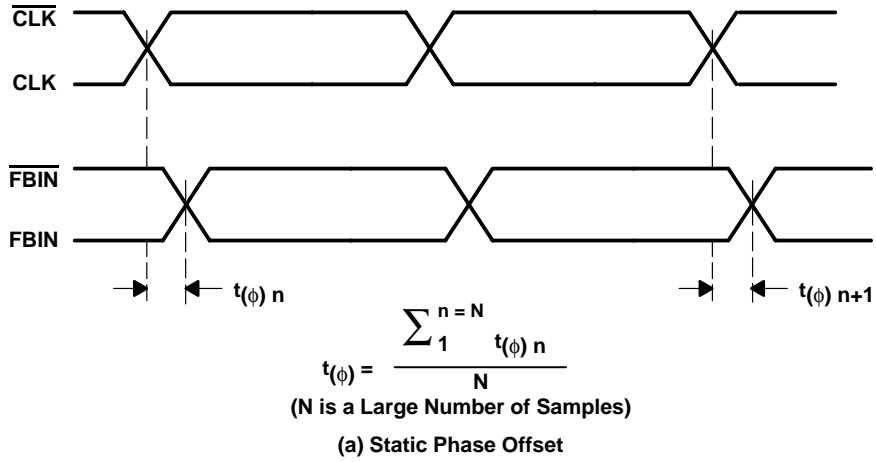


Figure 3. Phase Offset

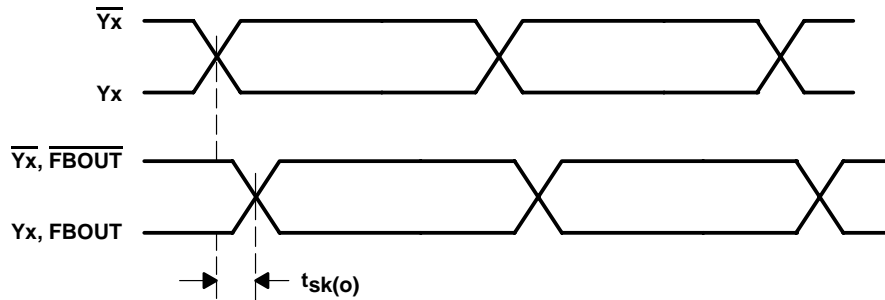


Figure 4. Output Skew

CDCV855, CDCV855I

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS660A – SEPTEMBER 2001 – REVISED DECEMBER 2002

PARAMETER MEASUREMENT INFORMATION

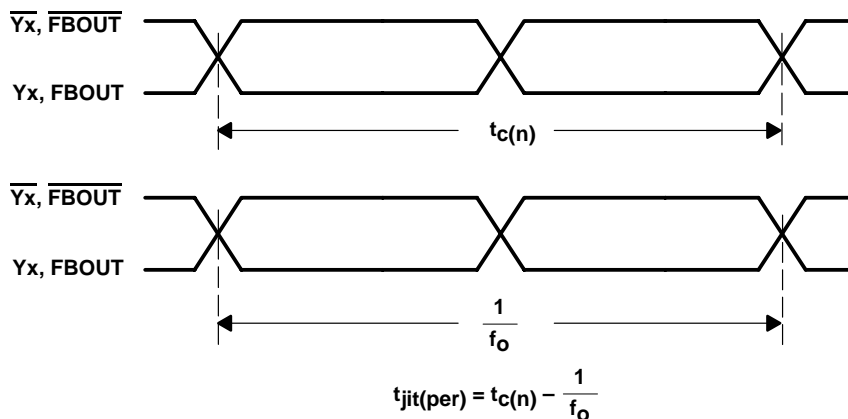


Figure 5. Period Jitter

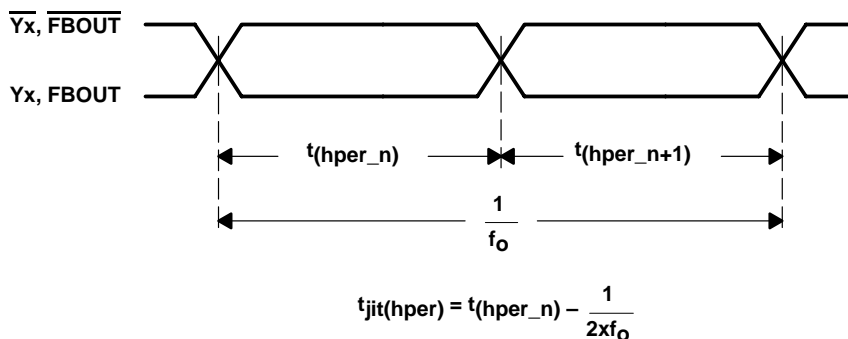


Figure 6. Half-Period Jitter

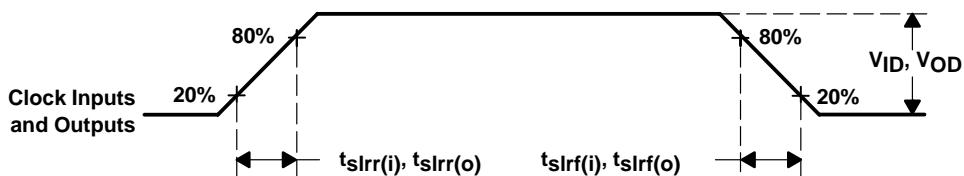


Figure 7. Input and Output Slew Rates

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|---------|
| CDCV855IPW | NRND | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCV855-I | |
| CDCV855IPWG4 | NRND | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCV855-I | |
| CDCV855IPWR | NRND | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCV855-I | |
| CDCV855IPWRG4 | NRND | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCV855-I | |
| CDCV855PW | NRND | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CDCV855 | |
| CDCV855PWG4 | NRND | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CDCV855 | |
| CDCV855PWR | NRND | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CDCV855 | |
| CDCV855PWRG4 | NRND | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CDCV855 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCV855IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| CDCV855PWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

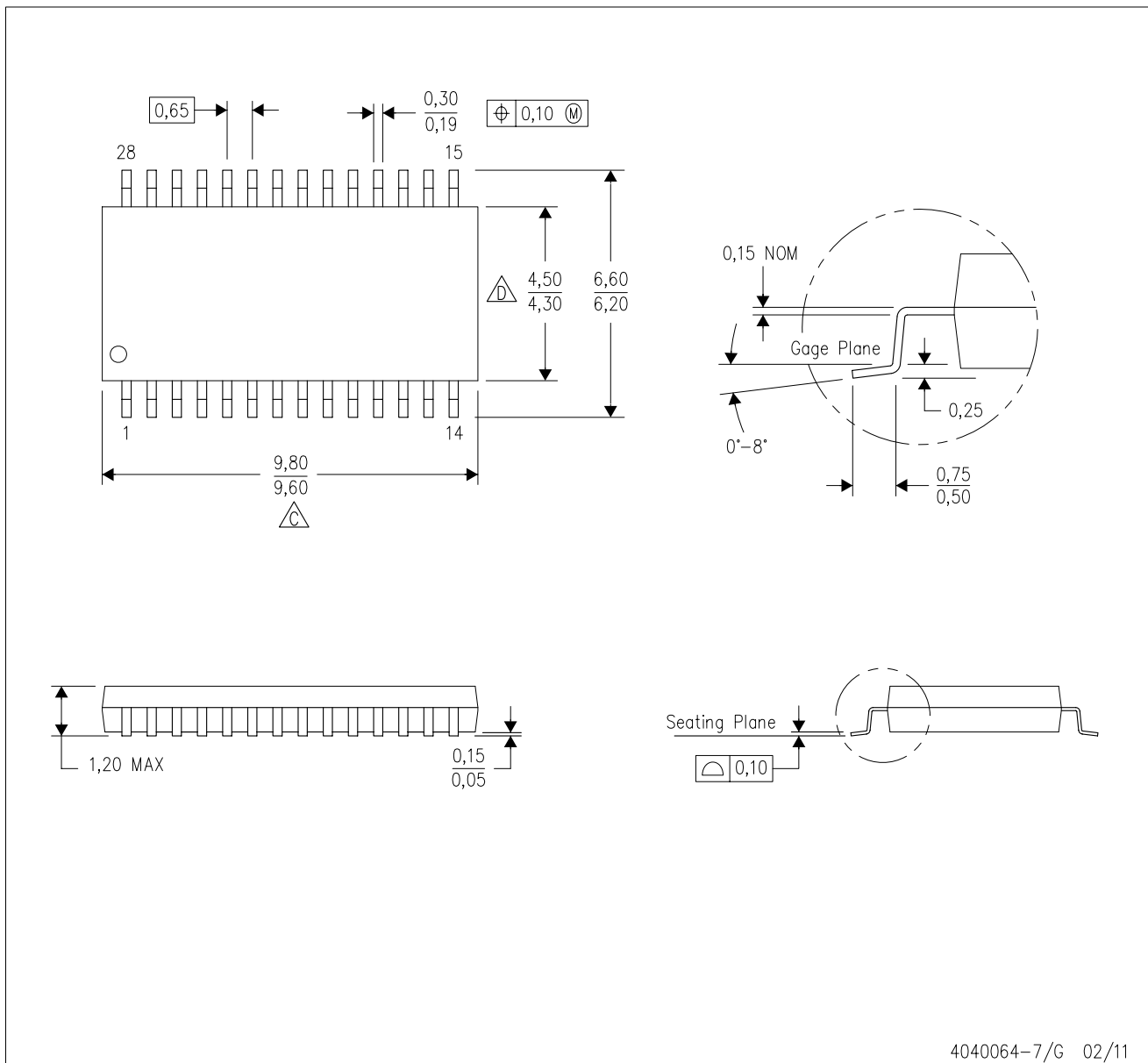
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCV855IPWR | TSSOP | PW | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| CDCV855PWR | TSSOP | PW | 28 | 2000 | 367.0 | 367.0 | 38.0 |

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

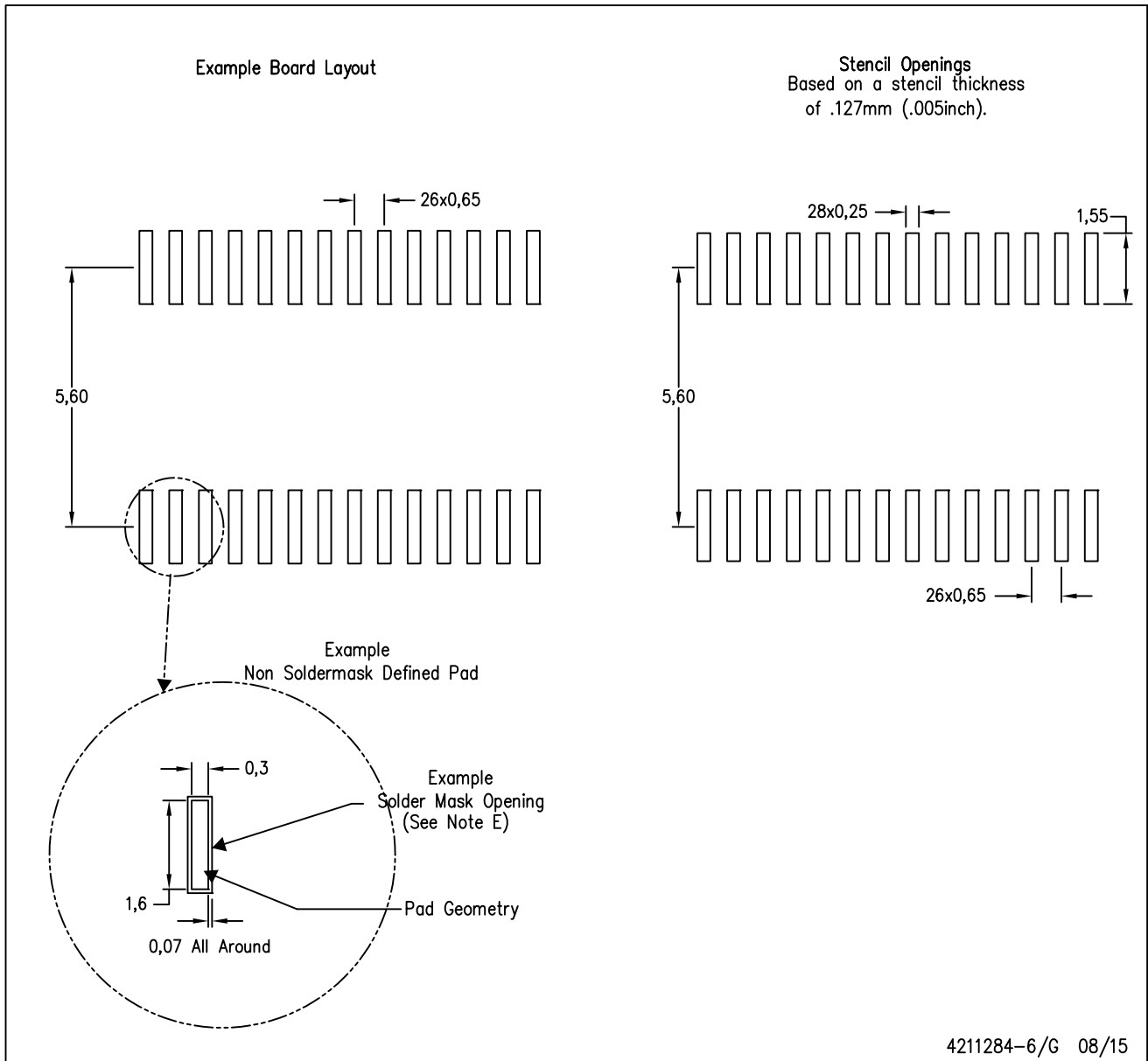


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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