- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29520
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Single- and Dual-Pipeline Operation Modes
- Multiplexed Data Inputs and Outputs
- CY29FCT520T
  - 64-mA Output Sink Current
    32-mA Output Source Current
- CY29FCT520ATDMB, CY29FCT520BTDMB
  - 32-mA Output Sink Current
    12-mA Output Source Current
- 3-State Outputs

D, P, OR SO PACKAGE
(TOP VIEW)

I_0	1	24	V_{CC}
I_1	2	23	S_0
D_0	3	22	S_1
D_1	4	21	Y_0
D_2	5	20	Y_1
D_3	6	19	Y_2
D_4	7	18	Y_3
D_5	8	17	Y_4
D_6	9	16	Y_5
D_7	10	15	Y_6
CLK	11	14	Y_7
GND	12	13	$\overline{OE}$
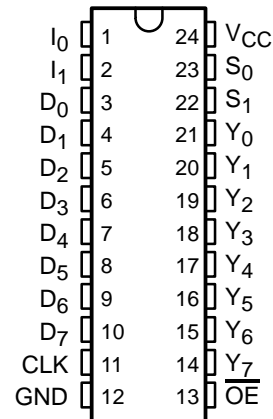
description

The CY29FCT520T is a multilevel 8-bit-wide pipeline register. The device consists of four registers, A1, A2, B1, and B2, which are configured by the instruction inputs I_0, I_1 as a single four-level pipeline or as two two-level pipelines. The contents of any register can be read at the multiplexed output at any time by using the multiplex-selection controls (S_0 and S_1).

The pipeline registers are positive-edge triggered, and data is shifted by the rising edge of the clock input. Instruction I = 0 selects the four-level pipeline mode. Instruction I = 1 selects the two-level B pipeline, while I = 2 selects the two-level A pipeline. I = 3 is the hold instruction; no shifting is performed by the clock in this mode.

In the two-level operation mode, data is shifted from level 1 to level 2 and new data is loaded into level 1.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

CY29FCT520T
MULTILEVEL PIPELINE REGISTER
WITH 3-STATE OUTPUTS

SCCS011C – MAY 1994 – REVISED NOVEMBER 2001

PIPELINE INSTRUCTION TABLE

I = 0		I = 1		I = 2		I = 3	
$I_1 = 0$	$I_0 = 0$	$I_1 = 0$	$I_0 = 1$	$I_1 = 1$	$I_0 = 0$	$I_1 = 1$	$I_0 = 1$
A1	B1	A1	B1	A1	B1	A1	B1
A2	B2	A2	B2	A2	B2	A2	B2
Single four-level		Dual two-level				Hold	

ORDERING INFORMATION

| T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – SO	Tube	6.0	CY29FCT520CTSOC	29FCT520C
		Tape and reel	6.0	CY29FCT520CTSOCT	
	SOIC – SO	Tube	7.5	CY29FCT520BTSOC	29FCT520B
		Tape and reel	7.5	CY29FCT520BTSOCT	
	DIP – P	Tube	14.0	CY29FCT520ATPC	CY29FCT520ATPC
	SOIC – SO	Tube	14.0	CY29FCT520ATSOC	29FCT520A
		Tape and reel	14.0	CY29FCT520ATSOCT	
−55°C to 125°C	CDIP – D	Tube	8.0	5962-9220504MLA (CY29FCT520BTDMB)	
		Tube	16.0	5962-9220502MLA (CY29FCT520ATDMB)	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OUTPUT
S_1	S_0	
1	1	A1
1	0	A2
0	1	B1
0	0	B2

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram
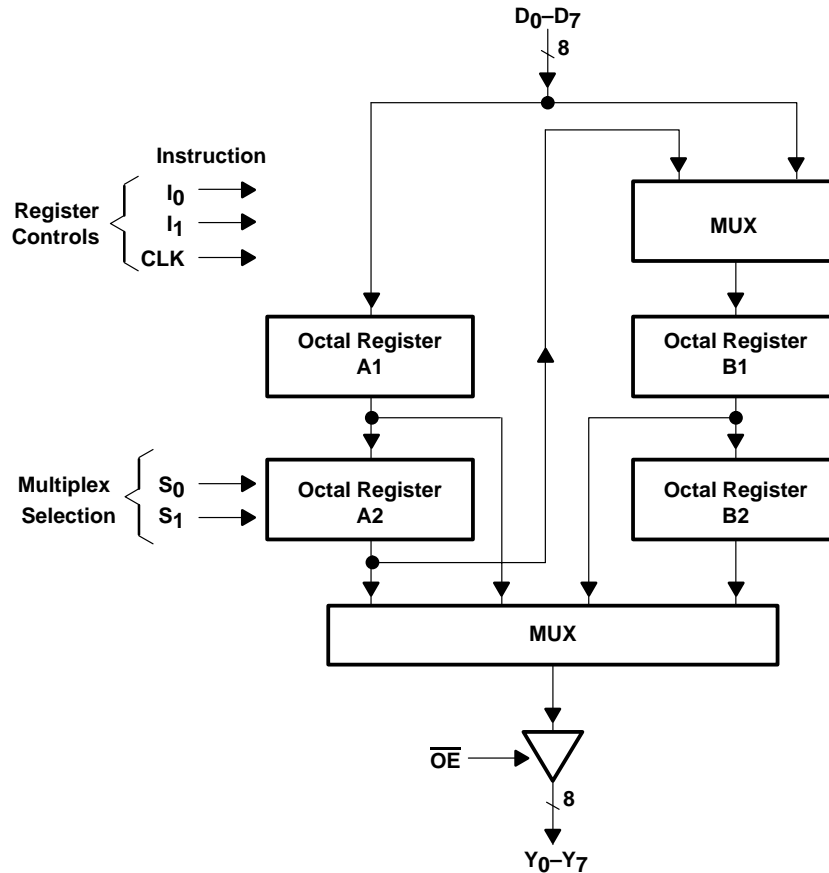
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential .... –0.5 V to 7 V
DC input voltage range .... –0.5 V to 7 V
DC output voltage range .... –0.5 V to 7 V
DC output current (maximum sink current/pin) .... 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package .... 67°C/W
(see Note 2): SO package .... 46°C/W
Ambient temperature range with power applied, T_A .... –65°C to 135°C
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
        2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

PARAMETER		CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
			MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = −18 mA		−0.7	−1.2				V
	V_{CC} = 4.75 V,	I_{IN} = −18 mA					−0.7	−1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = −15 mA				2.4	3.3		
		I_{OH} = −32 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{OS}[‡]	V_{CC} = 5.5 V,	V_{OUT} = 0 V	−60	−120	−225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				−60	−120	−225	
I_{OZH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			10				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			−10				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						−10	
I_{CC}	V_{CC} = 5.5 V, $V_{IN} \leq$ 0.2 V,	$V_{IN} \geq V_{CC}$ − 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V, $V_{IN} \leq$ 0.2 V,	$V_{IN} \geq V_{CC}$ − 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V[§], f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V[§], f_1 = 0, Outputs open						0.5	2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CCD}¶	V_{CC} = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V						0.06	0.12	
I_C#	V_{CC} = 5.5 V, Outputs open, f_0 = 10 MHz, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V		2.8	5.6‖				
			V_{IN} = 3.4 V or GND		5.1	14.3‖				
	V_{CC} = 5.25 V, Outputs open, f_0 = 10 MHz, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					2.8	5.6‖	
			V_{IN} = 3.4 V or GND					5.1	14.3‖	
C_i			5		10	5		10	pF
C_o			9		12	9		12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ This parameter is derived for use in total power-supply calculations.

\# I_C = $I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$
   Where:

   I_C = Total supply current
   I_{CC} = Power-supply current with CMOS input levels
   ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
   D_H = Duty cycle for TTL inputs high
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

CY29FCT520T
MULTILEVEL PIPELINE REGISTER
WITH 3-STATE OUTPUTS
SCCS011C – MAY 1994 – REVISED NOVEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			CY29FCT520ATDMB		CY29FCT520BTDMB		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		8		6		ns
t_{su}	Setup time, before CLK↑	Data	6		2.8		ns
		I	6		4.5		
t_h	Hold time, after CLK↑	Data	2		2		ns
		I	2		2		

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			CY29FCT520AT		CY29FCT520BT		CY29FCT520CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		7		5.5		5.5		ns
t_{su}	Setup time, before CLK↑	Data	5		2.5		2.5		ns
		I	5		4		4		
t_h	Hold time, after CLK↑	Data	2		2		2		ns
		I	2		2		2		

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT520ATDMB		CY29FCT520BTDMB		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Y	2	16	2	8	ns
t_{PHL}			2	16	2	8	
t_{PLH}	S_0 or S_1	Y	2	15	2	8	ns
t_{PHL}			2	15	2	8	
t_{PHZ}	$\overline{OE}$	Y	1.5	13	1.5	7.5	ns
t_{PLZ}			1.5	13	1.5	7.5	
t_{PZH}	$\overline{OE}$	Y	1.5	16	1.5	8	ns
t_{PZL}			1.5	16	1.5	8	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT520AT		CY29FCT520BT		CY29FCT520CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Y	2	14	2	7.5	2	6	ns
t_{PHL}			2	14	2	7.5	2	6	
t_{PLH}	S_0 or S_1	Y	2	13	2	7.5	2	6	ns
t_{PHL}			2	13	2	7.5	2	6	
t_{PHZ}	$\overline{OE}$	Y	1.5	12	1.5	7	1.5	6	ns
t_{PLZ}			1.5	12	1.5	7	1.5	6	
t_{PZH}	$\overline{OE}$	Y	1.5	15	1.5	7.5	1.5	6	ns
t_{PZL}			1.5	15	1.5	7.5	1.5	6	

TEXAS
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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING
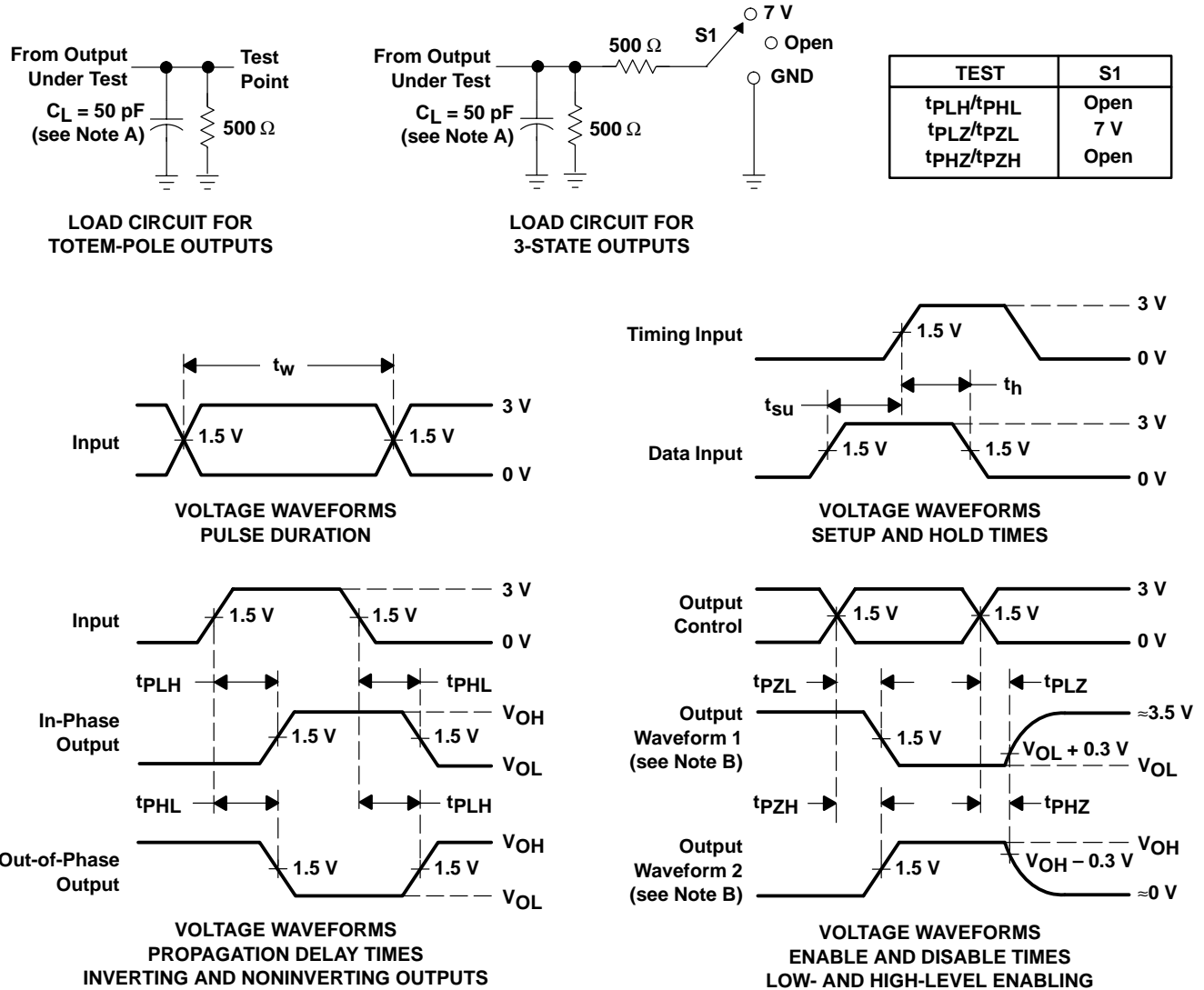
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9220502MLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220502MLA	Samples
5962-9220504MLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9220504MLA	Samples
CY29FCT520ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520A	Samples
CY29FCT520BTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JT (R-GDIP-T**)   **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN

	PINS **	24	28
DIM			
A MAX		1.280 (32,51)	1.460 (37,08)
A MIN		1.240 (31,50)	1.440 (36,58)
B MAX		0.300 (7,62)	0.291 (7,39)
B MIN		0.245 (6,22)	0.285 (7,24)

0.070 (1,78) / 0.030 (0,76)

0.100 (2,54) MAX   0.015 (0,38) MIN

0.320 (8,13) / 0.290 (7,37)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58) / 0.015 (0,38)

0.100 (2,54)

0°–15°

0.014 (0,36) / 0.008 (0,20)

4040110/C 08/96
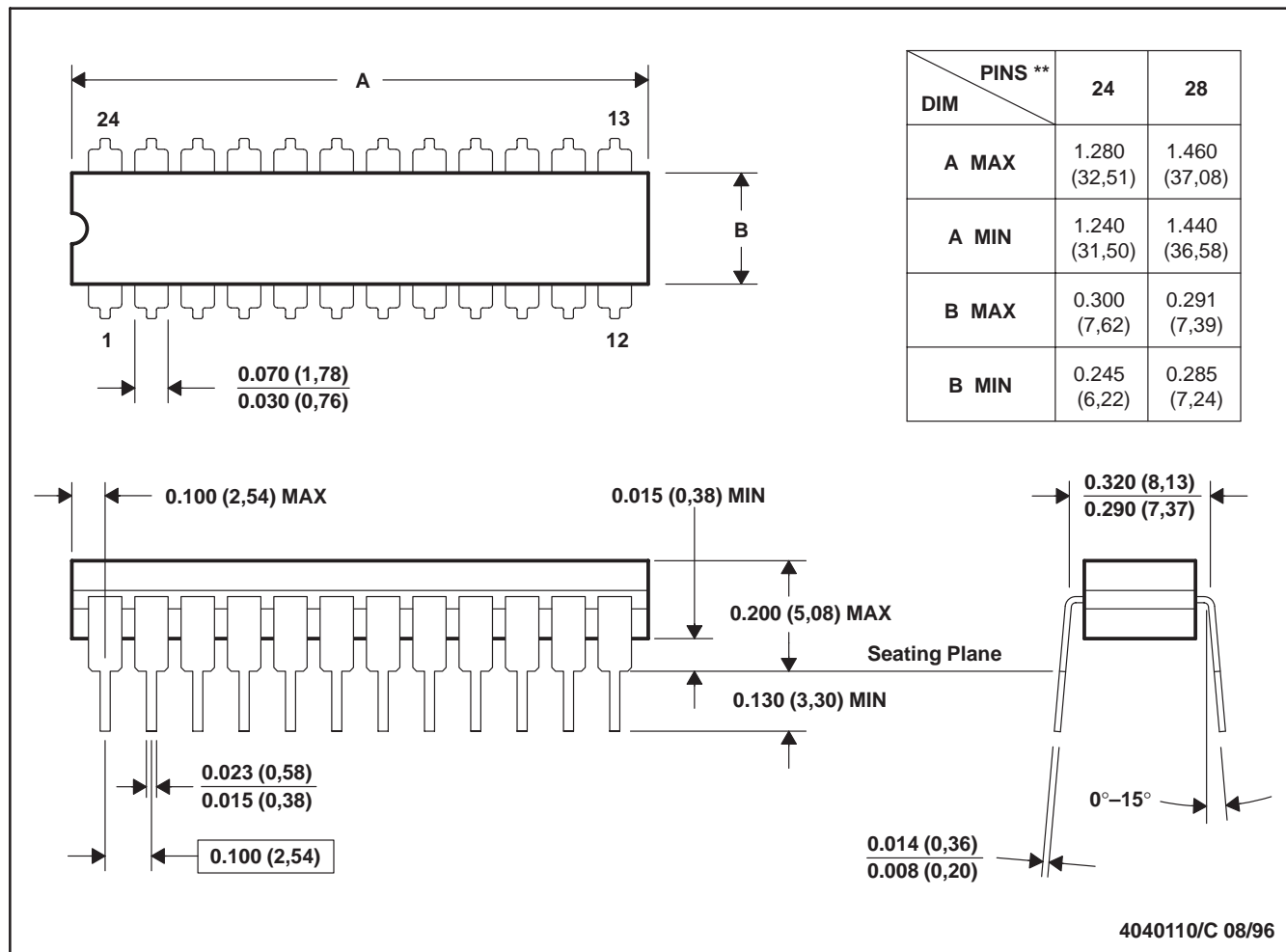
NOTES: A.   All linear dimensions are in inches (millimeters).
  B.   This drawing is subject to change without notice.
  C.   This package can be hermetically sealed with a ceramic lid using glass frit.
  D.   Index point is provided on cap for terminal identification.
  E.   Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

$\dfrac{0.614\ (15,60)}{0.598\ (15,20)}$

24   13

$\dfrac{0.419\ (10,63)}{0.393\ (9,97)}$

$\dfrac{0.299\ (7,60)}{0.291\ (7,40)}$

1   12

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\dfrac{0.012\ (0,30)}{0.004\ (0,10)}$

$\dfrac{0.013\ (0,33)}{0.008\ (0,20)}$

⌐ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

IMPORTANT NOTICE