# 16-Bit, Single-Channel, ±18V Output (Unbuffered), Ultra-Low Power, Serial Interface DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- **16-Bit Resolution**
- **Output: ±18V for ±18V Reference Input**
- **±18V Supply Operation**
- **Very Low Power**
- **High Accuracy INL: 1LSB**
- **Low Noise: 10nV/√Hz**
- **Fast Settling: 1μs to 1LSB**
- **Fast SPI™ Interface: Up To 50MHz**
- **16-Pin TSSOP Package**
- **Selectable Reset to Zero or Midscale**

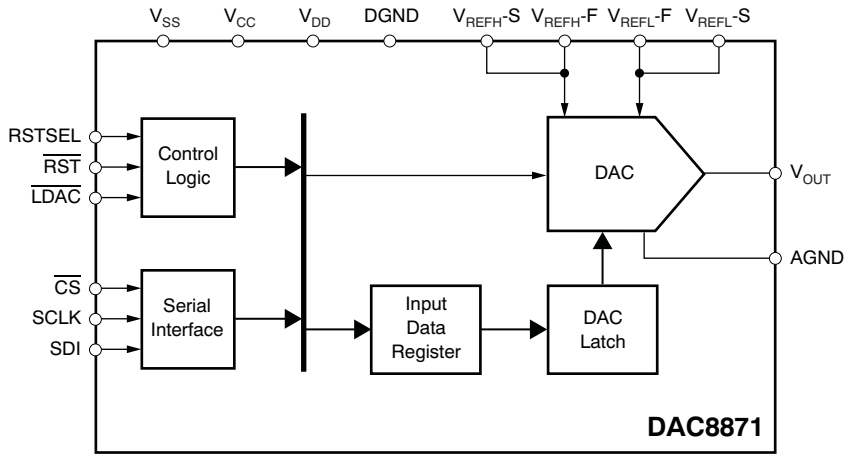
## APPLICATIONS

- **Portable Equipment**
- **Automatic Test Equipment**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Optical Networking**

## DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial input, voltage output digital-to-analog converter (DAC). The output range is determined by the reference voltage, $V_{REFH}$ and $V_{REFL}$. By properly selecting the reference, the output can be unipolar or bipolar, and up to ±18V. The DAC8871 provides excellent linearity (1LSB INL), low noise, and fast settling (1μs to 1LSB of full scale output) over the specified temperature range of –40°C to +105°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. This device features a standard high-speed clock (up to 50MHz), and a 3V or 5V SPI serial interface to communicate with the DSP or microprocessors. For optimum performance, a set of Kelvin connections to external reference are provided.

The DAC8871 is available in a TSSOP-16 package.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | MINIMUM RELATIVE ACCURACY (LSB) | DIFFERENTIAL NONLINEARITY (LSB) | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | PACKAGE-LEAD | PACKAGE DESIGNATOR |
|---|---|---|---|---|---|---|
| DAC8871B | ±1 | ±1 | –40°C to +105°C | 8871 | TSSOP-16 | PW |
| DAC8871 | ±3 | ±1 | –40°C to +105°C | 8871 | TSSOP-16 | PW |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | DAC8871 | UNIT |
|---|---|---|---|
| $V_{DD}$ to GND | | –0.3 to +7 | V |
| Digital input voltage to GND | | –0.3 to ($V_{DD}$ + 0.3) | V |
| AGND to DGND | | –0.3 to +0.3 | V |
| $V_{CC}$ to $V_{SS}$ | | –0.3 to +39.6 | V |
| $V_{CC}$ to AGND | | –0.3 to +19.8 | V |
| $V_{SS}$ to AGND | | +0.3 to –19.8 | V |
| $V_{REFH}$ to $V_{REFL}$ | | –0.3 to +39.6 | V |
| $V_{REFH}$ to AGND | | –0.3 to +19.8 | V |
| $V_{REFL}$ to AGND | | –19.8 to +17.5 | V |
| Operating temperature range | | –40 to +105 | °C |
| Storage temperature range | | –65 to +150 | °C |
| Maximum junction temperature ($T_J$ max) | | +150 | °C |
| Power dissipation | | ($T_J$ max - $T_A$)/$\theta_{JA}$ | W |
| Thermal impedance, $\theta_{JA}$ | TSSOP-16 | 161.4 | C/W |

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, $V_{REFL}$ = –10V, and $V_{DD}$ = +5V, unless otherwise noted; specifications subject to change without notice.

| PARAMETER | | CONDITIONS | DAC8871 MIN | DAC8871 TYP | DAC8871 MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | |
| Resolution | | | 16 | | | Bits |
| Linearity error | DAC8871B | $V_{REFH}$ = 10V, $V_{REFL}$ = –5V | | ±0.75 | ±1 | LSB |
| | | $V_{REFH}$ = 10V, $V_{REFL}$ = –10V | | ±1 | ±1.5 | LSB |
| | DAC8871 | | | ±1 | ±3 | LSB |
| Differential linearity error | | | | ±0.25 | ±1 | LSB |
| Gain error | | $T_A$ = +25°C | | ±0.5 | 2 | LSB |
| Gain drift | | | | ±0.1 | | ppm/°C |
| Bipolar zero error | | $T_A$ = +25°C | | ±1 | ±4 | LSB |
| Bipolar drift | | | | ±0.1 | | ppm/°C |
| Zero code error | | $T_A$ = +25°C | | ±0.5 | ±2 | LSB |
| Zero code drift | | | | ±0.05 | | ppm/°C |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Voltage output | | | $V_{REFL}$ | | $V_{REFH}$ | V |
| Output impedance | | | | 6.25 | | kΩ |
| Settling time | | To 1LSB of FS, $C_L$ = 15 pF | | 1 | | µs |
| Slew rate(1) | | $C_L$ = 15pF | | 40 | | V/µs |
| Digital feedthrough(2) | | | | 0.2 | | nV-s |
| Output noise | | $T_A$ = +25°C | | 10 | | nV/√Hz |
| Power supply rejection | | Supplies vary ±10% | | | 1 | LSB |
| **REFERENCE INPUT** | | | | | | |
| $V_{REFH}$ | Ref high input voltage range | | 0 | | +18 | V |
| $V_{REFL}$ | Ref low input voltage range | | –18 | | $V_{REFH}$ – 1.25 | V |
| Ref high input current | | | | 1.3 | | mA |
| Ref low input current | | | | –1.3 | | mA |
| Reference input impedance(3) | | | 7.5 | | | kΩ |
| Reference input capacitance | | Code = 0000h | | 75 | | pF |
| | | Code = FFFFh | | 120 | | pF |
| **DIGITAL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | $V_{DD}$ = +5V | DGND | | 0.8 | V |
| | | $V_{DD}$ = +3V | DGND | | 0.6 | V |
| $V_{IH}$ | Input high voltage | $V_{DD}$ = +5V | 2.6 | | $V_{DD}$ | V |
| | | $V_{DD}$ = +3V | 2.1 | | $V_{DD}$ | V |
| Input current | | | | | ±1 | µA |
| Input capacitance | | | | | 10 | pF |

(1) Slew Rate is measured from 10% to 90% of transition when the output changes from 0 to full scale.
(2) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; $\overline{CS}$ is held high, while SCLK and DIN signals are toggled. It is specified with a full-scale code change on the SDI bus (that is, from all 0s to all 1s and vice versa).
(3) Reference input resistance is code-dependent, with a minimum at 8555h

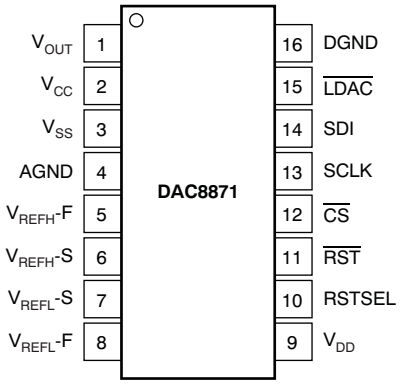
## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, $V_{REFL}$ = –10V, and $V_{DD}$ = +5V, unless otherwise noted; specifications subject to change without notice.

| PARAMETER | CONDITIONS | DAC8871 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | |
| $V_{CC}$ | | +13.5 | +15 | +19.8 | V |
| $V_{SS}$ | | –19.8 | –15 | –13.5 | V |
| $V_{DD}$ | | +2.7 | | +5.5 | V |
| $I_{CC}$ | | | 0.01 | 2 | µA |
| $I_{SS}$ | | | –0.01 | –2 | µA |
| $I_{DD}$ | | | 3 | 10 | µA |
| Power | | | 15 | 30 | µW |
| **TEMPERATURE RANGE** | | | | | |
| Specified performance | | –40 | | +105 | °C |

## PIN CONFIGURATION (NOT TO SCALE)

**PW PACKAGE**
**TSSOP-16**
**(TOP VIEW)**




## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 1 | $V_{OUT}$ | Analog output of the DAC |
| 2 | $V_{CC}$ | Positive analog power supply: +15V |
| 3 | $V_{SS}$ | Negative analog power supply: –15V |
| 4 | AGND | Analog ground |
| 5 | $V_{REFH}$-F | $V_{REFH}$ reference input (Force). Connect to external $V_{REFH}$. |
| 6 | $V_{REFH}$-S | $V_{REFH}$ reference input (Sense). Connect to external $V_{REFH}$. |
| 7 | $V_{REFL}$-S | $V_{REFL}$ reference input (Sense). Connect to external $V_{REFL}$. |
| 8 | $V_{REFL}$-F | $V_{REFL}$ reference input (Force). Connect to external $V_{REFL}$. |
| 9 | $V_{DD}$ | Digital power. +5V for 5V interface logic; +3V for 3V logic. |
| 10 | RSTSEL | Power-On-Reset select. Determines $V_{OUT}$ after power-on reset. If tied to $V_{DD}$, the DAC latch is set to mid-scale after power-on, and $V_{OUT}$ is ($V_{REFH}$ – $V_{REFL}$)/2. If tied to DGND, the DAC latch is cleared ('0'), and $V_{OUT}$ is $V_{REFL}$. |
| 11 | $\overline{RST}$ | Reset (active low) |
| 12 | $\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low. |
| 13 | SCLK | Serial clock input |
| 14 | SDI | Serial data input. Data are latched into input register on the rising edge of SCLK. |
| 15 | $\overline{LDAC}$ | Load DAC control input (active low). When $\overline{LDAC}$ is low, the DAC latch is simultaneously updated with the content of the input register. |
| 16 | DGND | Digital ground |

## TIMING DIAGRAMS

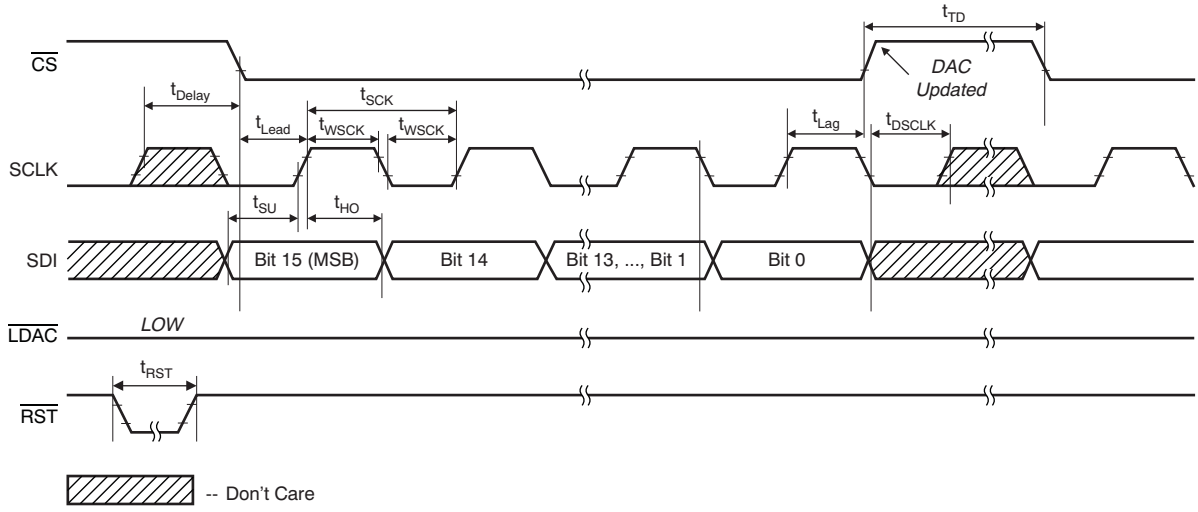



**Figure 1. Case 1—$\overline{\text{LDAC}}$ Tied Low**

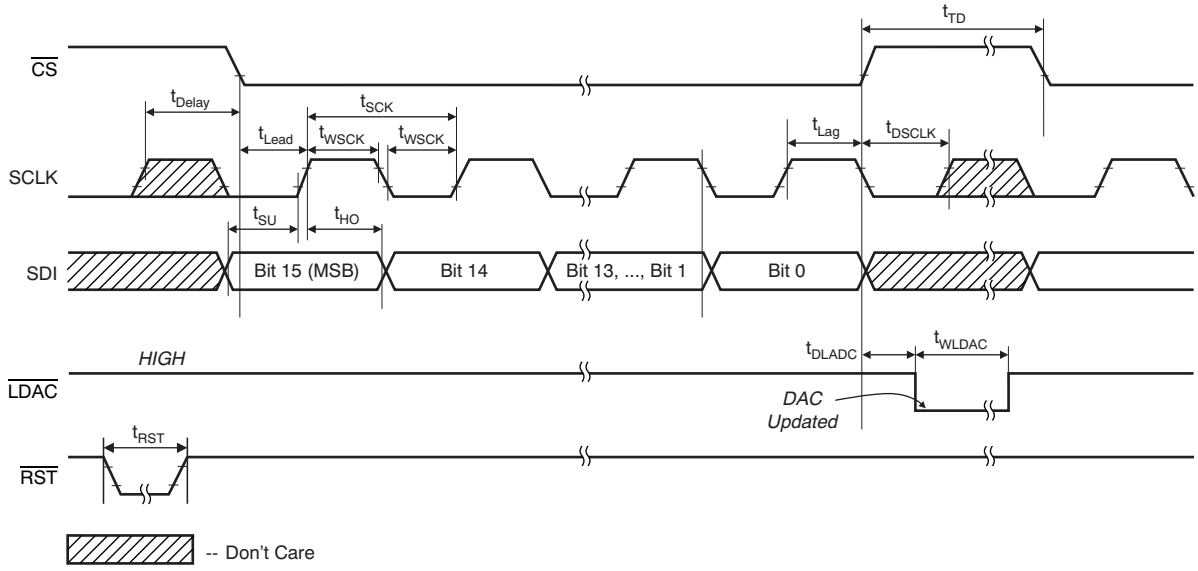



**Figure 2. Case 2—$\overline{\text{LDAC}}$ Active**

## TIMING CHARACTERISTICS: $V_{DD}$ = +5V(1) (2)

At –40°C to +105°C, unless otherwise noted.

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{SCK}$ | SCLK period | 20 | | ns |
| $t_{WSCK}$ | SCLK high or low time | 10 | | ns |
| $t_{Delay}$ | Delay from SCLK high to $\overline{CS}$ low | 10 | | ns |
| $t_{Lead}$ | $\overline{CS}$ enable lead time | 10 | | ns |
| $t_{Lag}$ | $\overline{CS}$ enable lag time | 10 | | ns |
| $t_{DSCLK}$ | Delay from $\overline{CS}$ high to SCLK high | 10 | | ns |
| $t_{TD}$ | $\overline{CS}$ high between active period | 30 | | ns |
| $t_{SU}$ | Data setup time (input) | 10 | | ns |
| $t_{HO}$ | Data hold time (input) | 0 | | ns |
| $t_{WLDAC}$ | $\overline{LDAC}$ width | 30 | | ns |
| $t_{DLDAC}$ | Delay from $\overline{CS}$ high to $\overline{LDAC}$ low | 30 | | ns |
| $t_{RST}$ | Reset ($\overline{RST}$) low | 10 | | ns |
| | $V_{DD}$ high to $\overline{CS}$ low (power-up delay) | 10 | | µs |

(1) Assured by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

**LINEARITY ERROR vs DIGITAL INPUT CODE**

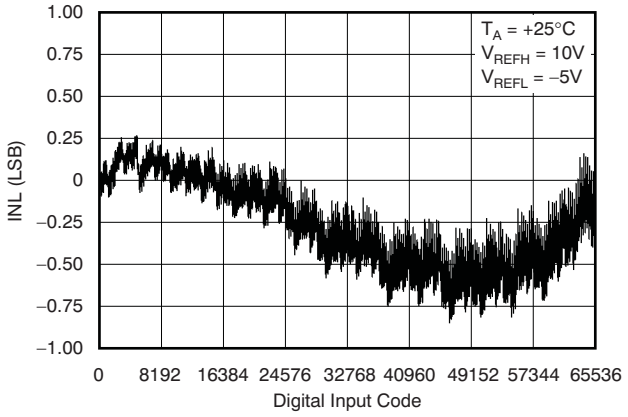



**Figure 3.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**

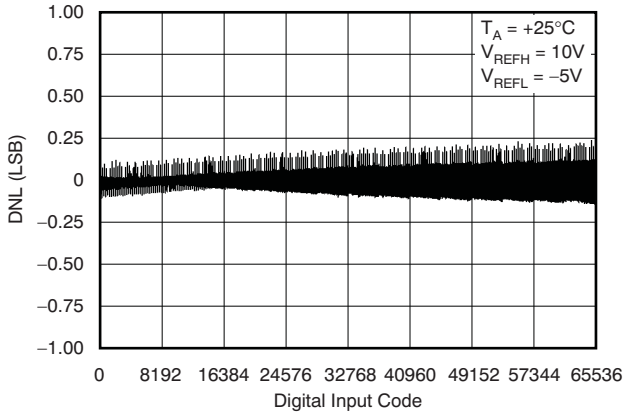



**Figure 4.**

**LINEARITY ERROR vs DIGITAL INPUT CODE**

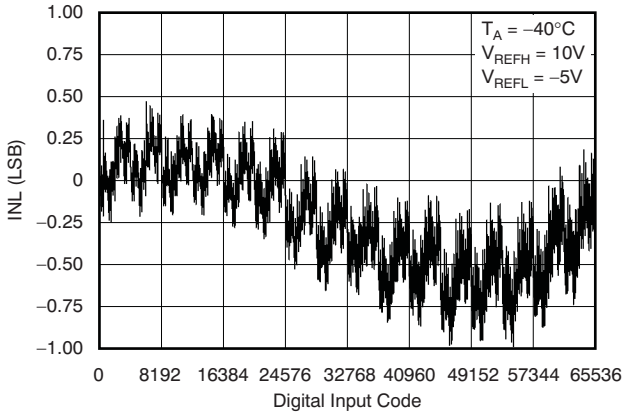



**Figure 5.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**

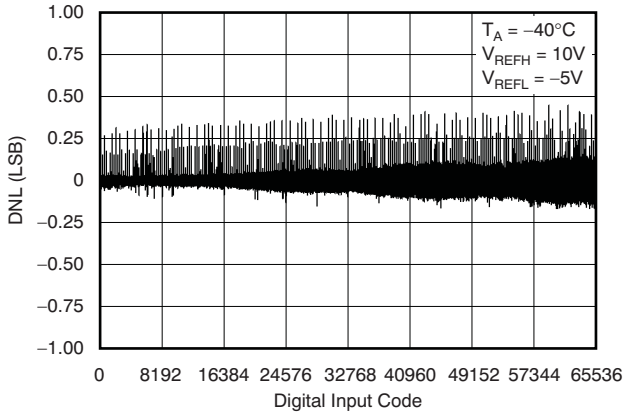



**Figure 6.**

**LINEARITY ERROR vs DIGITAL INPUT CODE**

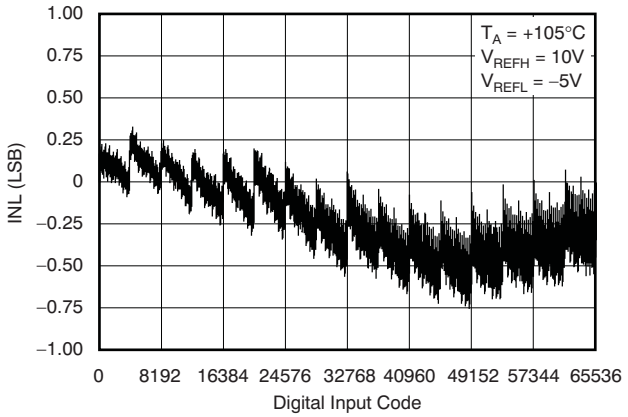



**Figure 7.**

**DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE**

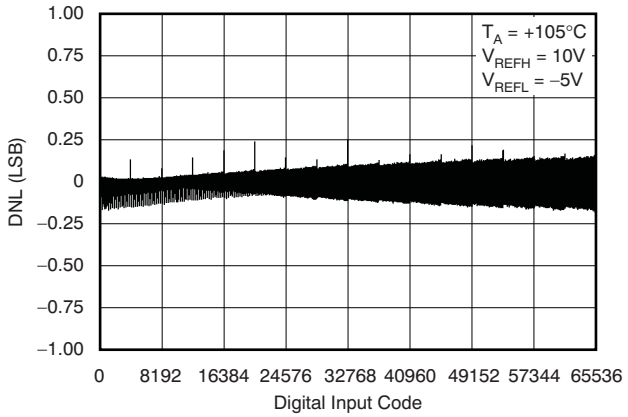



**Figure 8.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

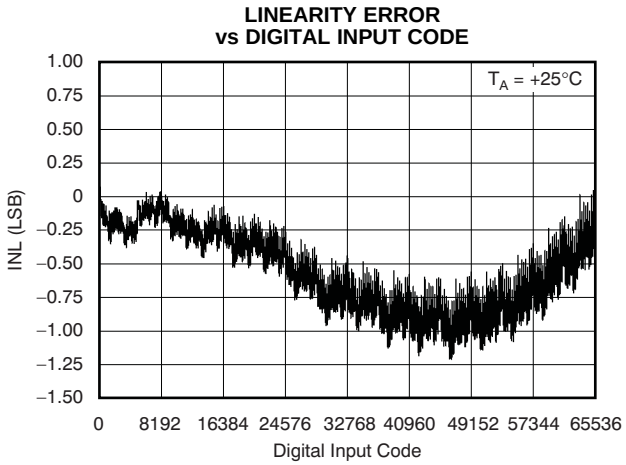



**Figure 9.**

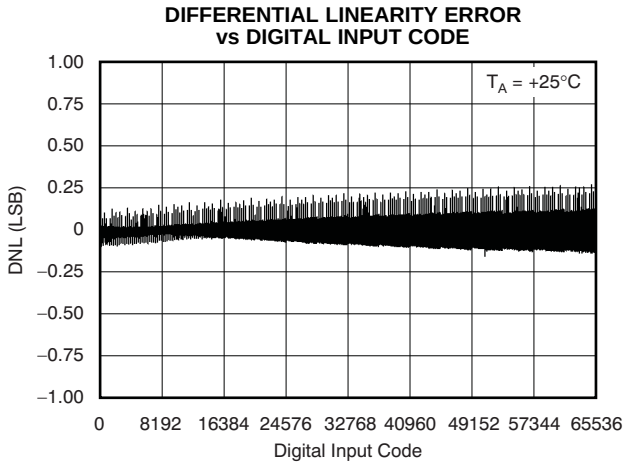



**Figure 10.**

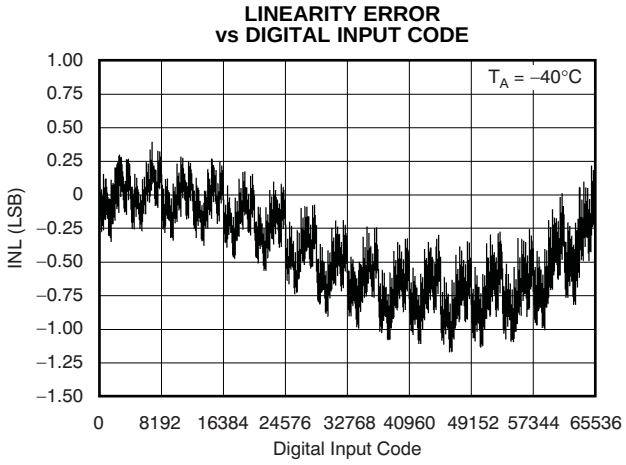



**Figure 11.**

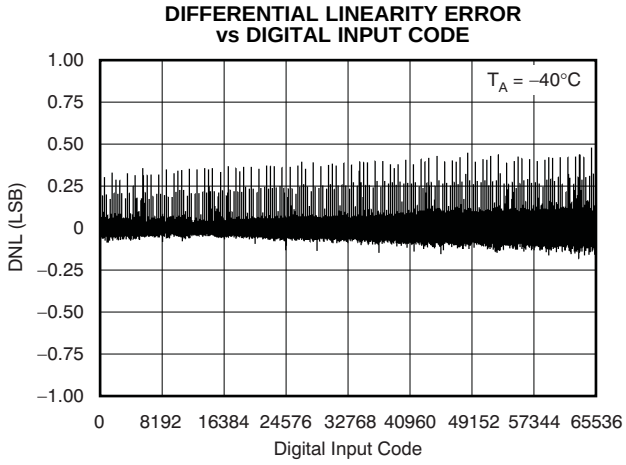



**Figure 12.**

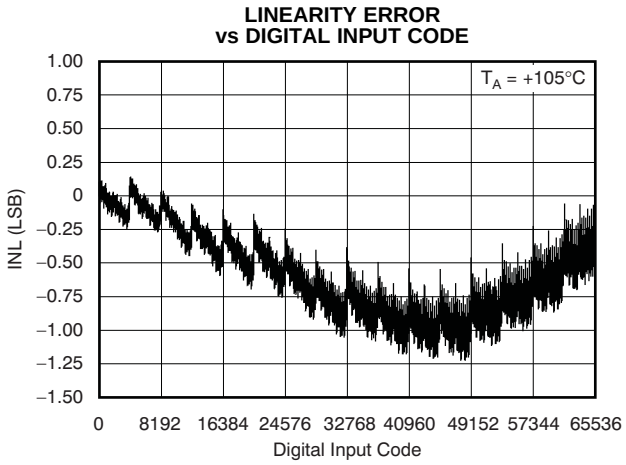



**Figure 13.**

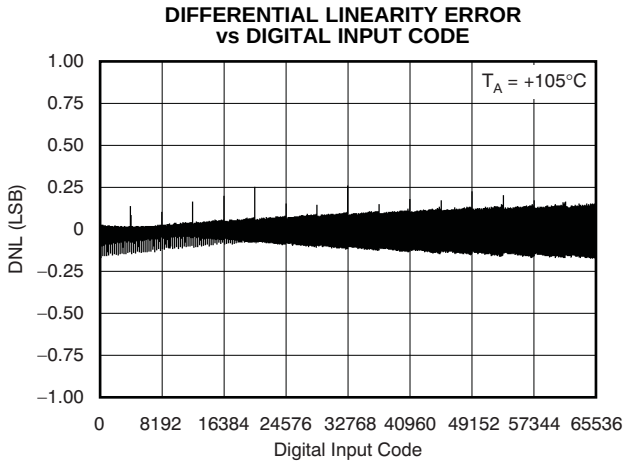



**Figure 14.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

**LINEARITY ERROR vs DIGITAL INPUT CODE**

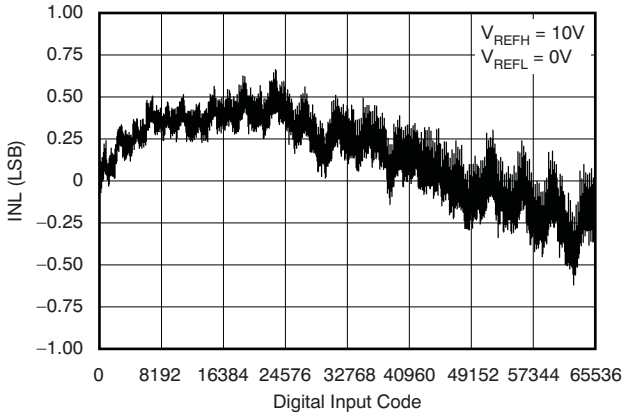



**Figure 15.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**

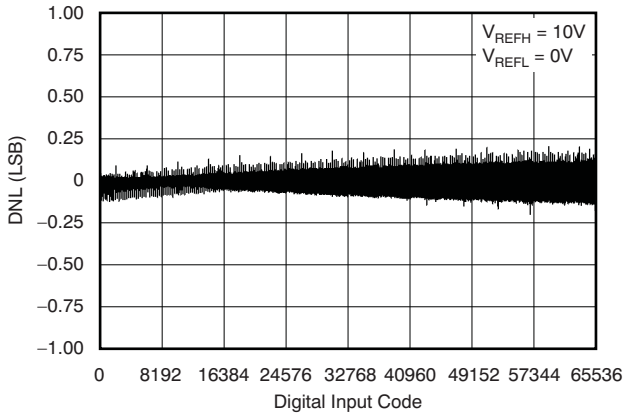



**Figure 16.**

**LINEARITY ERROR vs DIGITAL INPUT CODE**

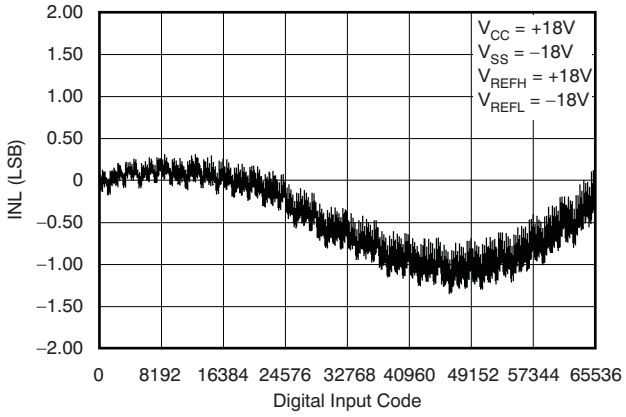



**Figure 17.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**

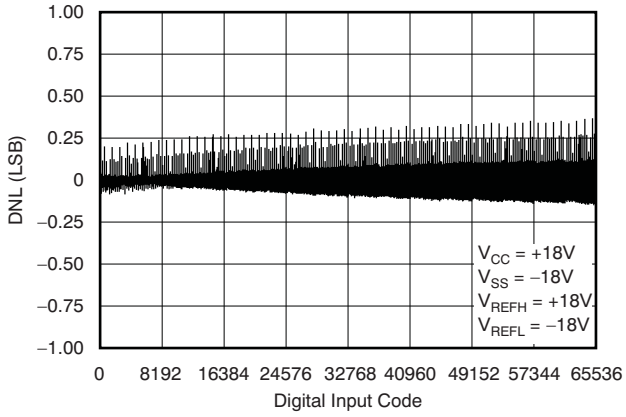



**Figure 18.**

**INTEGRAL NONLINEARITY ERROR vs REFERENCE VOLTAGE**

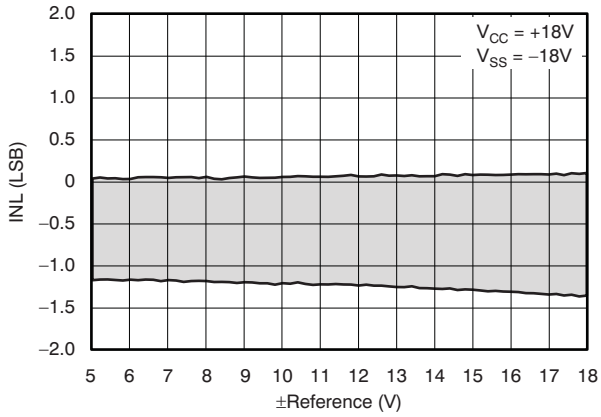



**Figure 19.**

**DIFFERENTIAL NONLINEARITY ERROR vs REFERENCE VOLTAGE**

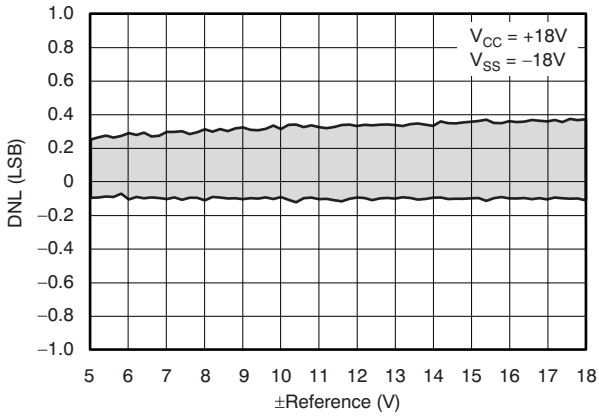



**Figure 20.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

**INTEGRAL NONLINEARITY ERROR vs ANALOG SUPPLY VOLTAGE**

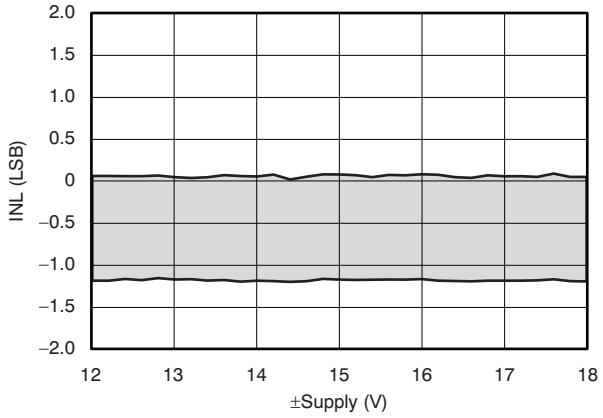



**Figure 21.**

**DIFFERENTIAL NONLINEARITY ERROR vs ANALOG SUPPLY VOLTAGE**

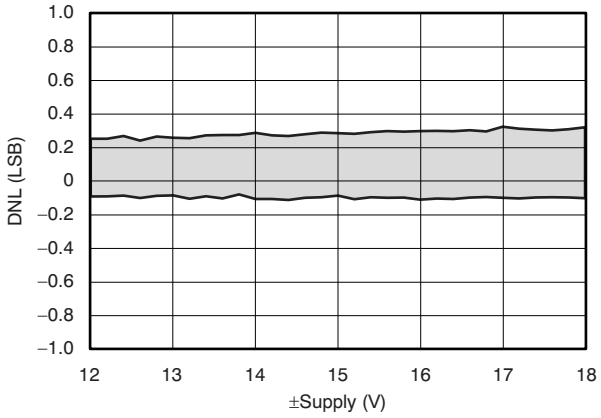



**Figure 22.**

**GAIN ERROR vs TEMPERATURE**

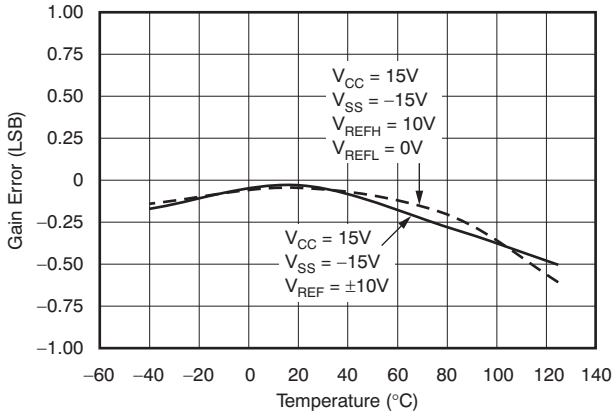



**Figure 23.**

**ZERO-CODE ERROR vs TEMPERATURE**

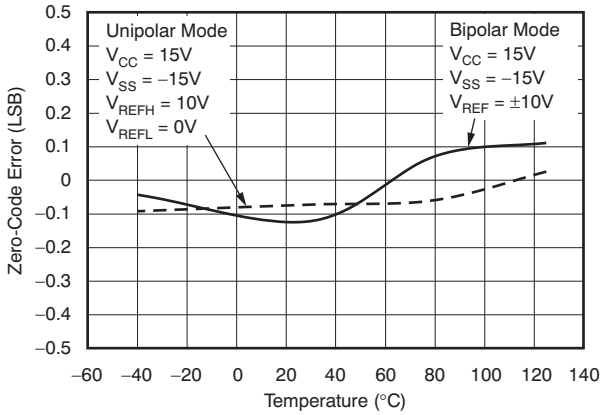



**Figure 24.**

**BIPOLAR ZERO ERROR vs TEMPERATURE**

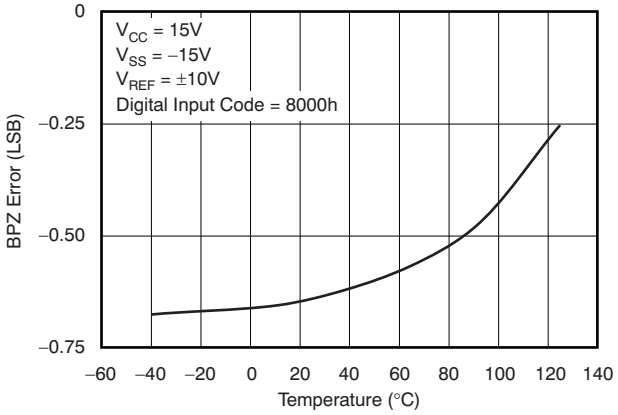



**Figure 25.**

**SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE**

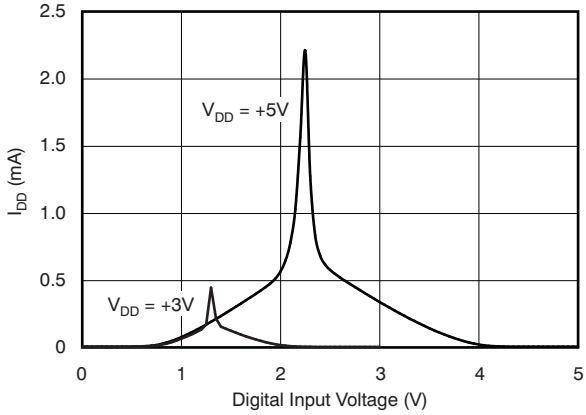



**Figure 26.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

**DUAL REFERENCE CURRENT vs CODE**

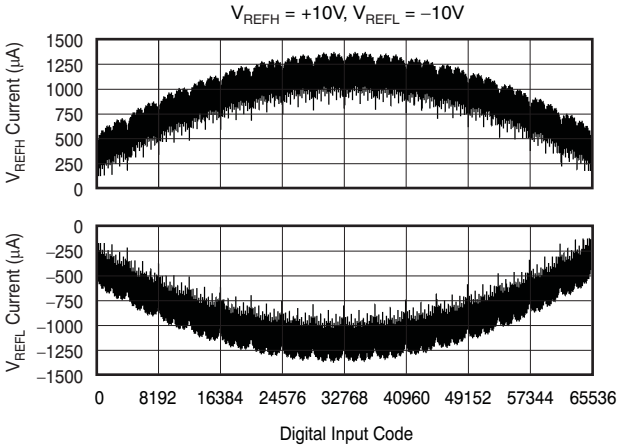



**Figure 27.**

**SINGLE REFERENCE CURRENT vs CODE**

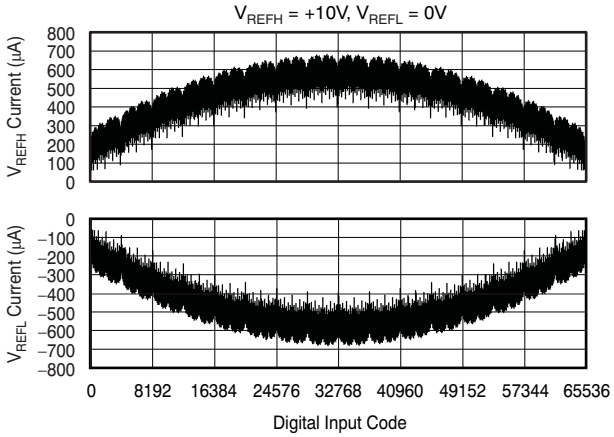



**Figure 28.**

**SUPPLY CURRENTS vs TEMPERATURE**

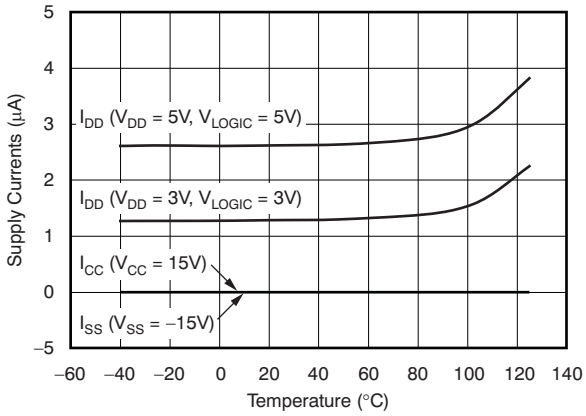



**Figure 29.**

**DIGITAL SUPPLY CURRENT vs DIGITAL SUPPLY VOLTAGE**

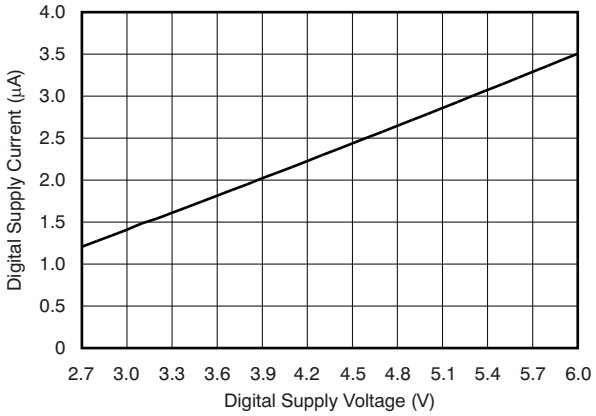



**Figure 30.**

**ANALOG SUPPLY CURRENT vs ANALOG SUPPLY VOLTAGE**

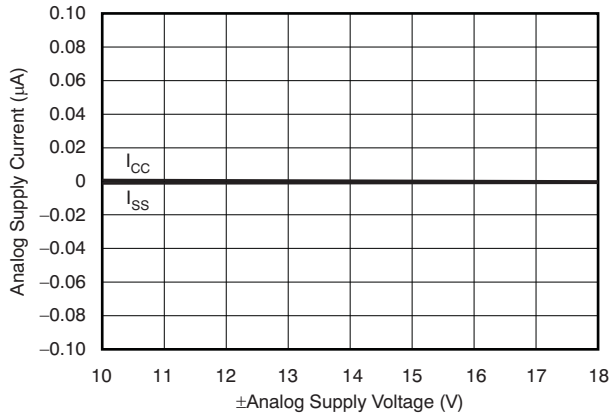



**Figure 31.**

**SUPPLY CURRENTS vs REFERENCE VOLTAGES**

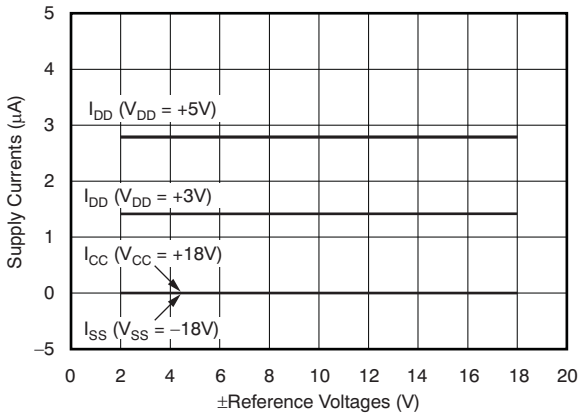



**Figure 32.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_{DD}$ = +5V, $V_{CC}$ = +15V, $V_{SS}$ = –15V, $V_{REFH}$ = +10V, and $V_{REFL}$ =–10V, unless otherwise noted.

**MAJOR CARRY GLITCH (FALLING)**

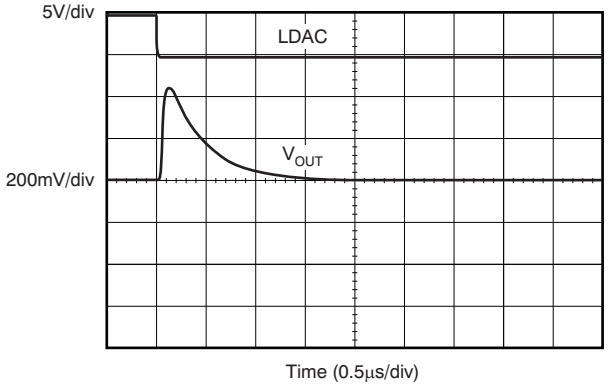



**Figure 33.**

**MAJOR CARRY GLITCH (RISING)**

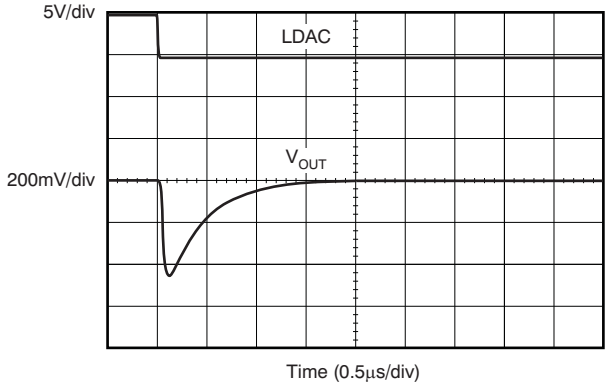



**Figure 34.**

**DAC SETTLING TIME (FALLING)**

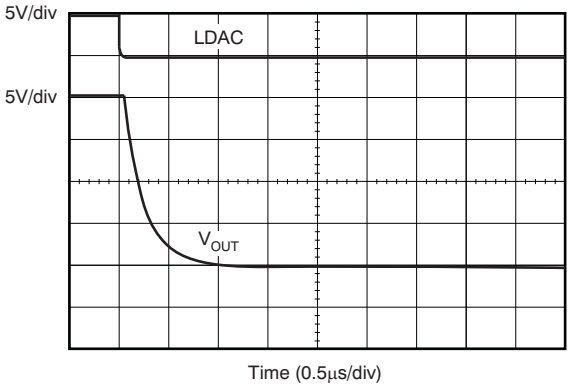



**Figure 35.**

**DAC SETTLING TIME (RISING)**

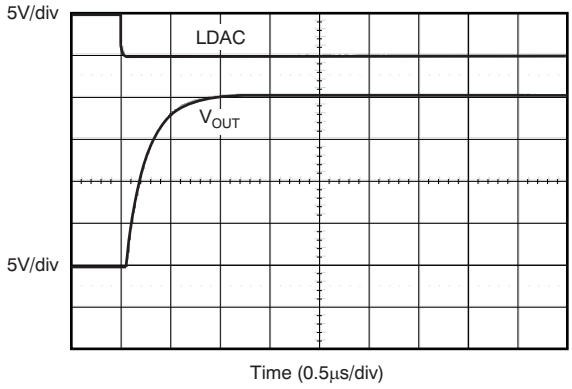



**Figure 36.**

**BROADBAND NOISE**

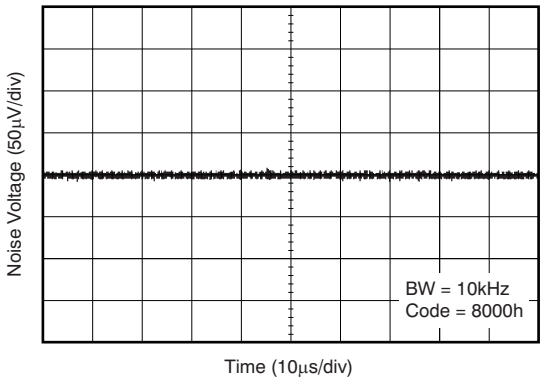



**Figure 37.**

# THEORY OF OPERATION

## GENERAL DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial-input, voltage-output DAC. It operates from a dual power supply ranging from ±13.5V to ±19.8V, and typically consumes 10µA. The output range is from $V_{REFL}$ to $V_{REFH}$. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8871 is designed with a power-on reset function. After power on, the state of the RSTSEL pin sets the value of the input register and DAC latch, which sets the output state of the $V_{OUT}$ pin. Refer to the Power-On Reset and Hardware Reset section for more details.

Kelvin sense connections for the reference and analog ground are also included.

## DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 38. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either $V_{REFH}$ or $V_{REFL}$. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

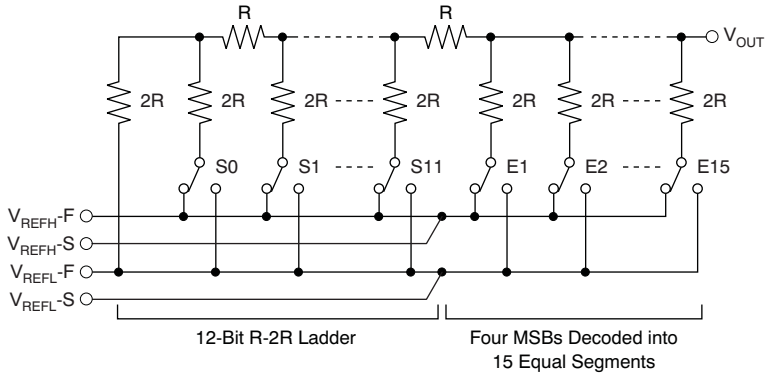



**Figure 38. DAC Architecture**

## OUTPUT RANGE

The output of the DAC is:

$$V_{OUT} = \frac{V_{REFH} - V_{REFL}}{65536} \times Code + V_{REFL} \quad (1)$$

Where *Code* is the decimal data word loaded to the DAC latch.

For example, if $V_{REFH}$ is +10V, and $V_{REFL}$ is –10V, the range of $V_{OUT}$ is from –10V (Code = 0000h) to +10V (Code = FFFFh).

The range of $V_{REFL}$ is from –18V to ($V_{REFH}$ – 1.25V), and the range of $V_{REFH}$ is 0V to +18V. The output from the DAC8871 can be unipolar (from 0V to +18V) or bipolar by setting the proper $V_{REFL}$ and $V_{REFH}$ values.

## POWER-ON RESET AND HARDWARE RESET

The DAC8871 has a power-on reset function. When the RSTSEL pin is low (tied to DGND), and after power-on or a hardware reset signal is applied to the $\overline{RST}$ pin, the DAC latch is cleared ('0') and the $V_{OUT}$ pin is set to negative full-scale. When RSTSEL is high, the DAC latch and $V_{OUT}$ are set to mid-scale.

## SERIAL INTERFACE

The DAC8871 digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™ and TI DSP™ interfaces, which can operate at speeds up to 50 Mbits/second. The data transfer is framed by the chip select ($\overline{CS}$) signal. The DAC works as a bus slave. The bus master generates the synchronize clock (SCLK) and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and SCLK and SDI are ignored. The bus master accesses the DAC by driving $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on the SDI pin are shifted out from the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the content of the input shift register to the input register.

All data registers are 16 bits. It takes 16 SCLK cycles to transfer one data word to the device. To complete a whole data word, $\overline{CS}$ must be taken high immediately after the 16th SCLK is clocked in. If more than 16 SCLK cycles are applied while $\overline{CS}$ is low, the last 16 bits are transferred into the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC latch with a new 16-bit word.

The DAC8871 has an $\overline{LDAC}$ pin that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be kept high while $\overline{CS}$ is low. If $\overline{LDAC}$ is permanently tied low, the DAC latch will be updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

## EXTERNAL AMPLIFIER SELECTION

The output of the DAC8871 is unbuffered. The output impedance is approximately 6.2kΩ. If the applications require an external buffer amplifier, the selected amplifier must have a low-offset voltage (1LSB = 305µV for ±10V output range), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25kΩ) adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. The output impedance of the DAC is constant and code-independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3dB bandwidth of 1MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3dB amplifier bandwidth results in a shorter effective settling time of the DAC and amplifier combination.

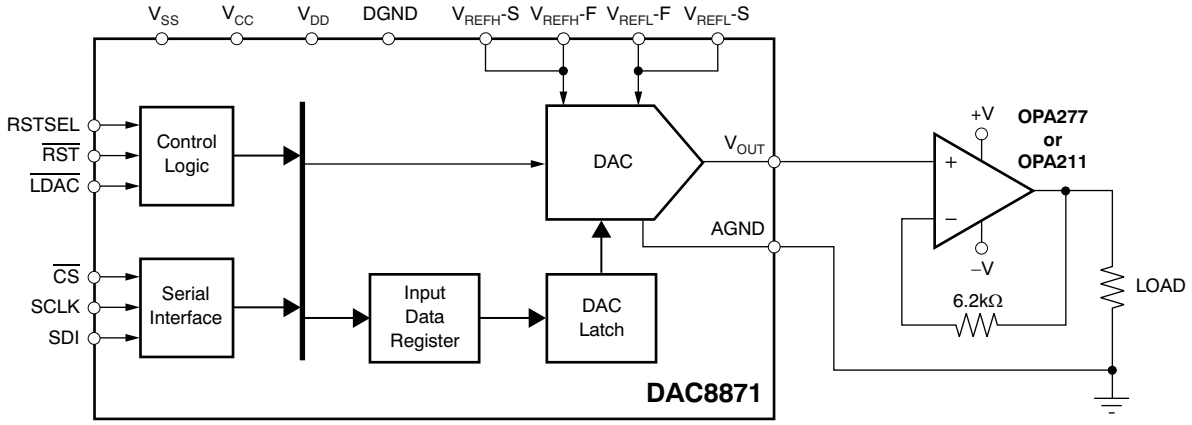



**Figure 39. DAC8871 with External Amplifier**

## APPLICATION INFORMATION

### REFERENCE INPUT

The DAC full-scale output voltage is determined by the reference voltage, as shown in the *Output Range* section.

Reference input $V_{REFH}$ can be any voltage from 0V to +18V. Reference input $V_{REFL}$ can be any voltage from –18V to ($V_{REFH}$ – 1.25V). The current into the $V_{REFH}$ input and out of $V_{REFL}$ depends on the DAC output voltages. Refer to Figure 27 and Figure 28 for details. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC8871 features a reference drive (force) and sense connection that minimizes the internal errors caused by the changing reference current and the circuit impedances. Figure 40 shows a typical reference configuration.

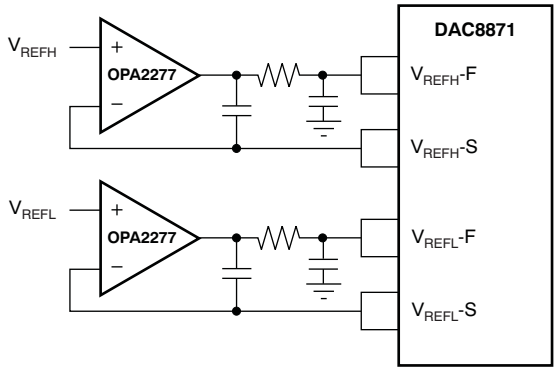



**Figure 40. Buffered Reference Connection**

### POWER-SUPPLY BYPASSING

For accurate, high-resolution performance, bypassing the supply pins with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is recommended.

### POWER-SUPPLY SEQUENCING

The analog supplies ($V_{CC}$ and $V_{SS}$) must power up before the digital supply ($V_{DD}$). All three supplies must power up before the reference voltages ($V_{REFH}$ and $V_{REFL}$) are applied. Additionally, because the DAC input shift register is not reset during a power-on reset (or a hardware reset through the $\overline{RST}$ pin), the $\overline{CS}$ pin must not be unintentionally asserted during power-up of the device. It is recommended that the $\overline{CS}$ pin be connected to $V_{DD}$ through a pull-up resistor to avoid improper power-up.

Likewise, the state of the $\overline{LDAC}$ pin must not be accidentally changed during power-up. It is recommended that the $\overline{LDAC}$ pin be connected to $V_{DD}$ through a pull-up resistor, unless it is permanently tied to ground.

To ensure that the ESD protection circuitry of this device is not activated, all other digital pins must be kept at ground potential until $V_{DD}$ is applied.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC8871SBPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |
| DAC8871SBPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |
| DAC8871SBPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |
| DAC8871SPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |
| DAC8871SPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |
| DAC8871SPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | DAC8871 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

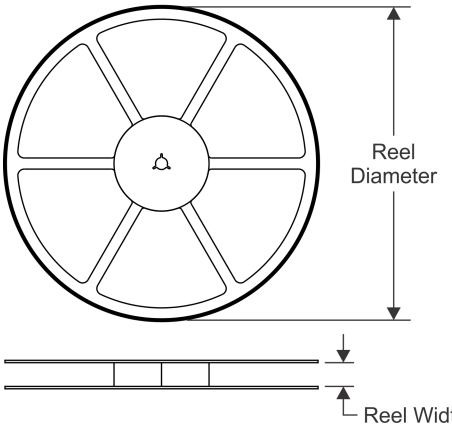
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

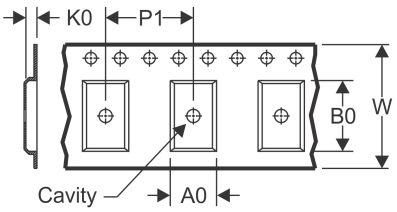
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

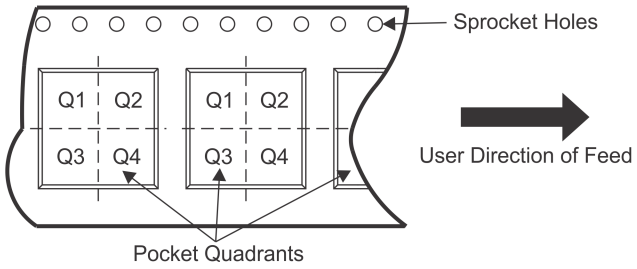



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

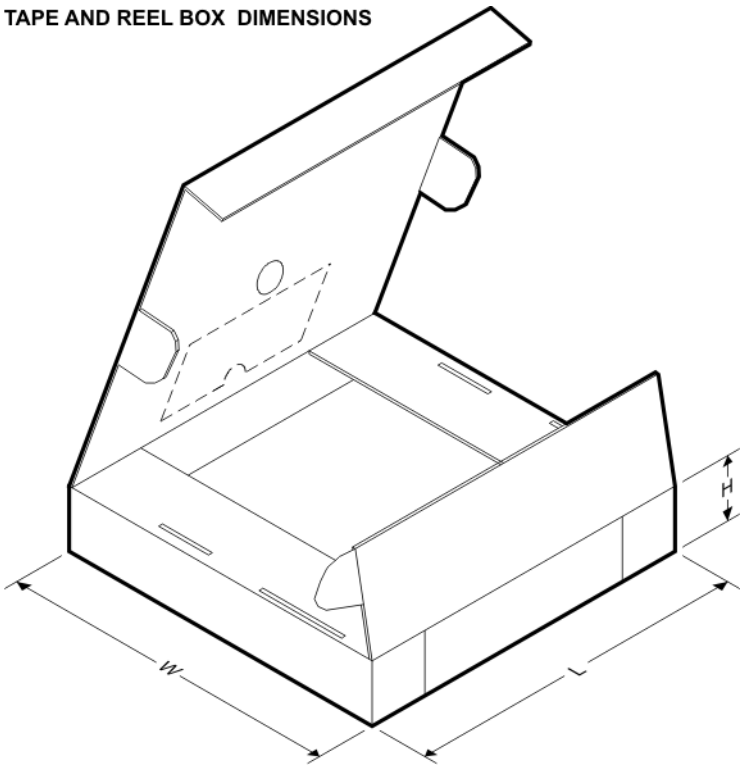
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC8871SBPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DAC8871SPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

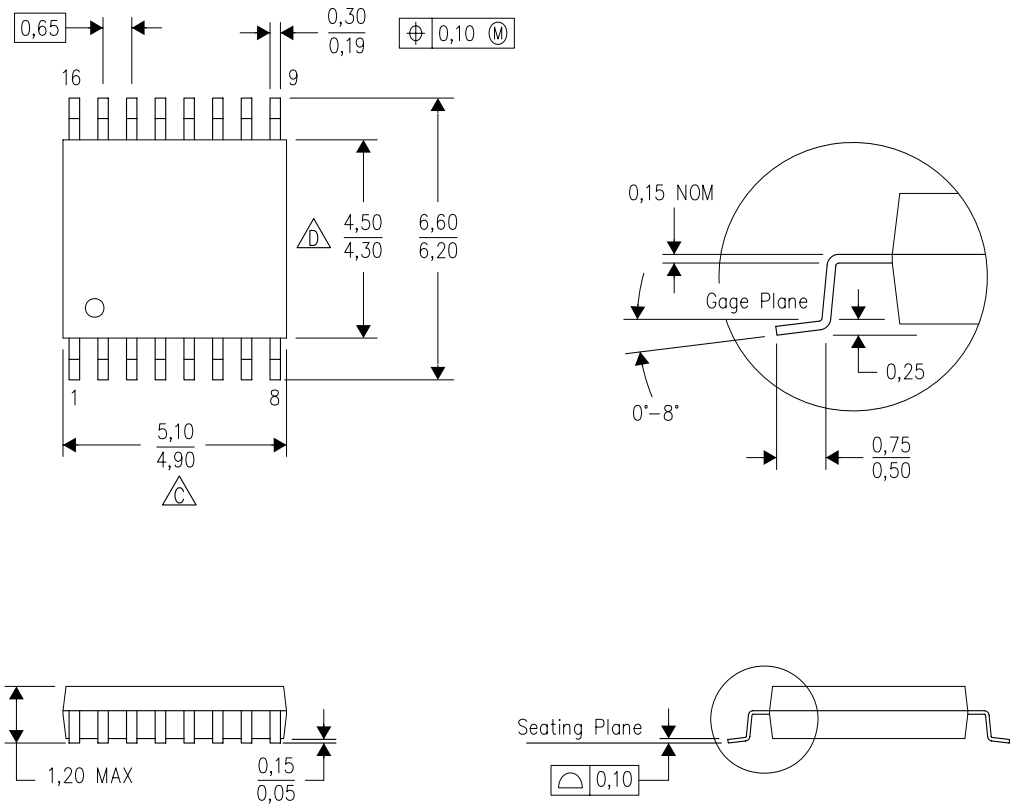
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DAC8871SBPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| DAC8871SPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

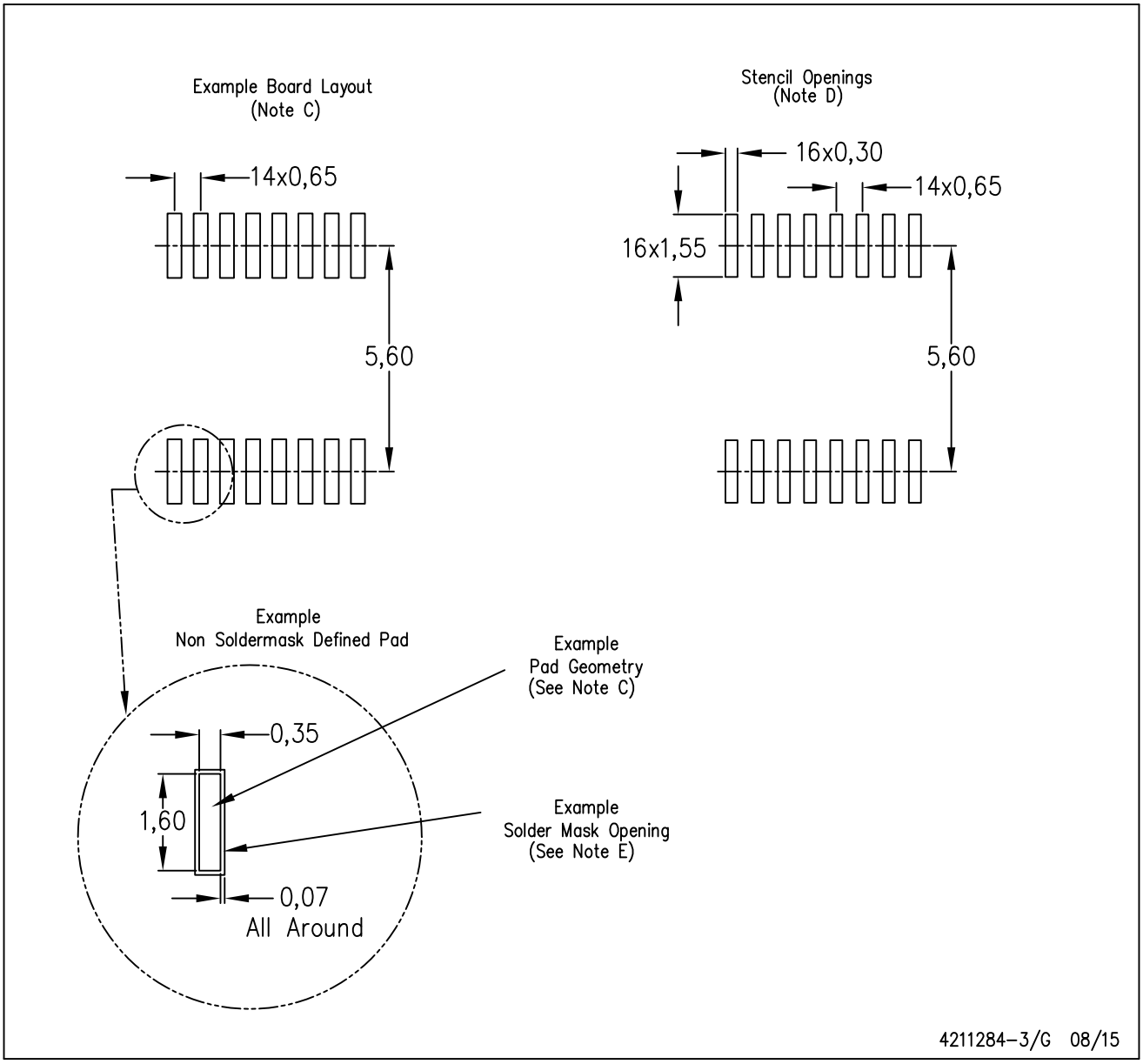
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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