Precision Monolithic Quad SPST Low-Voltage CMOS Analog Switches

DESCRIPTION

The DG411L, DG412L, DG413L are low voltage pin-for-pin compatible companion devices to the industry standard DG411, DG412, DG413 with improved performance.

Using BiCMOS wafer fabrication technology allows the DG411L, DG412L, DG413L to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

Combining high speed (t_{ON}: 19 ns), flat $R_{DS(on)}$ over the analog signal range (5 Ω), minimal insertion lose (- 3 dB at 280 MHz), and excellent crosstalk and off-isolation performance (- 50 dB at 50 MHz), the DG411L, DG412L, DG413L are ideally suited for audio and video signal switching.

The DG411L and DG412L respond to opposite control logic as shown in the Truth Table. The DG413L has two normally open and two normally closed switches.

FEATURES

- 2.7- thru 12 V single supply or ± 3- thru ± 6 dual supply
- On-resistance - $R_{DS(on)}$: 17 Ω
- Fast switching - t_{ON}: 19 ns
- t_{OFF}: 12 ns
- TTL, CMOS compatible
- Low leakage: 0.25 nA
- 2000 V ESD protection

Pb Available

RoHS* COMPLIANT

BENEFITS

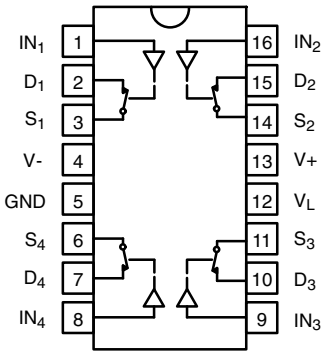
- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacinge

APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals
- SDSL, DSLAM
- Audio and video signal routing

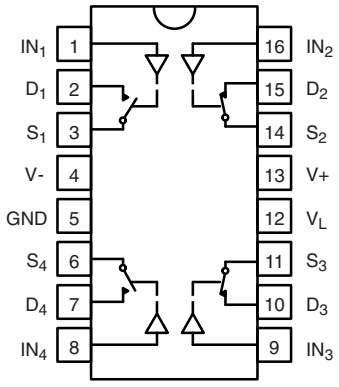
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG411L, DG412L
Dual-In-Line, TSSOP and SOIC



Top View

DG413L
Dual-In-Line, TSSOP and SOIC



Top View

TRUTH TABLE		
Logic	**DG411L**	**DG412L**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE		
Logic	**SW_1, SW_4**	**SW_2, SW_3**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION

Temp. Range	Package	Part Number
DG411L, DG412L		
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG411LDY DG411LDY-E3 DG411LDY-T1 DG411LDY-T1-E3
		DG412LDY DG412LDY-E3 DG412LDY-T1 DG412LDY-T1-E3
	16-Pin TSSOP	DG411LDQ DG411LDQ-E3 DG411LDQ-T1 DG411LDQ-T1-E3
		DG412LDQ DG412LDQ-E3 DG412LDQ-T1 DG412LDQ-T1-E3
DG413L		
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG413LDY DG413LDY-E3 DG413LDY-T1 DG413LDY-T1-E3
	16-Pin TSSOP	DG413LDQ DG413LDQ-E3 DG413LDQ-T1 DG413LDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to V-		- 0.3 to 13	V
GND to V-		7	
V_L		(GND - 0.3) to (V+) + 0.3	
I_N[a], V_S, V_D		- 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	
Continuous Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature	(DQ, DY Suffix)	- 65 to 125	°C
	(AK Suffix)	- 65 to 150	
Power Dissipation (Packages)[b]	16-Pin TSSOP[c]	450	mW
	16-Pin SOIC[d]	650	
	16-Pin CerDIP[e]	900	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 7 mW/°C above 75 °C
d. Derate 7.6 mW/°C above 75 °C
e. Derate 12 mW/°C above 75 °C.

SPECIFICATIONS[a] (Single Supply 12 V)									
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Typ.**[c]	**A Suffix Limits** - 55 °C to 125 °C **Min.**[d]	**A Suffix Limits** - 55 °C to 125 °C **Max.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Min.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 10.8 V, V- = 0 V I_S = 10 mA, V_D = 2/9 V	Room Full	20		30 45		30 40	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = 1/11 V, V_S = 11/1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{D(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 11/1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V	Full	0.01	- 1.5	1.5	- 1	1	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V	Full		- 1.5	1.5	- 1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 5 V, see figure 2	Room Full	20		50 70		50 60	ns
Turn-Off Time	t_{OFF}		Room Full	12		30 48		30 40	
Break-Before-Make Time Delay	t_D	DG413L only, V_S = 5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
Off-Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF , f = 1 MHz	Room	71					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	95					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	5					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	6					
Channel-On Capacitance[e]	$C_{D(on)}$		Room	15					
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full	0.02		1 7.5		1 5	µA
Negative Supply Current	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current	I_{GND}		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

SPECIFICATIONS[a] (Dual Supply ± 5 V)									
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, V- = - 5 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Ty.p**[c]	**A Suffix Limits** - 55 °C to 125 °C **Min.**[d]	**A Suffix Limits** - 55 °C to 125 °C **Max.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Min.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		- 5	5	- 5	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 5 V, V- = - 5 V I_S = 10 mA, V_D = ± 3.5 V	Room Full	20		33 45		33 40	Ω
Switch Off Leakage Current[g]	$I_{S(off)}$	V+ = 5.5 , V- = - 5.5 V V_D = ± 4.5 V, V_S = ± 4.5 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{D(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current[g]	$I_{D(on)}$	V+ = 5.5 V, V- = - 5.5 V V_S = V_D = ± 4.5 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current, V_{IN} Low[e]	I_{IL}	V_{IN} under test = 0.8 V	Full	0.05	- 1.5	1.5	- 1	1	µA
Input Current, V_{IN} High[e]	I_{IH}	V_{IN} under test = 2.4 V	Full	0.05	- 1.5	1.5	- 1	1	
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 3.5 V, see figure 2	Room Full	21		50 70		50 60	ns
Turn-Off Time[e]	t_{OFF}		Room Full	16		35 50		35 40	
Break-Before-Make Time Delay[e]	t_D	DG413L only, V_S = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF , f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	9					
Channel On Capacitance[e]	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current[e]	I+	V_{IN} = 0 or 5 V	Room Full	0.03		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current[e]	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

SPECIFICATIONS[a] (Single Supply 5 V)									
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Typ.**[c]	**A Suffix Limits** - 55 °C to 125 °C **Min.**[d]	**Max.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Min.**[d]	**Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			5		5	V
Drain-Source On-Resistance[e]	$R_{DS(on)}$	V+ = 4.5 V I_S = 5 mA, V_D = 1 V, 3.5 V	Room Full	35		50 88		50 75	Ω
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 3.5 V, see figure 2	Room Hot	27		50 90		50 60	ns
Turn-Off Time[e]	t_{OFF}		Room Hot	15		30 55		30 40	
Break-Before-Make Time Delay[e]	t_D	DG413L only, V_S = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	0.5					pC
Power Supplies									
Positive Supply Current[e]	I+	V_{IN} = 0 or 5 V	Room Hot	0.02		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Hot	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current[e]	I_L		Room Hot	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Hot	- 0.002	- 1 - 7.5		- 1 - 5		

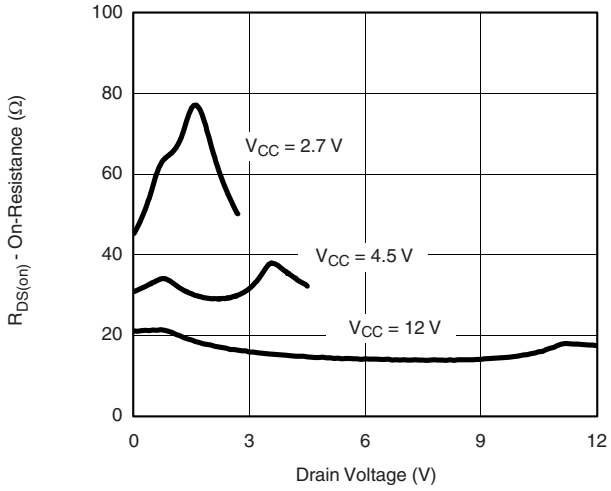
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

SPECIFICATIONS[a] (Single Supply 3 V)									
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 3 V, V- = 0 V V_L = 3 V, V_{IN} = 0.4 V[f]	**Temp.**[b]	**Typ.**[c]	**A Suffix Limits** - 55 °C to 125 °C **Min.**[d]	**Max.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Min.**[d]	**Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 2.7 V, V- = 0 V I_S = 5 mA, V_D = 0.5, 2.2 V	Room Full	65		80 115		80 100	Ω
Switch Off Leakage Current[g]	$I_{S(off)}$	V+ = 3.3 , V- = 0 V V_D = 1, 2 V, V_S = 2, 1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{D(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current[g]	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V V_S = V_D = 1, 2 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} under test = 0.4 V	Full	0.005	- 1.5	1.5	- 1	1	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V	Full	0.005	- 1.5	1.5	- 1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 1.5 V, see figure 2	Room Full	50		85 150		85 110	ns
Turn-Off Time	t_{OFF}		Room Full	30		60 100		60 85	
Break-Before-Make Time Delay	t_D	DG413L only, V_S = 1.5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	1					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF , f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	6					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	6					
Channel On Capacitance[e]	$C_{D(on)}$		Room	20					

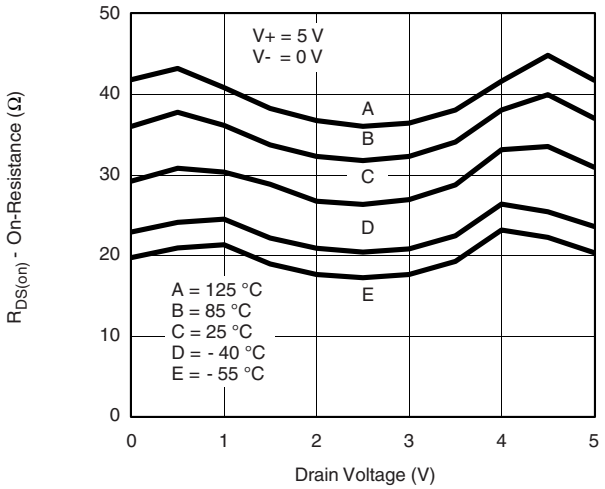
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

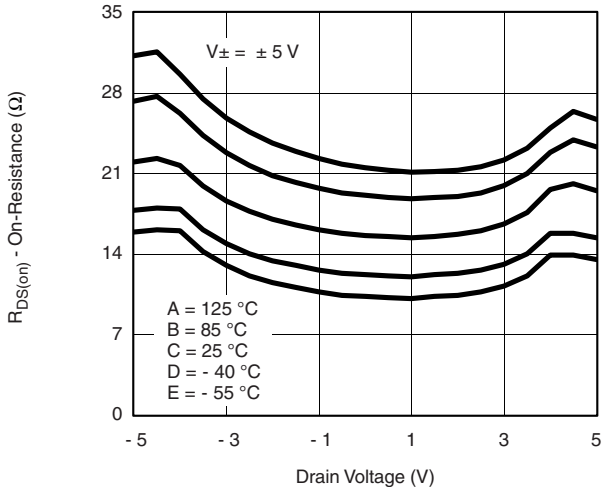
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



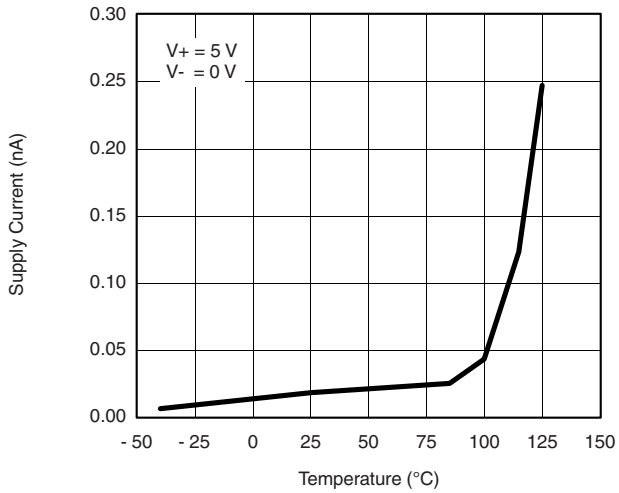
$R_{DS(on)}$ vs. Drain Voltage (Single Supply)



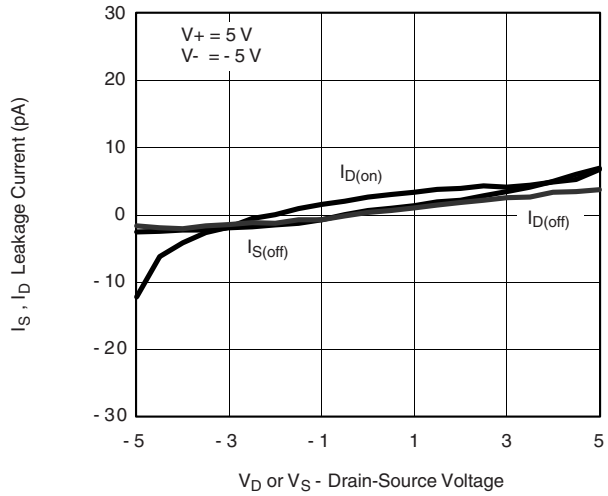
$R_{DS(on)}$ vs. Drain Voltage and Temperature (Single Supply)



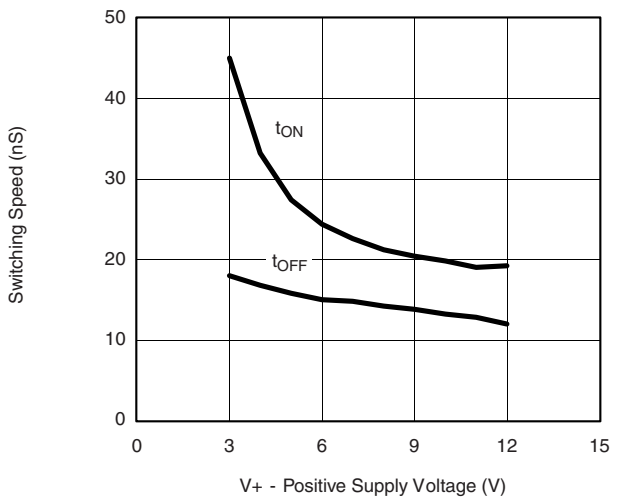
$R_{DS(on)}$ vs. Drain Voltage and Temperature (Dual Supply)



Supply Current vs. Temperature

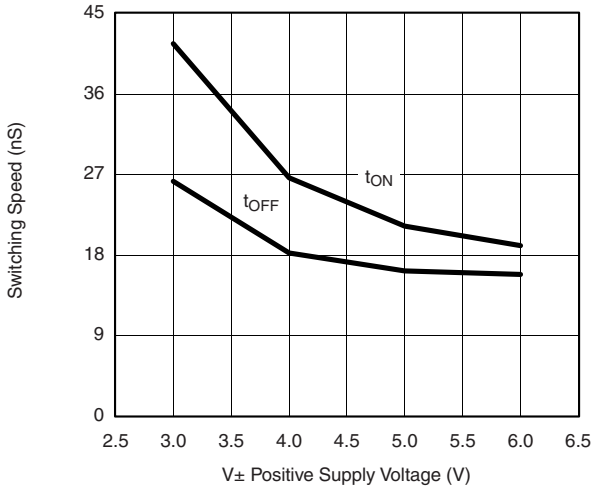


Leakage Current vs. Analog Voltage (Dual Supply)

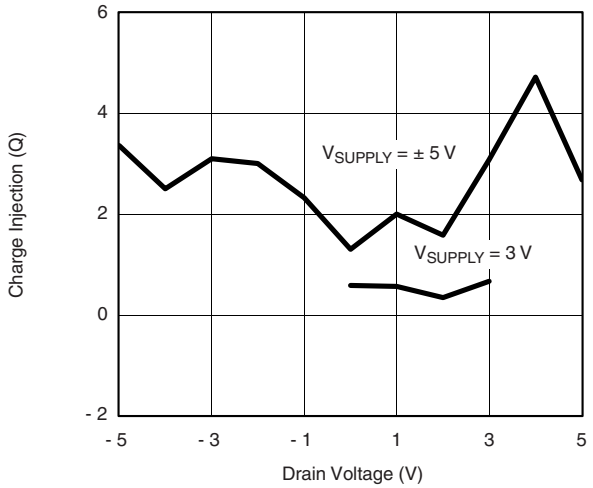


Switching Time vs. Single Supply

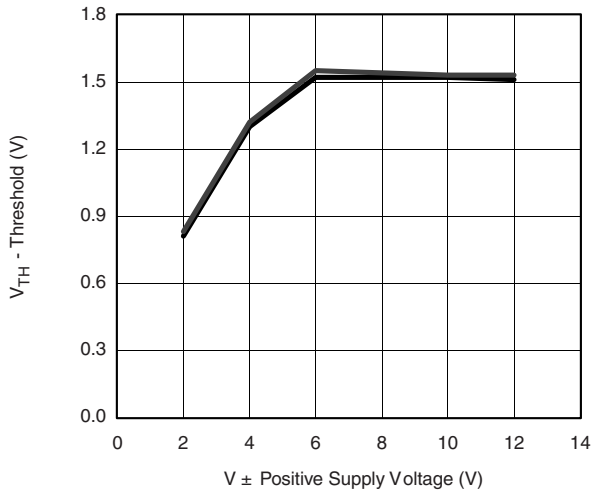
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



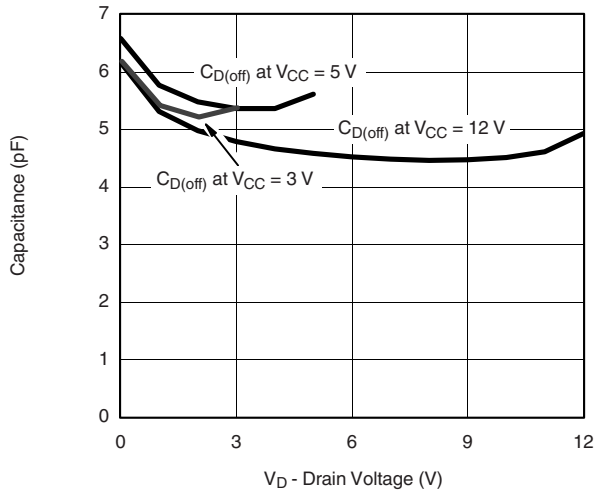
Switching Time vs. Dual Supply



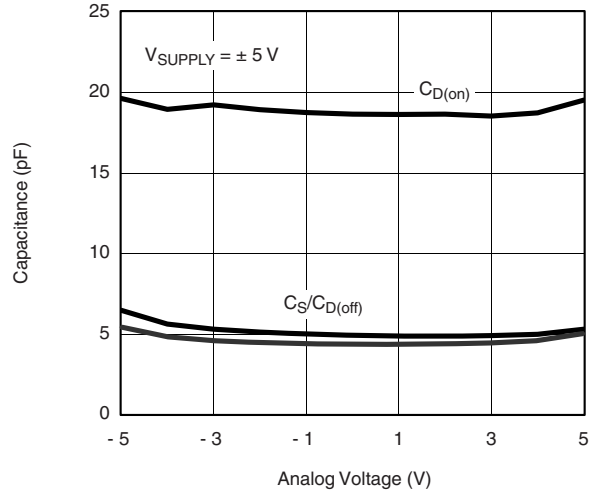
Charge Injection vs. Drain Voltage



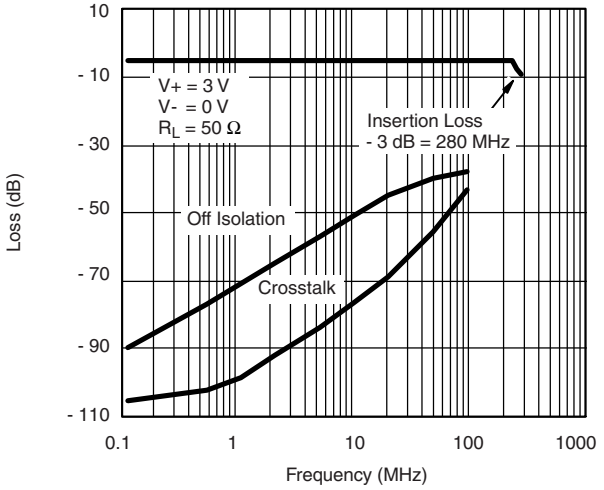
Input Threshold vs. Single Supply Voltage



Drain Capacitance vs. Drain Voltage (Single Supply)



Capacitance vs. Analog Signal (Dual Supply)



Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)

SCHEMATIC DIAGRAM (Typical Channel)

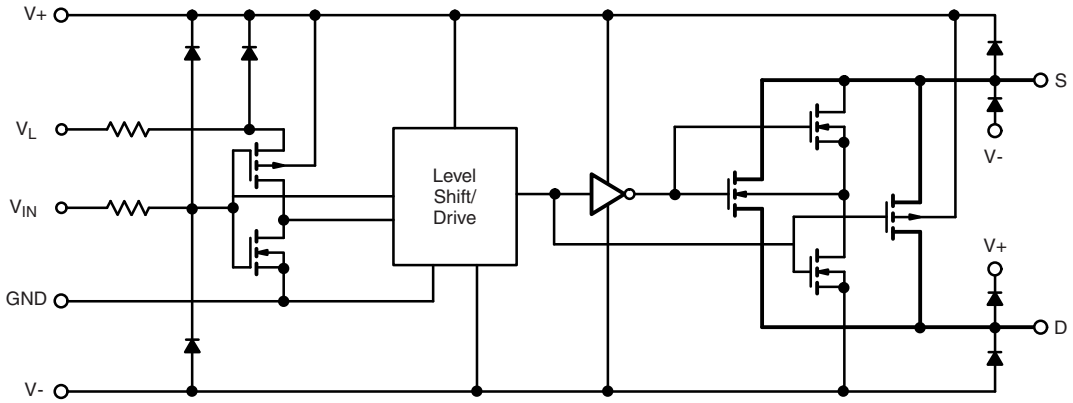
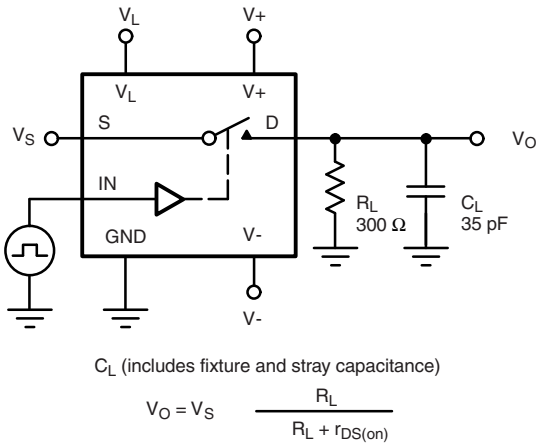
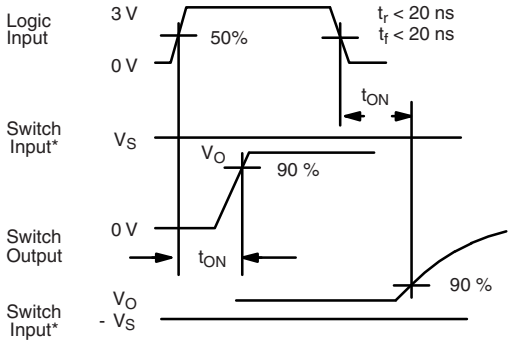


Figure 1.

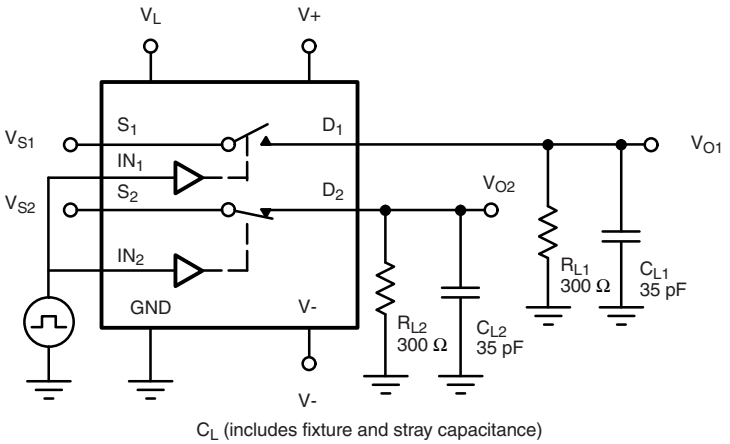
TEST CIRCUITS





Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



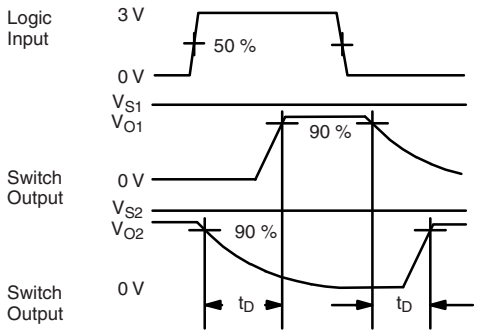
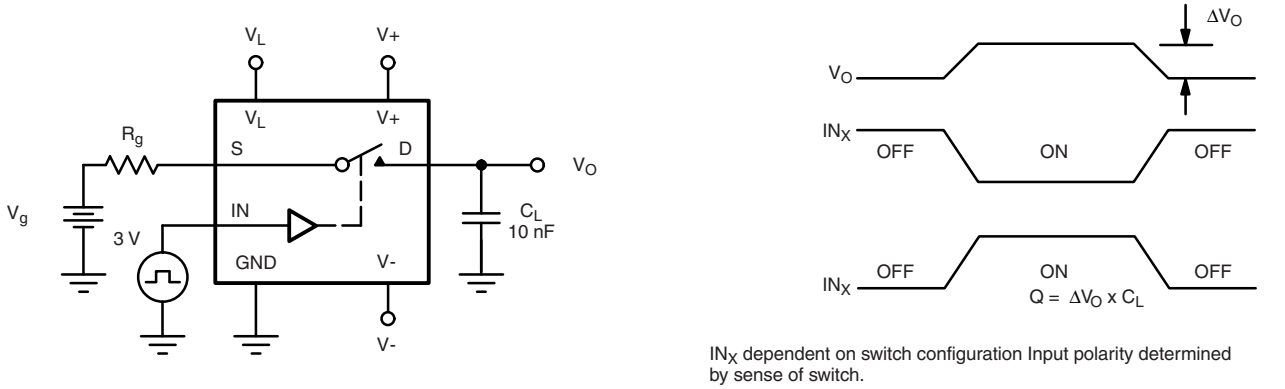


Figure 3. Break-Before-Make (DG413L)

TEST CIRCUITS



IN_X dependent on switch configuration Input polarity determined by sense of switch.

Figure 4. Charge Injection

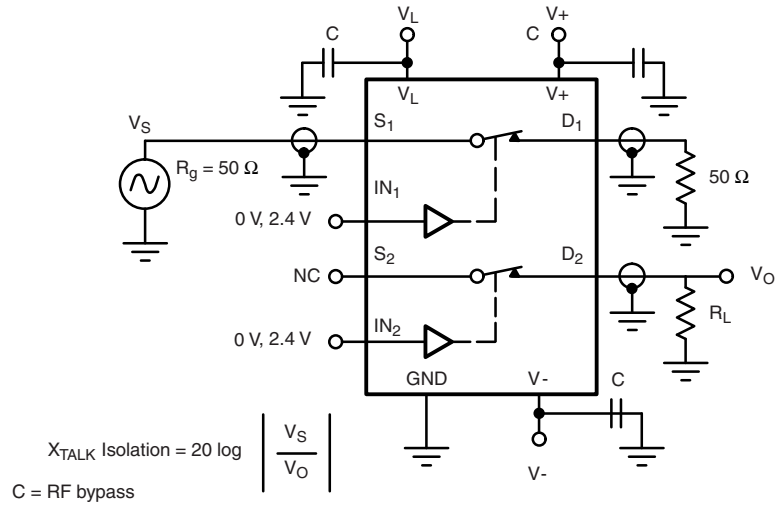


Figure 5. Crosstalk

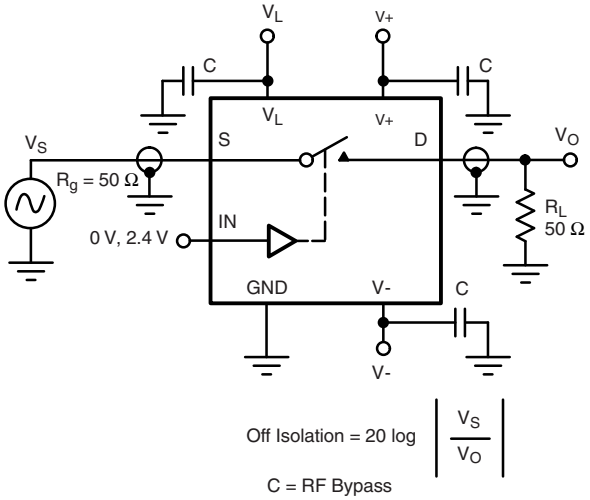


Figure 6. Off-Isolation

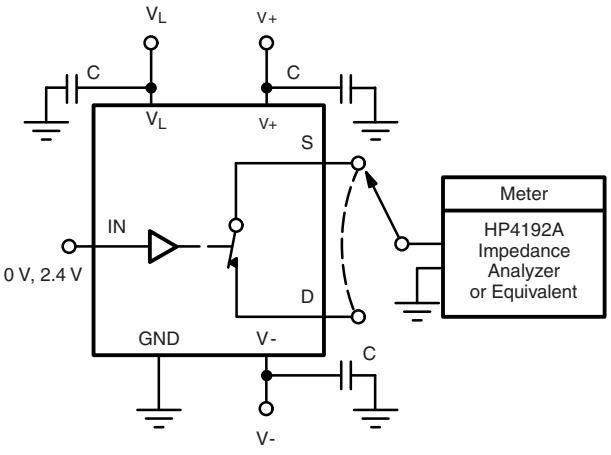


Figure 7. Source/Drain Capacitances

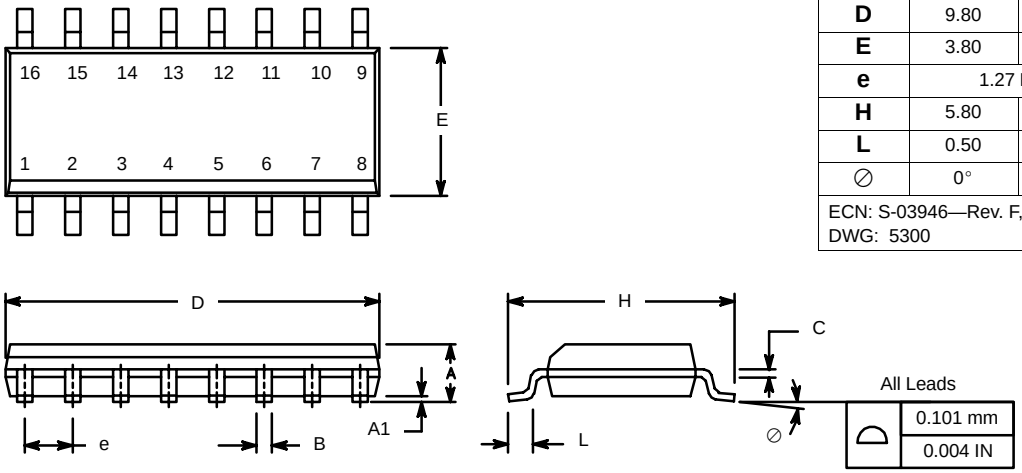
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71397.

SOIC (NARROW): 16-LEAD

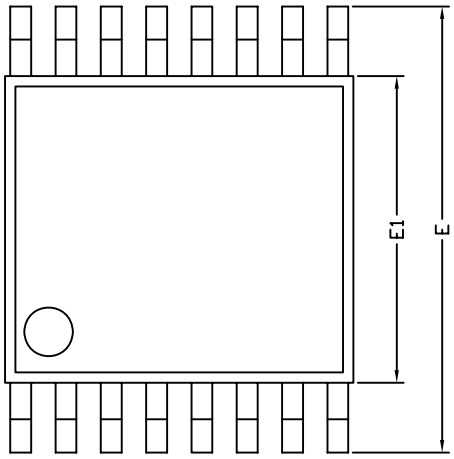
JEDEC Part Number: MS-012

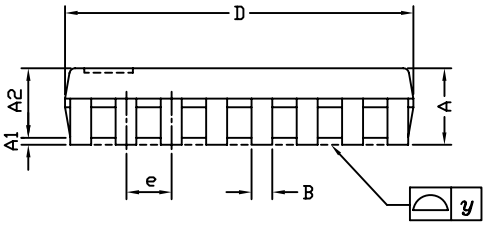
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

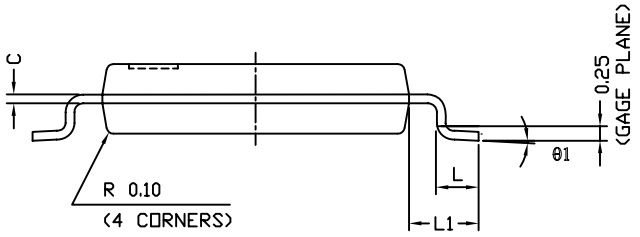
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



TSSOP: 16-LEAD

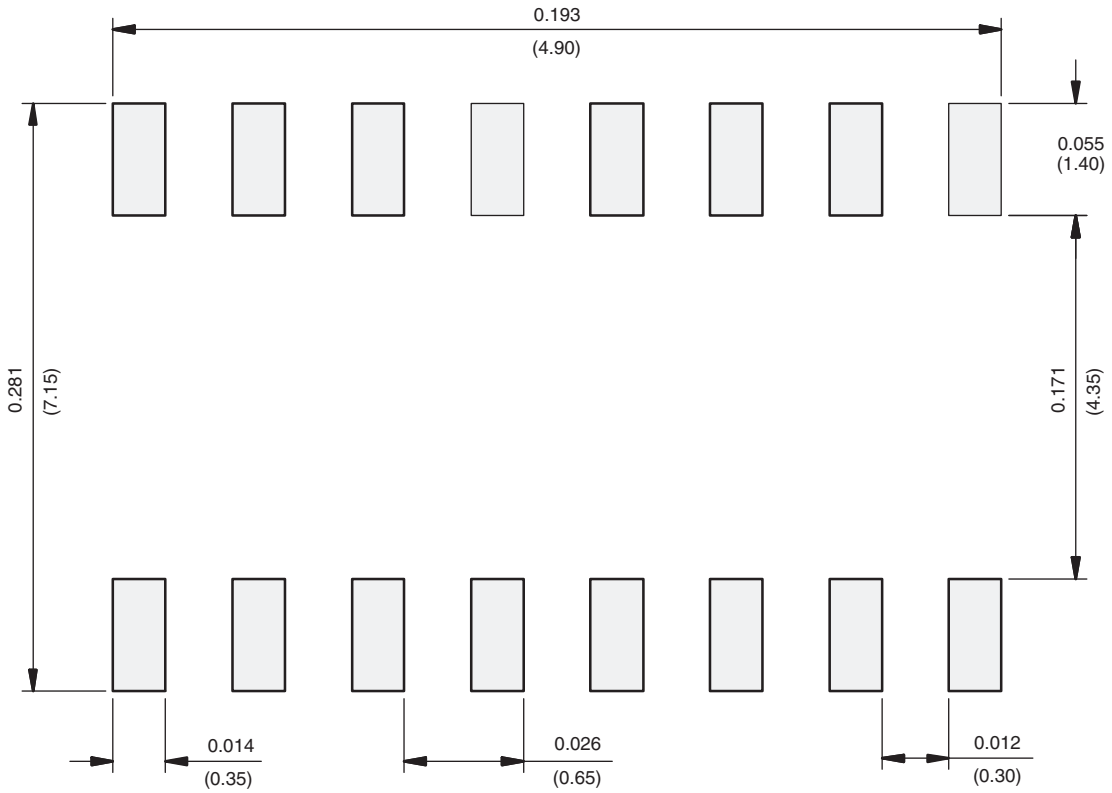






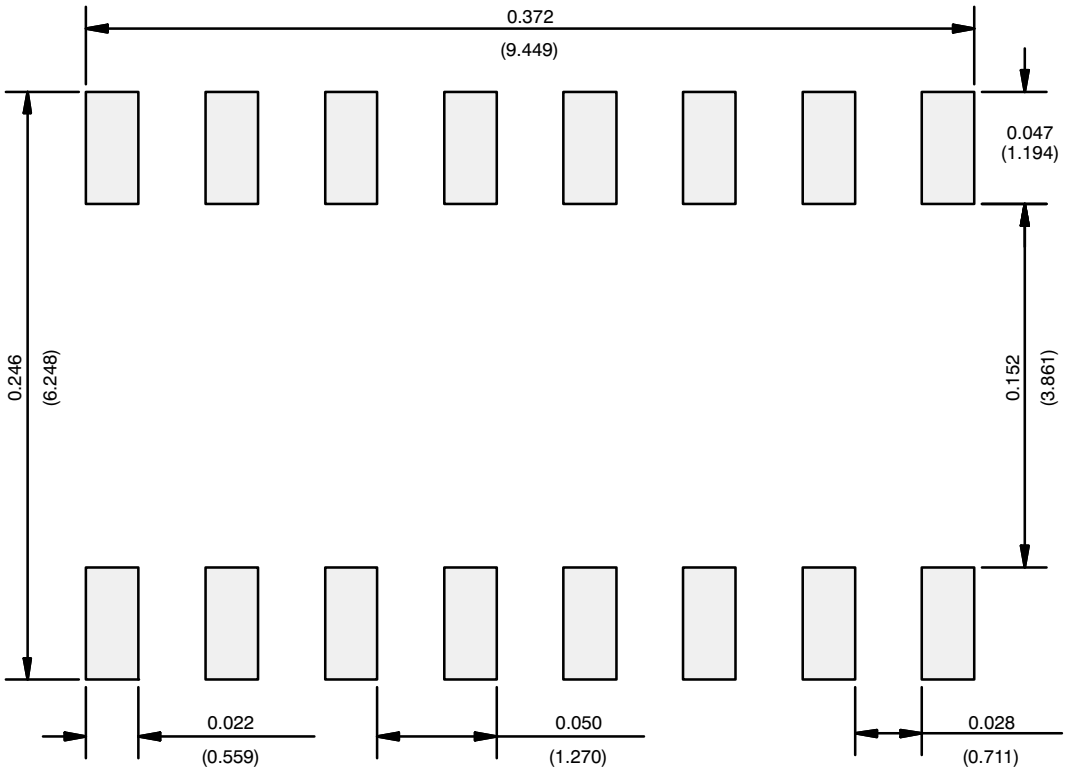
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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