

## Low-Voltage Dual SPST Analog Switch

### DESCRIPTION

The DG9262, DG9263 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed ( $t_{ON}$ : 35 ns,  $t_{OFF}$ : 20 ns), low on-resistance ( $R_{DS(on)}$ : 40  $\Omega$ ) and small physical size, the DG9262, DG9263 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9262, DG9263 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before make is guaranteed for DG9262, DG9263.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

### BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

### FEATURES

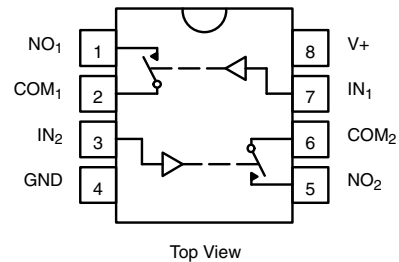
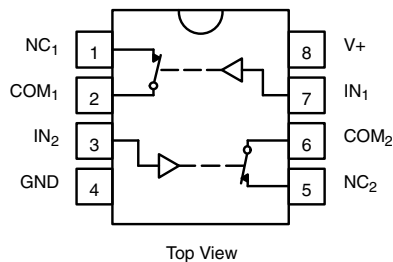
- **Halogen-free According to IEC 61249-2-21 Definition**
- Low Voltage Operation (- 2.7 V to 5 V)
- Low On-Resistance -  $R_{DS(on)}$ : 40  $\Omega$
- Fast Switching -  $t_{ON}$ : 35 ns,  $t_{OFF}$ : 20 ns
- Low Leakage -  $I_{COM(on)}$ : 200-pA max.
- Low Charge Injection -  $Q_{INJ}$ : 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in MSOP-8 and SOIC-8
- **Compliant to RoHS Directive 2002/95/EC**



### APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE - DG9262 |        |
|----------------------|--------|
| Logic                | Switch |
| 0                    | On     |
| 1                    | Off    |

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

| TRUTH TABLE - DG9263 |        |
|----------------------|--------|
| Logic                | Switch |
| 0                    | Off    |
| 1                    | On     |

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

| ORDERING INFORMATION |         |                |
|----------------------|---------|----------------|
| Temp Range           | Package | Part Number    |
| - 40 °C to 85 °C     | SOIC-8  | DG9262DY-E3    |
|                      |         | DG9262DY-T1    |
|                      |         | DG9262DY-T1-E3 |
|                      | MSOP-8  | DG9263DY-E3    |
|                      |         | DG9263DY-T1    |
|                      |         | DG9263DY-T1-E3 |
|                      |         | DG9262DQ-T1-E3 |
|                      |         | DG9263DQ-T1-E3 |

\* Pb containing terminations are not RoHS compliant, exemptions may apply

| ABSOLUTE MAXIMUM RATINGS                       |                                     |                     |      |
|--|-------------------------------------|---------------------|------|
| Parameter                                      |                                     | Limit               | Unit |
| Reference V+ to GND                            |                                     | - 0.3 to + 13       | V    |
| IN, COM, NC, NO <sup>a</sup>                   |                                     | - 0.3 to (V+ + 0.3) |      |
| Continuous Current (Any Terminal)              |                                     | ± 20                | mA   |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) |                                     | ± 40                |      |
| ESD (Method 3015.7)                            |                                     | > 2000              | V    |
| Storage Temperature (D Suffix)                 |                                     | - 65 to 125         | °C   |
| Power Dissipation (Packages) <sup>b</sup>      | 8-Pin Narrow Body SOIC <sup>c</sup> | 400                 | mW   |

Notes:

- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 75 °C.

| SPECIFICATIONS (V+ = 3 V)                 |                                      |  |                    |                              |                   |                   |      |
|---|--------------------------------------|--|--------------------|------------------------------|-------------------|-------------------|------|
| Parameter                                 | Symbol                               | Test Conditions<br>Unless Otherwise Specified<br>V+ = 3 V, ± 10 %, V <sub>IN</sub> = 0.8 V or 2.4 V <sup>e</sup> | Temp. <sup>a</sup> | D Suffix<br>- 40 °C to 85 °C |                   |                   | Unit |
|   |                                      |  |                    | Min. <sup>b</sup>            | Typ. <sup>c</sup> | Max. <sup>b</sup> |      |
| <b>Analog Switch</b>                      |                                      |  |                    |                              |                   |                   |      |
| Analog Signal Range <sup>d</sup>          | V <sub>ANALOG</sub>                  |  | Full               | 0                            |                   | 3                 | V    |
| Drain-Source On-Resistance                | R <sub>DS(on)</sub>                  | V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, V+ = 2.7 V<br>I <sub>COM</sub> = 5 mA                                | Room<br>Full       |                              | 50                | 80<br>140         | Ω    |
| R <sub>DS(on)</sub> Match <sup>d</sup>    | ΔR <sub>DS(on)</sub>                 | V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V   | Room               |                              | 0.4               | 2                 |      |
| R <sub>DS(on)</sub> Flatness <sup>d</sup> | R <sub>DS(on)</sub> Flatness         | V <sub>NO</sub> or V <sub>NC</sub> = 1 and 2 V   | Room               |                              | 4                 | 8                 |      |
| NO or NC Off Leakage Current <sup>g</sup> | I <sub>NO/NC(off)</sub>              | V <sub>NO</sub> or V <sub>NC</sub> = 1 V/2 V, V <sub>COM</sub> = 2 V/1 V   | Room<br>Full       | - 100<br>- 5000              | 5                 | 100<br>5000       | pA   |
| COM Off Leakage Current <sup>g</sup>      | I <sub>COM(off)</sub>                | V <sub>COM</sub> = 1 V/2 V, V <sub>NO</sub> or V <sub>NC</sub> = 2 V/1 V   | Room<br>Full       | - 100<br>- 5000              | 5                 | 100<br>5000       |      |
| Channel-On Leakage Current <sup>g</sup>   | I <sub>COM(on)</sub>                 | V <sub>COM</sub> = V <sub>NO</sub> or V <sub>NC</sub> = 1 V/2 V  | Room<br>Full       | - 200<br>- 10 000            | 10                | 200<br>10 000     |      |
| <b>Digital Control</b>                    |                                      |  |                    |                              |                   |                   |      |
| Input Current                             | I <sub>INL</sub> or I <sub>INH</sub> |  | Full               |                              | 1                 |                   | μA   |
| <b>Dynamic Characteristics</b>            |                                      |  |                    |                              |                   |                   |      |
| Turn-On Time                              | t <sub>ON</sub>                      | V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V   | Room<br>Full       |                              | 50                | 120<br>200        | ns   |
| Turn-Off Time                             | t <sub>OFF</sub>                     |  | Room<br>Full       |                              | 20                | 50<br>120         |      |
| Charge Injection <sup>d</sup>             | Q <sub>INJ</sub>                     | C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω  | Room               |                              | 1                 | 5                 | pC   |
| Off-Isolation                             | OIRR                                 | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz  | Room               |                              | - 74              |                   | dB   |
| Crosstalk                                 | X <sub>TALK</sub>                    |  | Room               |                              | - 90              |                   |      |
| NC and NO Capacitance                     | C <sub>(off)</sub>                   | f = 1 MHz  | Room               |                              | 7                 |                   | pF   |
| Channel-On Capacitance                    | C <sub>COM(on)</sub>                 |  | Room               |                              | 20                |                   |      |
| COM-Off Capacitance                       | C <sub>COM(off)</sub>                |  | Room               |                              | 13                |                   |      |
| <b>Power Supply</b>                       |                                      |  |                    |                              |                   |                   |      |
| Power Supply Range                        | V+                                   |  |                    | 2.7                          |                   | 12                | V    |
| Power Supply Current                      | I+                                   | V+ = 3.3 V, V <sub>IN</sub> = 0 V or 3.3 V   |                    |                              |                   | 1                 | μA   |

Notes:

- a. Room = 25 °C, full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V<sub>IN</sub> = input voltage to perform proper function.
- f. Difference of min and max values.
- g. Guraranteed by 5 V leakage testing, not production tested.



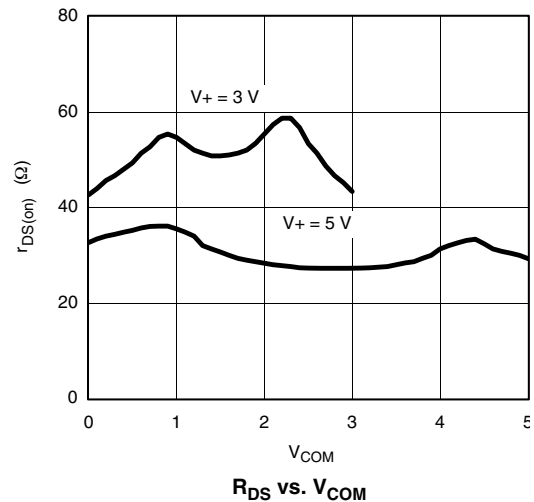
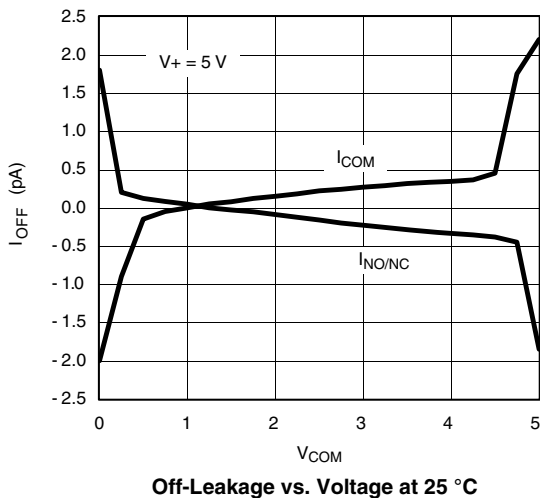
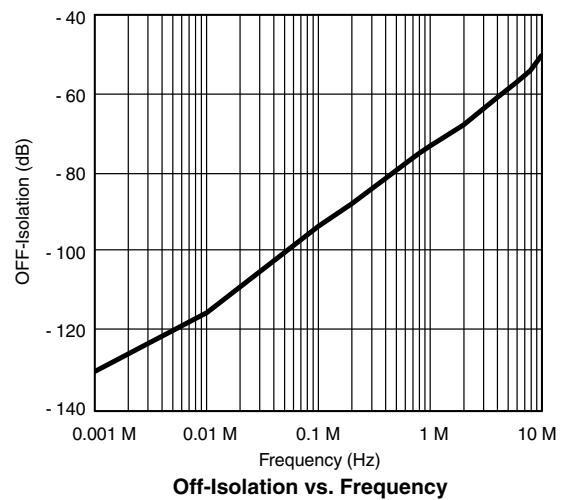
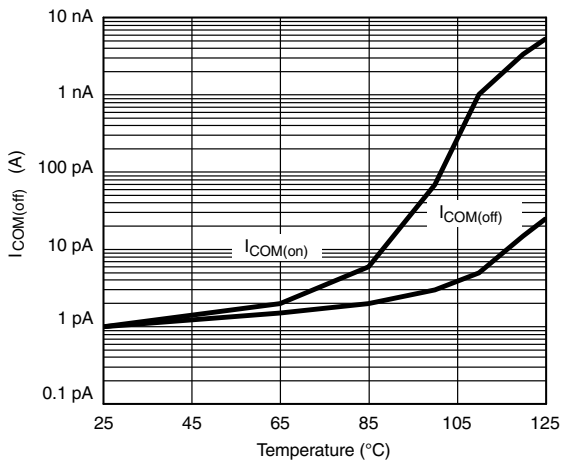
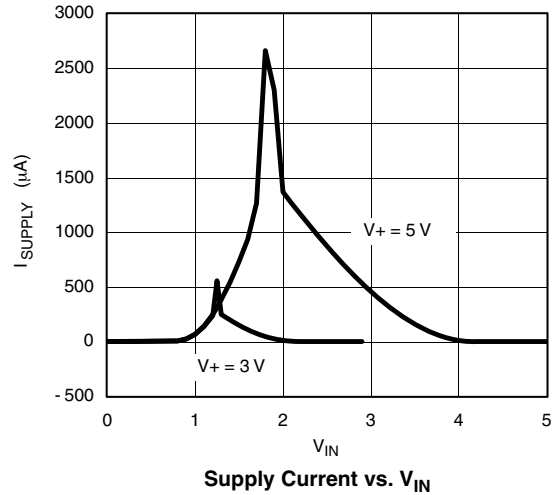
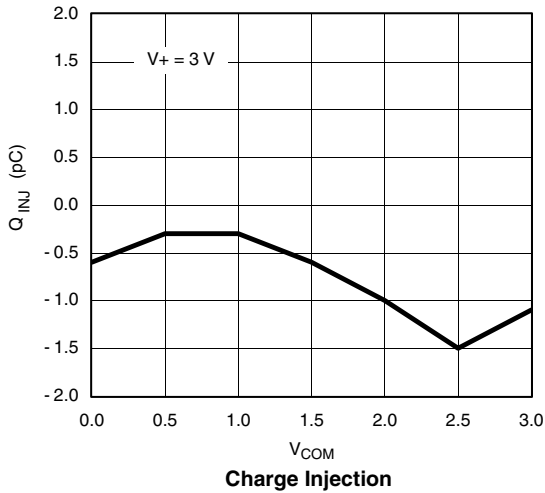
| SPECIFICATIONS (V <sub>+</sub> = 5 V)     |                                      |  |                    |                              |                   |                   |      |
|---|--------------------------------------|--|--------------------|------------------------------|-------------------|-------------------|------|
| Parameter                                 | Symbol                               | Test Conditions<br>Unless Otherwise Specified<br>V <sub>+</sub> = 5 V, ± 10 %, V <sub>IN</sub> = 0.8 V or 2.4 V <sup>e</sup> | Temp. <sup>a</sup> | D Suffix<br>- 40 °C to 85 °C |                   |                   | Unit |
|   |                                      |  |                    | Min. <sup>b</sup>            | Typ. <sup>c</sup> | Max. <sup>b</sup> |      |
| <b>Analog Switch</b>                      |                                      |  |                    |                              |                   |                   |      |
| Analog Signal Range <sup>d</sup>          | V <sub>ANALOG</sub>                  |  | Full               | 0                            |                   | 5                 | V    |
| Drain-Source On-Resistance                | R <sub>DS(on)</sub>                  | V <sub>NO</sub> or V <sub>NC</sub> = 3.5 V, V <sub>+</sub> = 4.5 V<br>I <sub>COM</sub> = 5 mA                                | Room<br>Full       |                              | 30                | 60<br>75          | Ω    |
| R <sub>DS(on)</sub> Match <sup>d</sup>    | ΔR <sub>DS(on)</sub>                 | V <sub>NO</sub> or V <sub>NC</sub> = 3.5 V   | Room               |                              | 0.4               | 2                 |      |
| R <sub>DS(on)</sub> Flatness <sup>f</sup> | R <sub>DS(on)</sub><br>Flatness      | V <sub>NO</sub> or V <sub>NC</sub> = 1, 2 and 3 V  | Room               |                              | 2                 | 6                 |      |
| NO or NC Off Leakage Current              | I <sub>NO/NC(off)</sub>              | V <sub>NO</sub> or V <sub>NC</sub> = 1 V/4 V, V <sub>COM</sub> = 4 V/1 V   | Room<br>Full       | - 100<br>- 5000              | 10                | 100<br>5000       | pA   |
| COM Off Leakage Current                   | I <sub>COM(off)</sub>                | V <sub>COM</sub> = 1 V/4 V, V <sub>NO</sub> or V <sub>NC</sub> = 4 V/1 V   | Room<br>Full       | - 100<br>- 5000              | 10                | 100<br>5000       |      |
| Channel-On Leakage Current                | I <sub>COM(on)</sub>                 | V <sub>COM</sub> = V <sub>NO</sub> or V <sub>NC</sub> = 1 V/4 V  | Room<br>Full       | - 200<br>- 10 000            |                   | 200<br>10 000     |      |
| <b>Digital Control</b>                    |                                      |  |                    |                              |                   |                   |      |
| Input Current                             | I <sub>INL</sub> or I <sub>INH</sub> |  | Full               |                              | 1                 |                   | μA   |
| <b>Dynamic Characteristics</b>            |                                      |  |                    |                              |                   |                   |      |
| Turn-On Time                              | t <sub>ON</sub>                      | V <sub>NO</sub> or V <sub>NC</sub> = 3 V   | Room<br>Full       |                              | 35                | 75<br>150         | ns   |
| Turn-Off Time                             | t <sub>OFF</sub>                     |  | Room<br>Full       |                              | 20                | 50<br>100         |      |
| Charge Injection <sup>d</sup>             | Q <sub>INJ</sub>                     | C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω  | Room               |                              | 2                 | 5                 | pC   |
| Off-Isolation                             | OIRR                                 | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz  | Room               |                              | - 74              |                   | dB   |
| Crosstalk                                 | X <sub>TALK</sub>                    |  | Room               |                              | - 90              |                   |      |
| NC and NO Capacitance                     | C <sub>(off)</sub>                   | f = 1 MHz  | Room               |                              | 7                 |                   | pF   |
| Channel-On Capacitance                    | C <sub>D(on)</sub>                   |  | Room               |                              | 20                |                   |      |
| COM-Off Capacitance                       | C <sub>COM(off)</sub>                |  | Room               |                              | 13                |                   |      |
| <b>Power Supply</b>                       |                                      |  |                    |                              |                   |                   |      |
| Power Supply Range                        | V <sub>+</sub>                       |  |                    | 2.7                          |                   | 12                | V    |
| Power Supply Current                      | I <sub>+</sub>                       | V <sub>+</sub> = 5.5 V, V <sub>IN</sub> = 0 V or 5.5 V   |                    |                              |                   | 1                 | μA   |

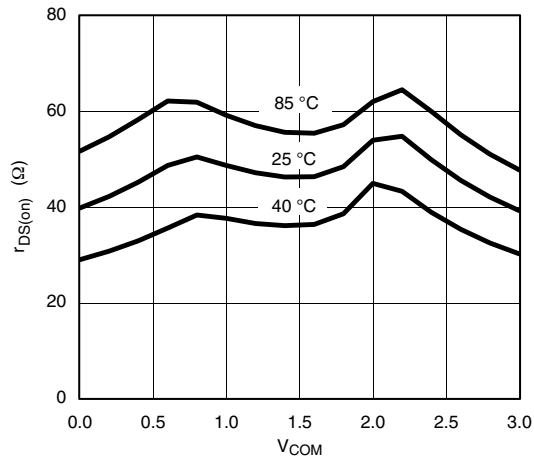
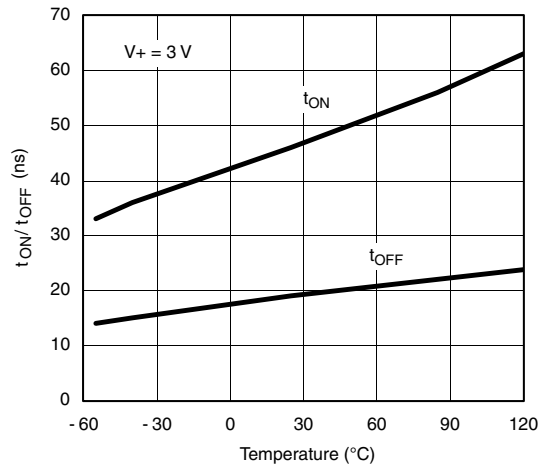
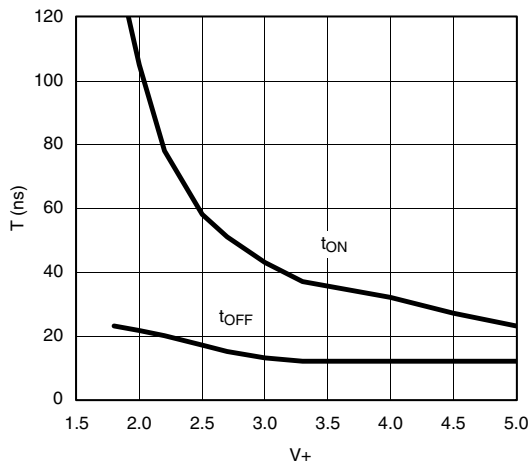
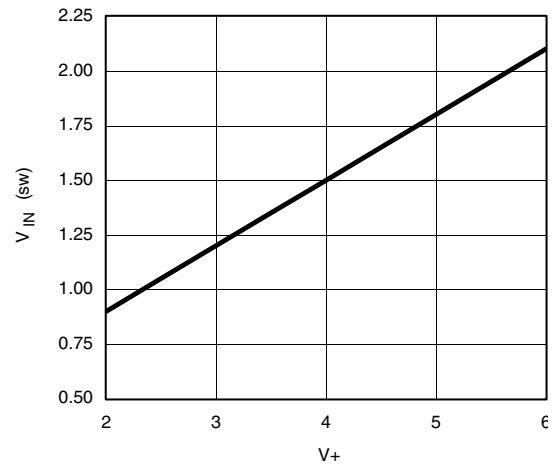
Notes:

- a. Room = 25 °C, full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V<sub>IN</sub> = input voltage to perform proper function.
- f. Difference of min and max values.

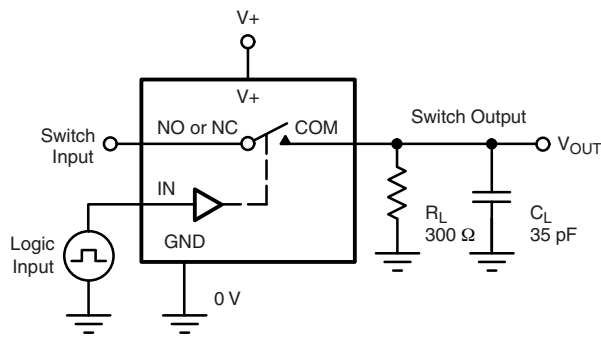
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)



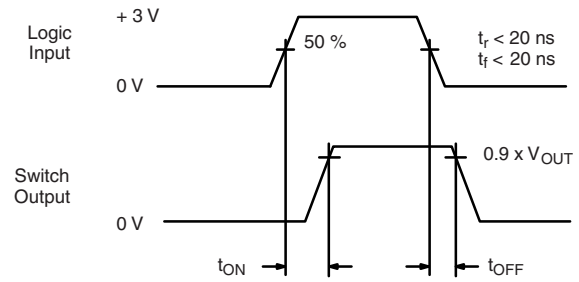
**TYPICAL CHARACTERISTICS** (25°C, unless otherwise noted)

 **$R_{DS}$  vs.  $V_{COM}$** 

**Switching Time vs. Temperature**

 **$t_{ON}/t_{OFF}$  vs. Power Supply Voltage**

**Input Switching Point vs. Power Supply Voltage**

### TEST CIRCUITS



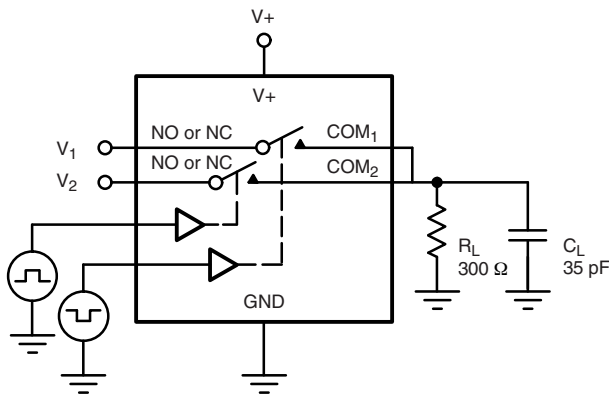
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

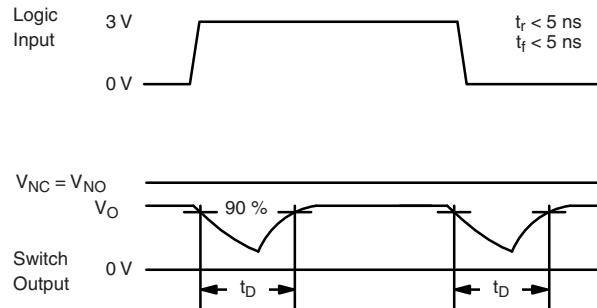
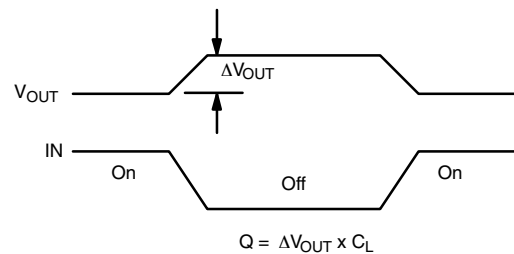
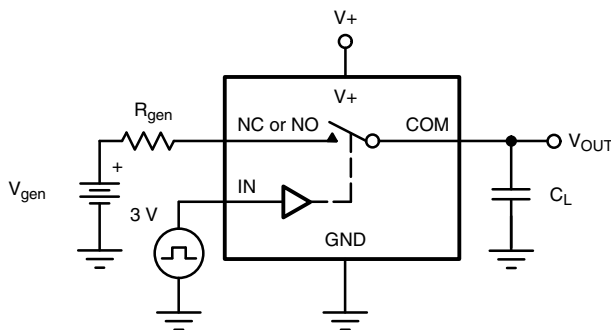
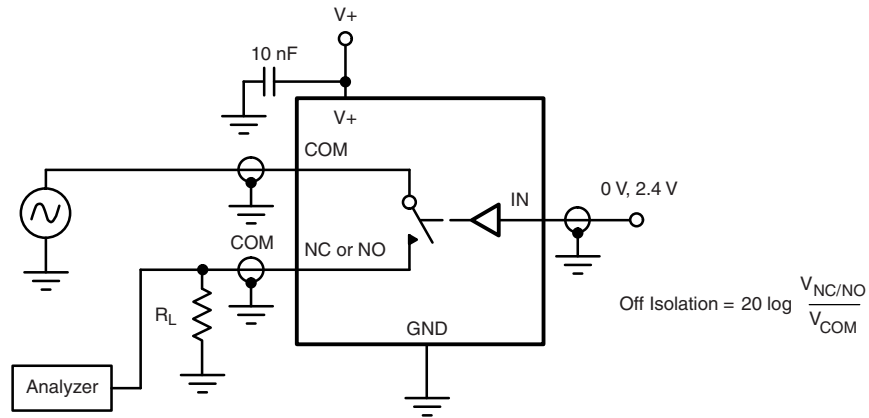
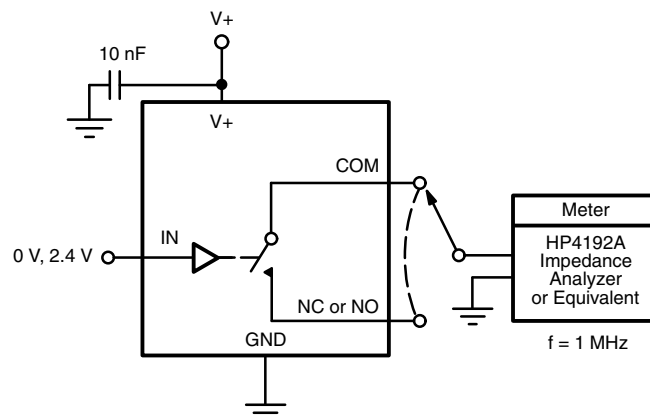


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

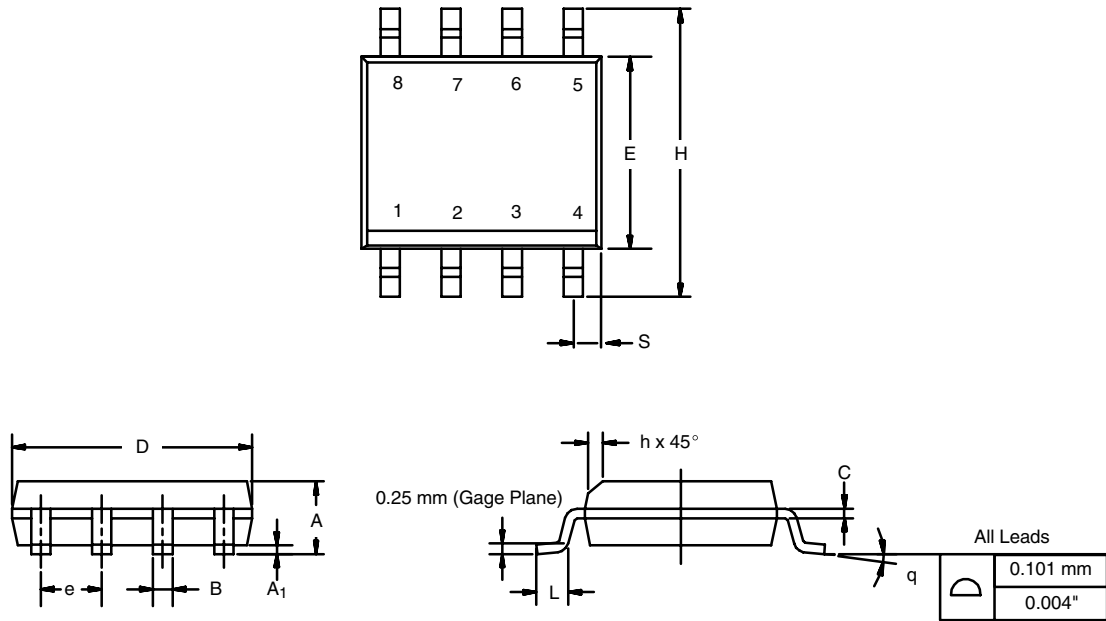
Figure 3. Charge Injection

**TEST CIRCUITS**

**Figure 4. Off-Isolation**

**Figure 5. Channel Off/On Capacitance**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70862](http://www.vishay.com/ppg?70862).

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



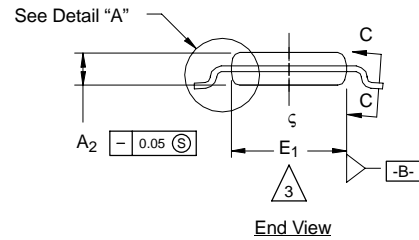
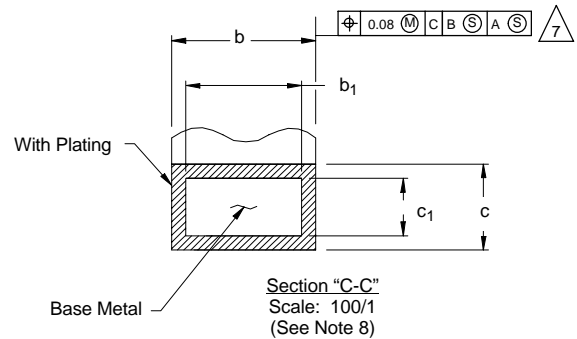
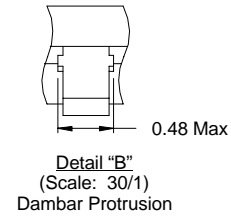
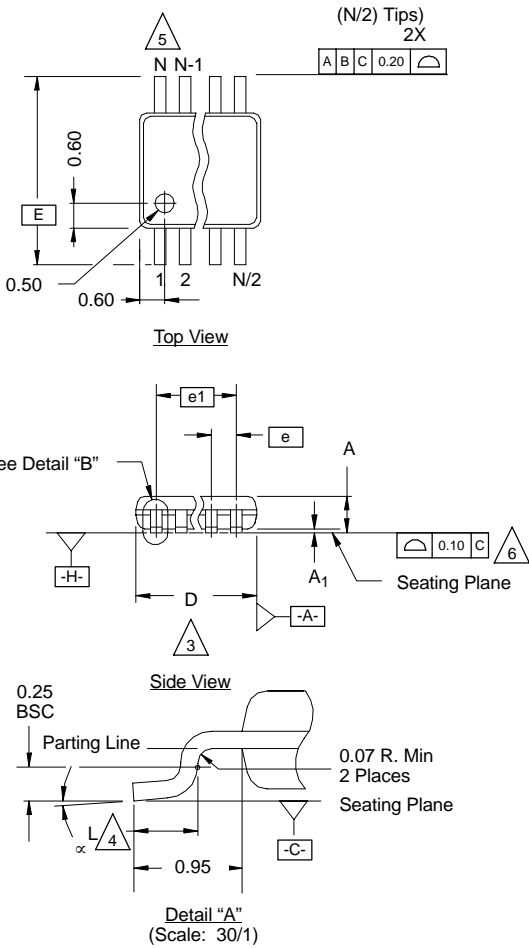
| DIM                            | MILLIMETERS |      | INCHES    |       |
|--------------------------------|-------------|------|-----------|-------|
|                                | Min         | Max  | Min       | Max   |
| A                              | 1.35        | 1.75 | 0.053     | 0.069 |
| A <sub>1</sub>                 | 0.10        | 0.20 | 0.004     | 0.008 |
| B                              | 0.35        | 0.51 | 0.014     | 0.020 |
| C                              | 0.19        | 0.25 | 0.0075    | 0.010 |
| D                              | 4.80        | 5.00 | 0.189     | 0.196 |
| E                              | 3.80        | 4.00 | 0.150     | 0.157 |
| e                              | 1.27 BSC    |      | 0.050 BSC |       |
| H                              | 5.80        | 6.20 | 0.228     | 0.244 |
| h                              | 0.25        | 0.50 | 0.010     | 0.020 |
| L                              | 0.50        | 0.93 | 0.020     | 0.037 |
| q                              | 0°          | 8°   | 0°        | 8°    |
| S                              | 0.44        | 0.64 | 0.018     | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06 |             |      |           |       |
| DWG: 5498                      |             |      |           |       |





**MSOP: 8-LEADS**

JEDEC Part Number: MO-187, (Variation AA and BA)



**NOTES:**

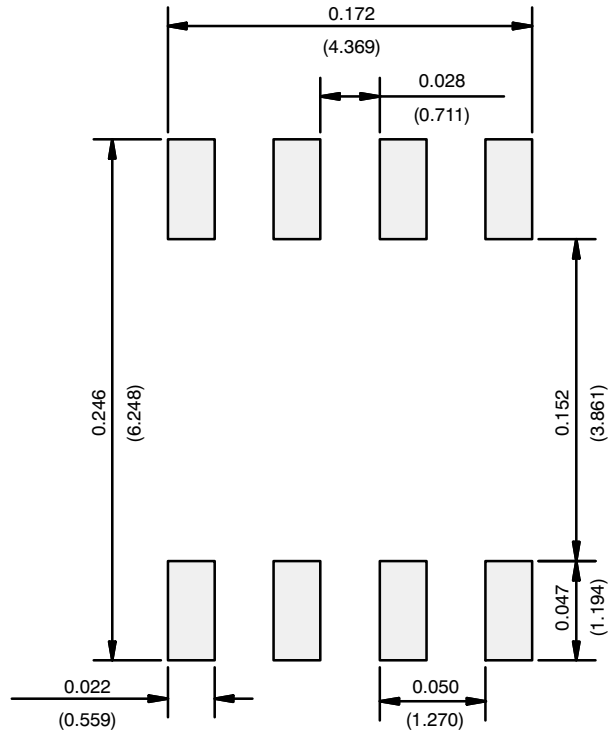
- Die thickness allowable is  $0.203 \pm 0.0127$ .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E<sub>1</sub>" do not include mold flash or protrusions, and are measured at Datum plane [-H-], mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums [-A-] and [-B-] to be determined Datum plane [-H-].
- Exposed pad area in bottom side is the same as teh leadframe pad size.

**N = 8L**

| Dim            | MILLIMETERS |      |      | Note |
|----------------|-------------|------|------|------|
|                | Min         | Nom  | Max  |      |
| A              | -           | -    | 1.10 |      |
| A <sub>1</sub> | 0.05        | 0.10 | 0.15 |      |
| A <sub>2</sub> | 0.75        | 0.85 | 0.95 |      |
| b              | 0.25        | -    | 0.38 | 8    |
| b <sub>1</sub> | 0.25        | 0.30 | 0.33 | 8    |
| c              | 0.13        | -    | 0.23 |      |
| c <sub>1</sub> | 0.13        | 0.15 | 0.18 |      |
| D              | 3.00 BSC    |      |      | 3    |
| E              | 4.90 BSC    |      |      |      |
| E <sub>1</sub> | 2.90        | 3.00 | 3.10 | 3    |
| e              | 0.65 BSC    |      |      |      |
| e <sub>1</sub> | 1.95 BSC    |      |      |      |
| L              | 0.40        | 0.55 | 0.70 | 4    |
| N              | 8           |      |      | 5    |
| α              | 0°          | 4°   | 6°   |      |

ECN: T-02080—Rev. C, 15-Jul-02  
DWG: 5867

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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