# DIRECTPATH™ STEREO LINE DRIVER, ADJUSTABLE GAIN

**Check for Samples: DRV601**

## FEATURES

- **External Gain Setting Resistors**
- **Space Saving Package**
  - **20-Pin, 4 mm × 4 mm Thin QFN, Thermally Optimized PowerPAD™ Package**
- **Ground-Referenced Outputs Eliminate DC-Blocking Capacitor**
  - **Reduce Board Area**
  - **Reduce Component Cost**
  - **Improve THD+N Performance**
  - **No Degradation of Low-Frequency Response Due to Output Capacitors**
- **Wide Power Supply Range: 1.8 V to 4.5 V**
- **2 Vrms/Ch Output Voltage into 600 Ω at 3.3 V supply**
- **Independent Right and Left Channel Shutdown Control**
- **Short-Circuit and Thermal Protection**
- **Pop Reduction Circuitry**

## APPLICATIONS

- **Set-Top Boxes**
- **CD / DVD Players**
- **DVD-Receivers**
- **HTIB**
- **PDP / LCD TV's**

## DESCRIPTION

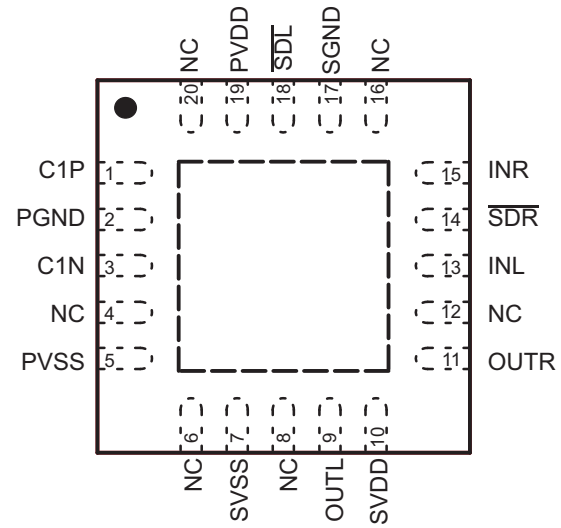
The DRV601 is a stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The DRV601 is capable of driving 2 Vrms into a 600-Ω load at 3.3 V. The device has external gain setting resistors, that support a gain range of -1V/V to -10V/V, and line outputs that has ±8-kV IEC ESD protection. The device has independent shutdown control for the right and left audio channels.

The DRV601 is available in a 4 mm × 4 mm Thin QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**RTJ (QFN) PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | QFN | | |
| C1P | 1 | I/O | Charge pump flying capacitor positive terminal |
| PGND | 2 | I | Power ground, connect to ground. |
| C1N | 3 | I/O | Charge pump flying capacitor negative terminal |
| NC | 4, 6, 8, 12, 16, 20 | | No connection |
| PVSS | 5 | O | Output from charge pump. |
| SVSS | 7 | I | Amplifier negative supply, connect to PVSS via star connection. |
| OUTL | 9 | O | Left audio channel output signal |
| SVDD | 10 | I | Amplifier positive supply, connect to PVDD via star connection. |
| OUTR | 11 | O | Right audio channel output signal |
| INL | 13 | I | Left audio channel input signal |
| $\overline{\text{SDR}}$ | 14 | I | Right channel shutdown, active low logic. |
| INR | 15 | I | Right audio channel input signal |
| SGND | 17 | I | Signal ground, connect to ground. |
| $\overline{\text{SDL}}$ | 18 | I | Left channel shutdown, active low logic. |
| PVDD | 19 | I | Supply voltage, connect to positive supply. |
| Exposed Pad | | | Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground. |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, $T_A$ = 25°C (unless otherwise noted)

| | | VALUE / UNIT |
|---|---|---|
| | Supply voltage, AVDD, PVDD | –0.3 V to 5.5 V |
| $V_I$ | Input voltage | $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V |
| $R_{(Load)}$ | Minimum load impedance | ≥ 100 Ω |
| $T_A$ | Operating free-air temperature range | –40°C to 85°C |
| $T_J$ | Operating junction temperature range | 0°C to 150°C |
| $T_{stg}$ | Storage temperature range | –65°C to 85°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICES (1) | PART NUMBER | SYMBOL |
|---|---|---|---|
| -40°C to 85°C | 20-pin, 4 mm × 4 mm QFN | DRV601RTJ(2) | AKQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RTJ package is only available taped and reeled. To order, add the suffix “R” to the end of the part number for a reel of 3000, or add the suffix “T” to the end of the part number for a reel of 250 (e.g., DRV601RTJR).

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SS}$ | Supply voltage, AVDD, PVDD | | 1.8 | 4.5(1) | V |
| $V_{IH}$ | High-level input voltage | $\overline{SDL}$, $\overline{SDR}$ | 1.5 | | V |
| $V_{IL}$ | Low-level input voltage | $\overline{SDL}$, $\overline{SDR}$ | | 0.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) Device can shut down for $V_{DD}$ > 4.5 V to prevent damage to the device.

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C (unless otherwise noted)

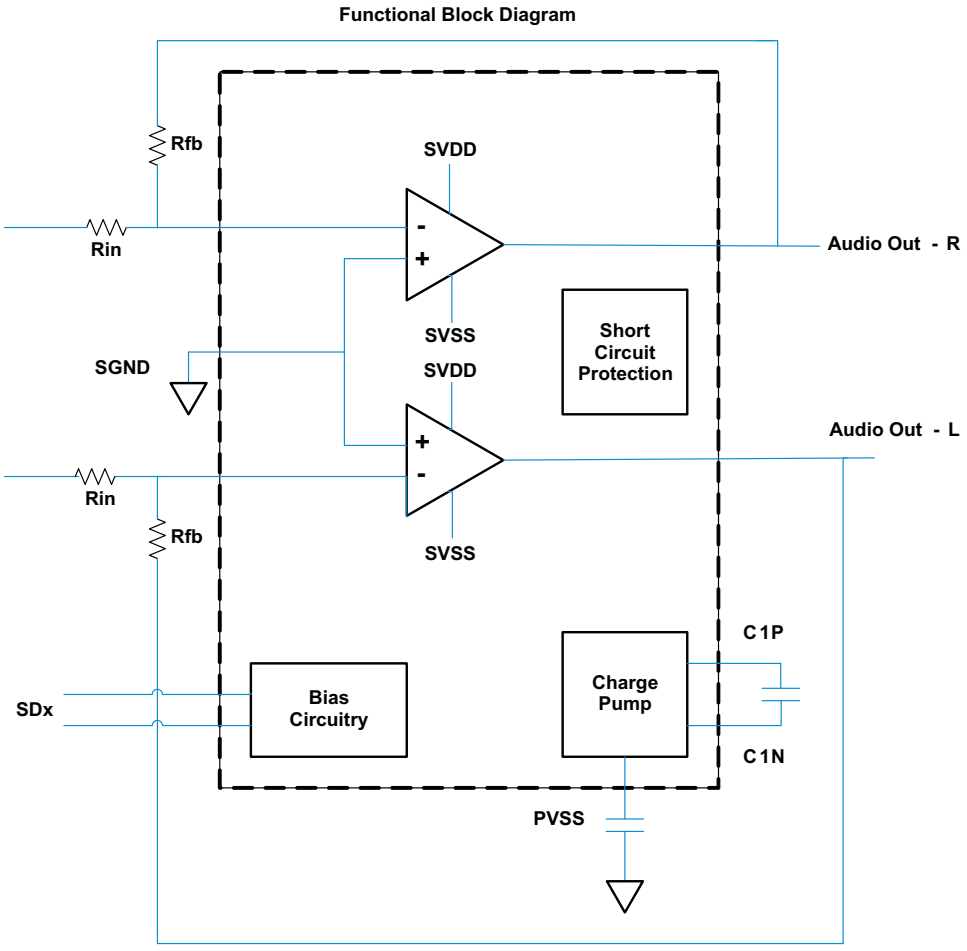
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\lvert V_{OS}\rvert$ | Output offset voltage | $V_{DD}$ = 1.8 V to 4.5 V, Inputs grounded | | | 8 | mV |
| PSRR | Power Supply Rejection Ratio | $V_{DD}$ = 1.8 V to 4.5 V | | 88 | | dB |
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = 3.3 V, $R_L$ = 600 Ω | 3.10 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = 3.3 V, $R_L$ = 600 Ω | | | –3.05 | V |
| $\lvert I_{IH}\rvert$ | High-level input current ($\overline{SDL}$, $\overline{SDR}$) | $V_{DD}$ = 4.5 V, $V_I$ = $V_{DD}$ | | | 1 | µA |
| $\lvert I_{IL}\rvert$ | Low-level input current ($\overline{SDL}$, $\overline{SDR}$) | $V_{DD}$ = 4.5 V, $V_I$ = 0 V | | | 1 | µA |
| $I_{DD}$ | Supply Current | $V_{DD}$ = 1.8 V, No load, $\overline{SDL}$= $\overline{SDR}$ = $V_{DD}$ | | 5.3 | | mA |
| | | $V_{DD}$ = 3.3 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = $V_{DD}$ | | 7.1 | | |
| | | $V_{DD}$ = 4.5 V, No load, $\overline{SDL}$ = $\overline{SDR}$ = $V_{DD}$ | | 8.7 | | |
| | | Shutdown mode, $V_{DD}$ = 1.8 V to 4.5 V | | | 1 | µA |

## OPERATING CHARACTERISTICS

$V_{DD}$ = 3.3 V , $T_A$ = 25°C, $R_L$ = 600 Ω, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1 µF , $C_{IN}$ = 1 µF, $R_{in}$ = 10 kΩ, $R_{fb}$ = 20 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage(Outputs In Phase) | THD = 1%, $V_{DD}$ = 3.3 V, f = 1 kHz | | 2.1 | | $V_{RMS}$ |
| | | THD = 1%, $V_{DD}$ = 4.5 V, f = 1 kHz | | 2.7 | | |
| | | THD = 1%, $V_{DD}$ = 4.5 V, f = 1 kHz, $R_L$ = 100 kΩ | | 2.8 | | |
| THD+N | Total harmonic distortion plus noise | $V_O$ = 2 Vrms, f = 1 kHz | | 0.008% | | |
| | | $V_O$ = 2 Vrms, f = 6.67 kHz | | 0.030% | | |
| | Crosstalk | $V_O$ = 2 Vrms, f = 1 kHz | | -80 | | dB |
| $A_{vo}$ | Open-loop voltage gain | | | 155 | | dB |
| $R_{in}$ | Input resistor range | | 1 | 10 | 47 | kΩ |
| $R_{fb}$ | Feedback resistor range | | 4.7 | 20 | 100 | kΩ |
| | Slew rate | | | 2.2 | | V/µs |
| | Maximum capacitive load | | | 300 | | pF |
| $V_n$ | Noise output voltage | 22-kHz filter, A-weighted | | 10 | | µVrms |
| ESD | Electrostatic discharge | OUTR, OUTL | | ±8 | | kV |
| $f_{osc}$ | Charge pump switching frequency | | 225 | 450 | 690 | kHz |
| | Start-up time from shutdown | | | 450 | | µs |
| | Input impedance | | 1 | | | MΩ |
| SNR | Signal-to-noise ratio | $V_o$ = 2 Vrms (THD+N = 0.1%), 22-kHz BW, A-weighted | | 105 | | dB |
| $G_{(bw)}$ | Unity Gain Bandwidth | | | 3.5 | | MHz |
| | Thermal shutdown | Threshold | 150 | | 170 | °C |
| | | Hysteresis | | 15 | | °C |

## Functional Block Diagram



## TYPICAL CHARACTERISTICS

$C_{(PUMP)} = C_{(PVSS)} = 1\ \mu F$ , $C_{IN} = 1\ \mu F$, $R_{in} = 10\ k\Omega$, $R_{fb} = 20\ k\Omega$ (unless otherwise noted)

### Table of Graphs

| | | FIGURE |
|---|---|---|
| Total harmonic distortion + noise | vs Output Voltage | 1-6 |
| Total harmonic distortion + noise | vs Frequency | 7-8 |
| Quiescent supply current | vs Supply voltage | 9 |
| Output spectrum | | 10 |
| Gain and phase | vs Frequency | 11-12 |

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

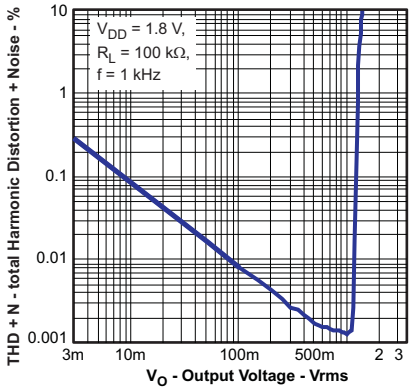



**Figure 1.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

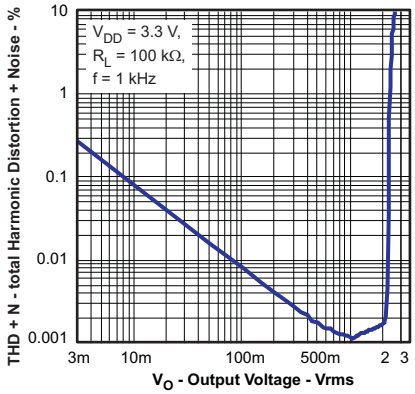



**Figure 2.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

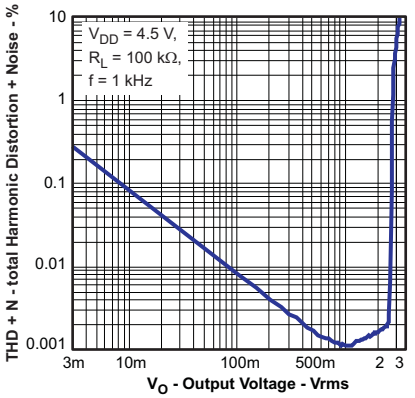



**Figure 3.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

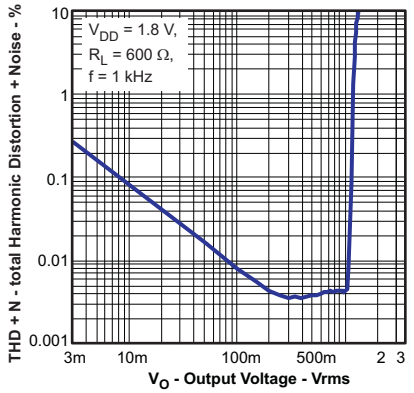



**Figure 4.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

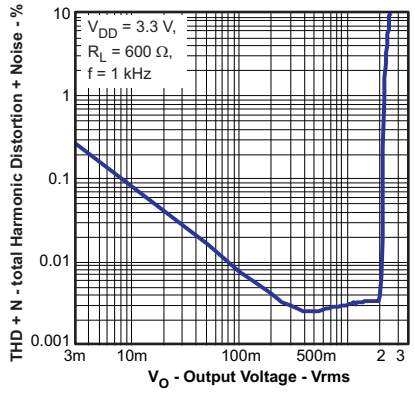



**Figure 5.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

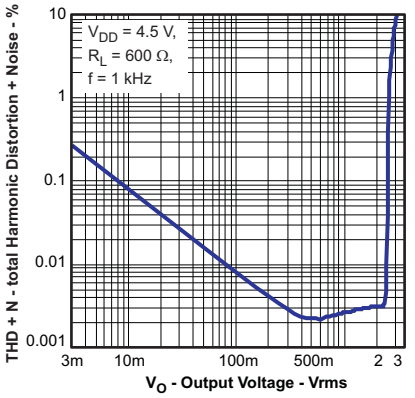



**Figure 6.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

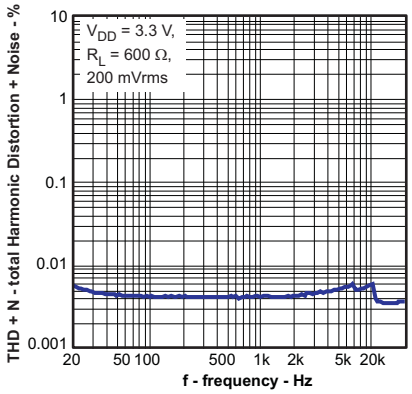



**Figure 7.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

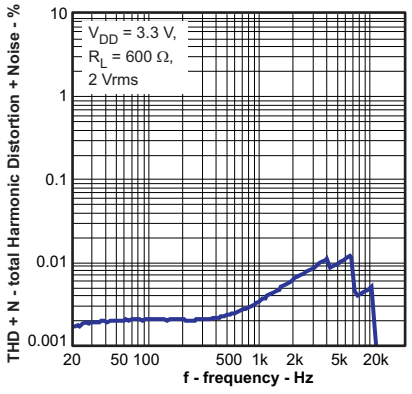



**Figure 8.**

**QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE**

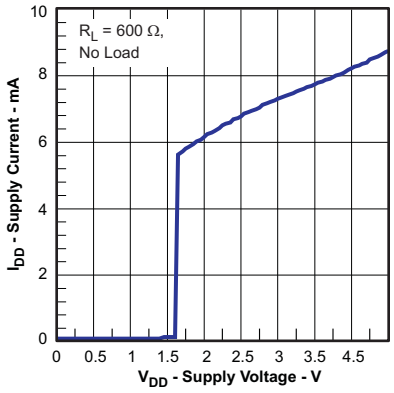



**Figure 9.**

**FFT vs FREQUENCY**

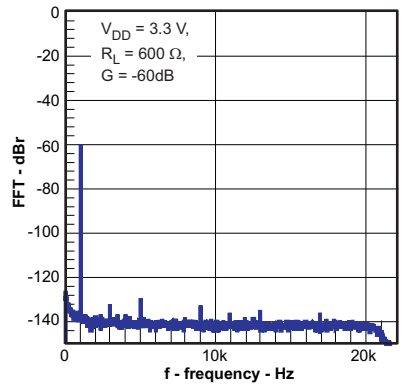



**Figure 10.**

**GAIN vs FREQUENCY**

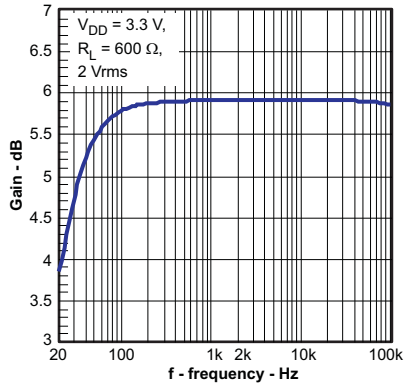



**Figure 11.**

**PHASE vs FREQUENCY**

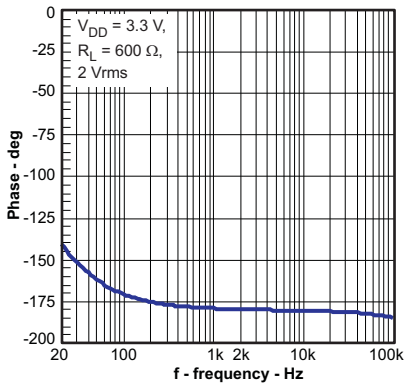



**Figure 12.**

## APPLICATION INFORMATION

### Line Driver Amplifiers

Single-supply Line Driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 13 illustrates the conventional Line Driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value. The line load (typical resistive values of 600 Ω to 10 kΩ) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance ($R_L$), the capacitor ($C_O$), and the cutoff frequency ($f_C$).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

$C_O$ can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If $f_C$ is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

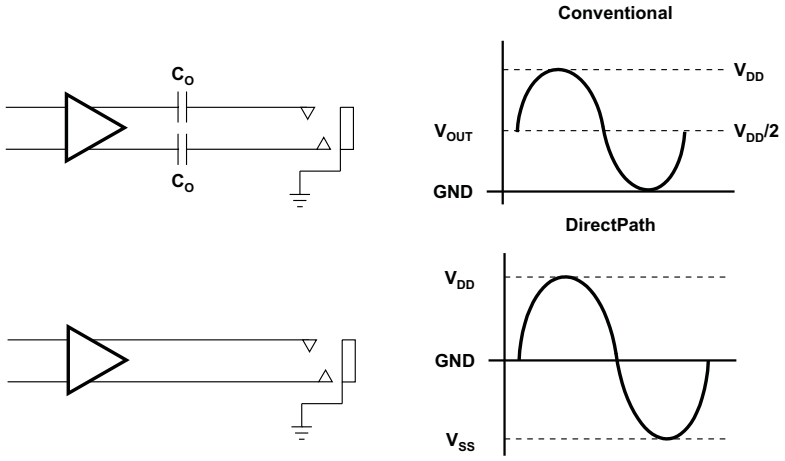



**Figure 13. Amplifier Applications**

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of Figure 13 illustrate the ground-referenced Line Driver architecture. This is the architecture of the DRV601.

## Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1µF is typical. Capacitor values that are smaller than 1µF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

## Decoupling Capacitors

The DRV601 is a DirectPath™ Line Driver amplifier that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2µF, placed as close as possible to the device $V_{DD}$ lead works best. Placing this decoupling capacitor close to the DRV601 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

## Gain setting resistors ranges

The gain setting resistors, $R_{in}$ and $R_{fb}$, must be chosen so that noise, stability and input capacitor size of the DRV601 is kept within acceptable limits. Voltage gain is defined as $R_{fb}$ divided by $R_{in}$.

Selecting values that are too low demands a large input ac-coupling capacitor, $C_{IN}$ . Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

**Table 1. Recommended Resistor Values**

| Gain | Input Resistor Value, $R_{in}$ | Feedback Resistor Value, $R_{fb}$ |
|---|---|---|
| -1 V/V | 10 kΩ | 10 kΩ |
| -1.5 V/V | 10 kΩ | 15 kΩ |
| -2 V/V | 10 kΩ | 20 kΩ |
| -10 V/V | 4,7 kΩ | 47 kΩ |

## Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV601. These capacitors block the DC portion of the audio source and allow the DRV601 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, $R_{in}$. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from the gain table above, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{3}$$

## Supply Voltage Limiting At 4.5 V

The DRV601 have a built-in charge pump which serves to generate a negative rail for the line driver. Because the line driver operates from a positive voltage and negative voltage supply, circuitry has been implemented to protect the devices in the amplifier from an overvoltage condition. Once the supply is above 4.5 V, the DRV601 can shut down in an overvoltage protection mode to prevent damage to the device. The DRV601 resume normal operation once the supply is reduced to 4.5 V or lower.

## Capacitive load

The DRV601 has the ability to drive a high capacitive load up to 330pF directly, higher capacitive loads can be accepted by adding a series resistor of 10Ω or larger. The figure below shows a 10kHz signal into a 470pF capacitor using the 10R series resistor.

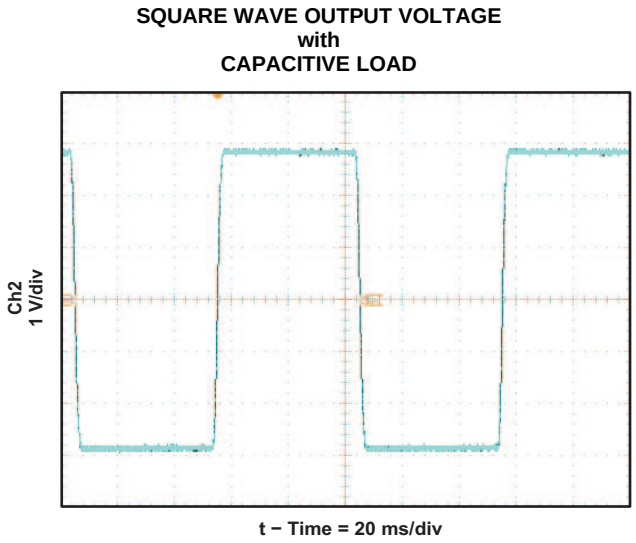



**Figure 14.**

## Layout Recommendations

A proposed layout for the DRV601 can be seen in the DRV601EVM user's guide, SLOU215, and the Gerber files can be downloaded on www.ti.com, open the DRV601 product folder and look in the Tools & Software folder.

### Exposed Pad On DRV601RTJ Package

The exposed metal pad on the DRV601RTJ package must be soldered down to a pad on the PCB in order to maintain reliability. *The pad on the PCB should be allowed to float and not be connected to ground or power*. Connecting this pad to power or ground prevents the device from working properly because it is connected internally to PVSS.

### SGND and PGND Connections

The SGND and PGND pins of the DRV601 must be routed back to the decoupling capacitor separately in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

### Gain setting resistors

The gain setting resistors, $R_{in}$ and $R_{fb}$ , must be placed close to pin 13 respectively pin 17 to minimize the capacitive loading on these input pins and to ensure maximum stability of the DRV601. For the recommenced PCB layout, see the DRV601EVM user guide.

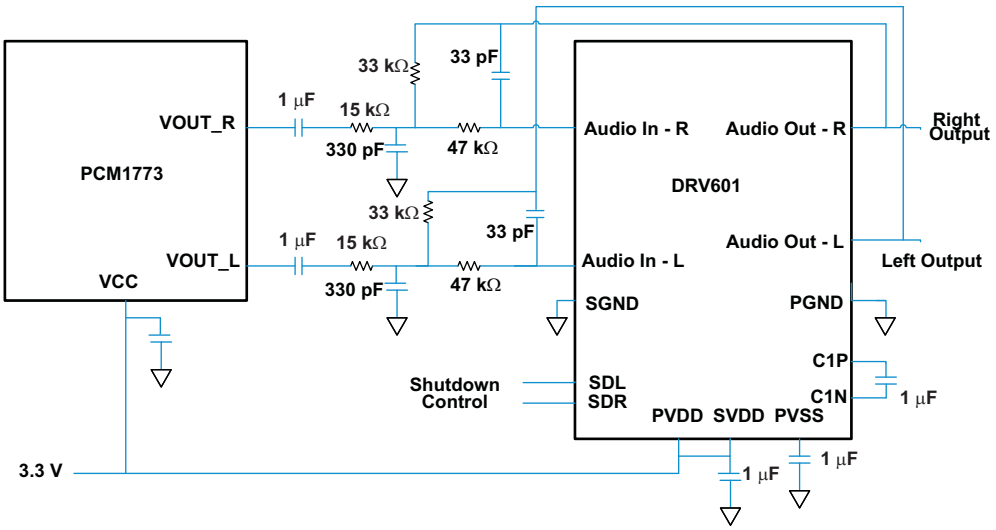



**Figure 15. Application Circuit**

## REVISION HISTORY

**Changes from Original (January 2008) to Revision A** **Page**

- Changed $T_A$ From: -40°C to 85°C To: 0°C to 70°C (AVAILABLE OPTIONS table) ..... 3

**Changes from Revision A (August 2008) to Revision B** **Page**

- Changed $T_A$ From: 0°C to 70°C To: -40°C to 85°C (ABSOLUTE MAXIMUM RATING table) ..... 3
- Changed $T_A$ From: 0°C to 70°C To: -40°C to 85°C (AVAILABLE OPTIONS table) ..... 3
- Changed $T_A$ From: 0°C to 70°C To: -40°C to 85°C (RECOMMENDED OPERATING CONDITIONS table) ..... 3

**Changes from Revision B (Novemebr 2008) to Revision C** **Page**

- Changed values - Charge pump switching frequency. From: Min = 280 Typ = 320 Max = 420 To: Min = 225 Typ = 450 Max = 690 ..... 4

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV601RTJR | ACTIVE | QFN | RTJ | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV601 | Samples |
| DRV601RTJRG4 | ACTIVE | QFN | RTJ | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV601 | Samples |
| DRV601RTJT | ACTIVE | QFN | RTJ | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | DRV601 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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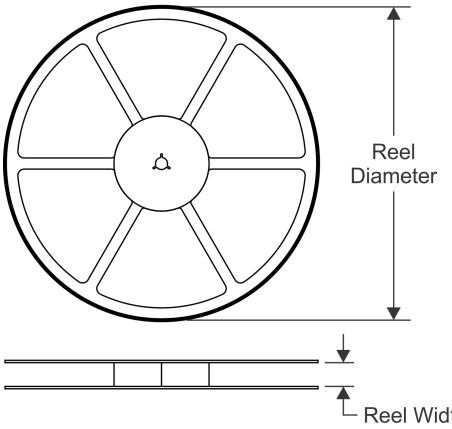
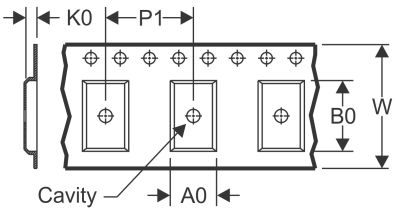
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

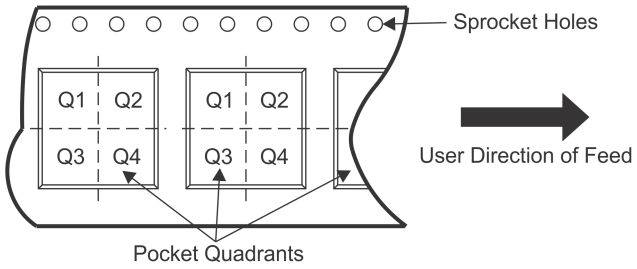



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

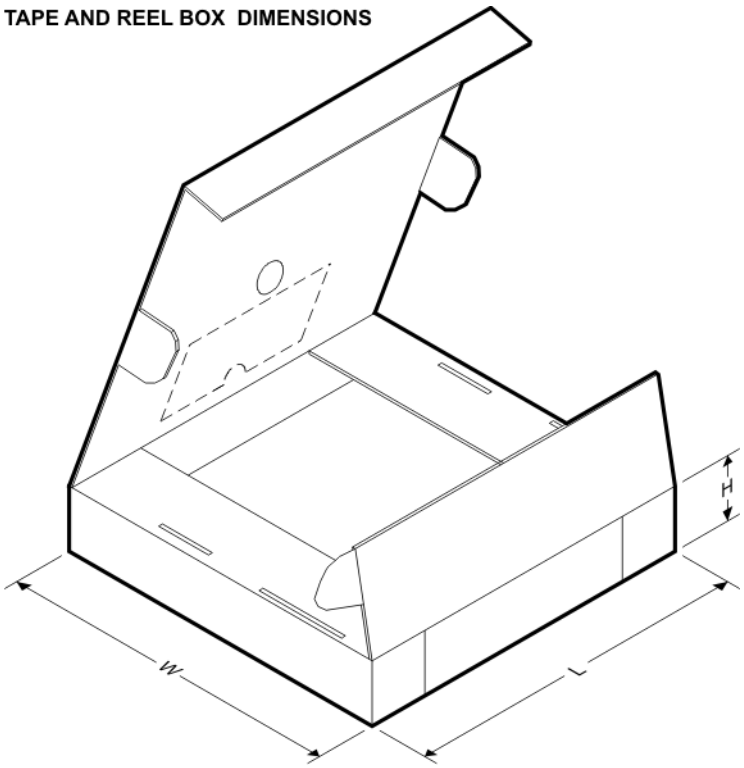
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV601RTJR | QFN | RTJ | 20 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| DRV601RTJT | QFN | RTJ | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

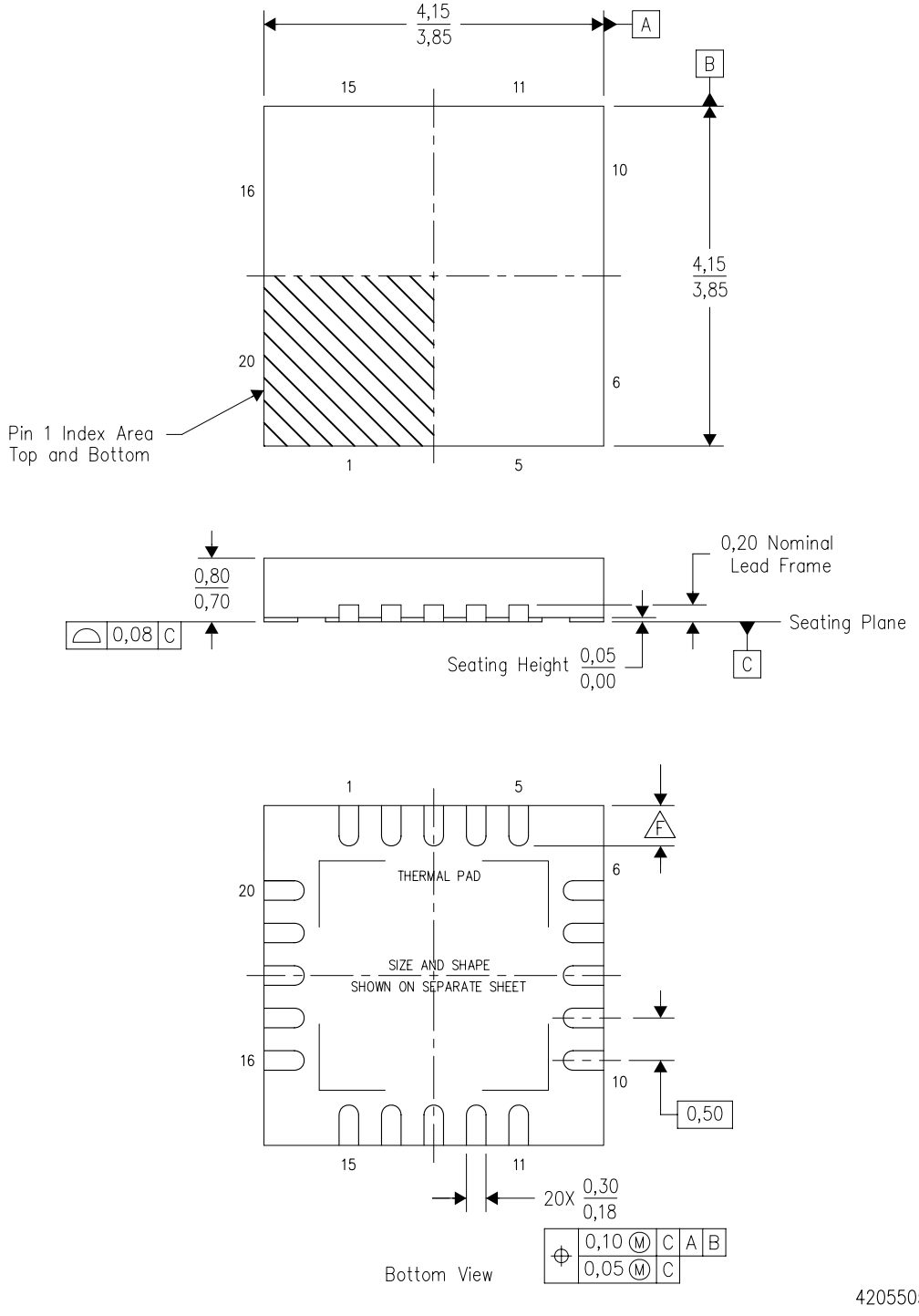
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV601RTJR | QFN | RTJ | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| DRV601RTJT | QFN | RTJ | 20 | 250 | 210.0 | 185.0 | 35.0 |

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

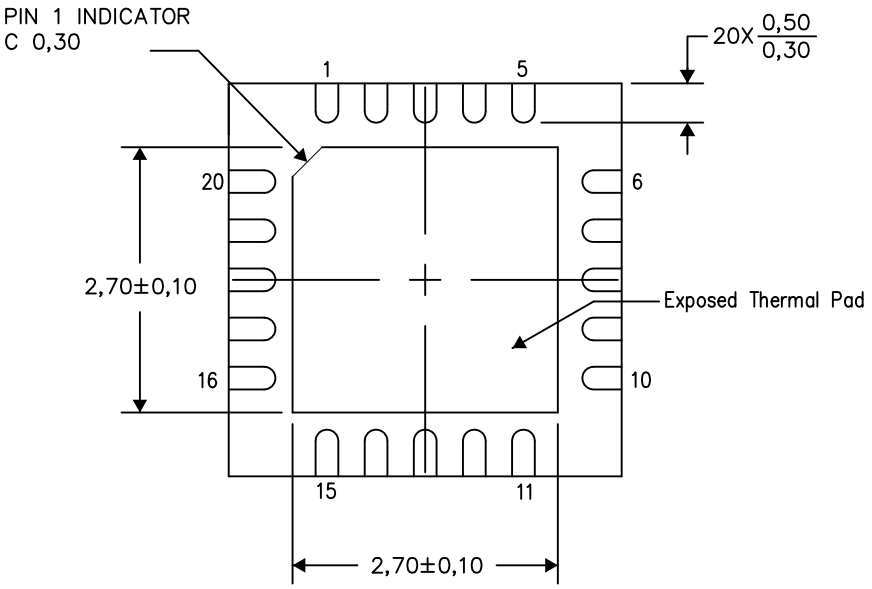
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



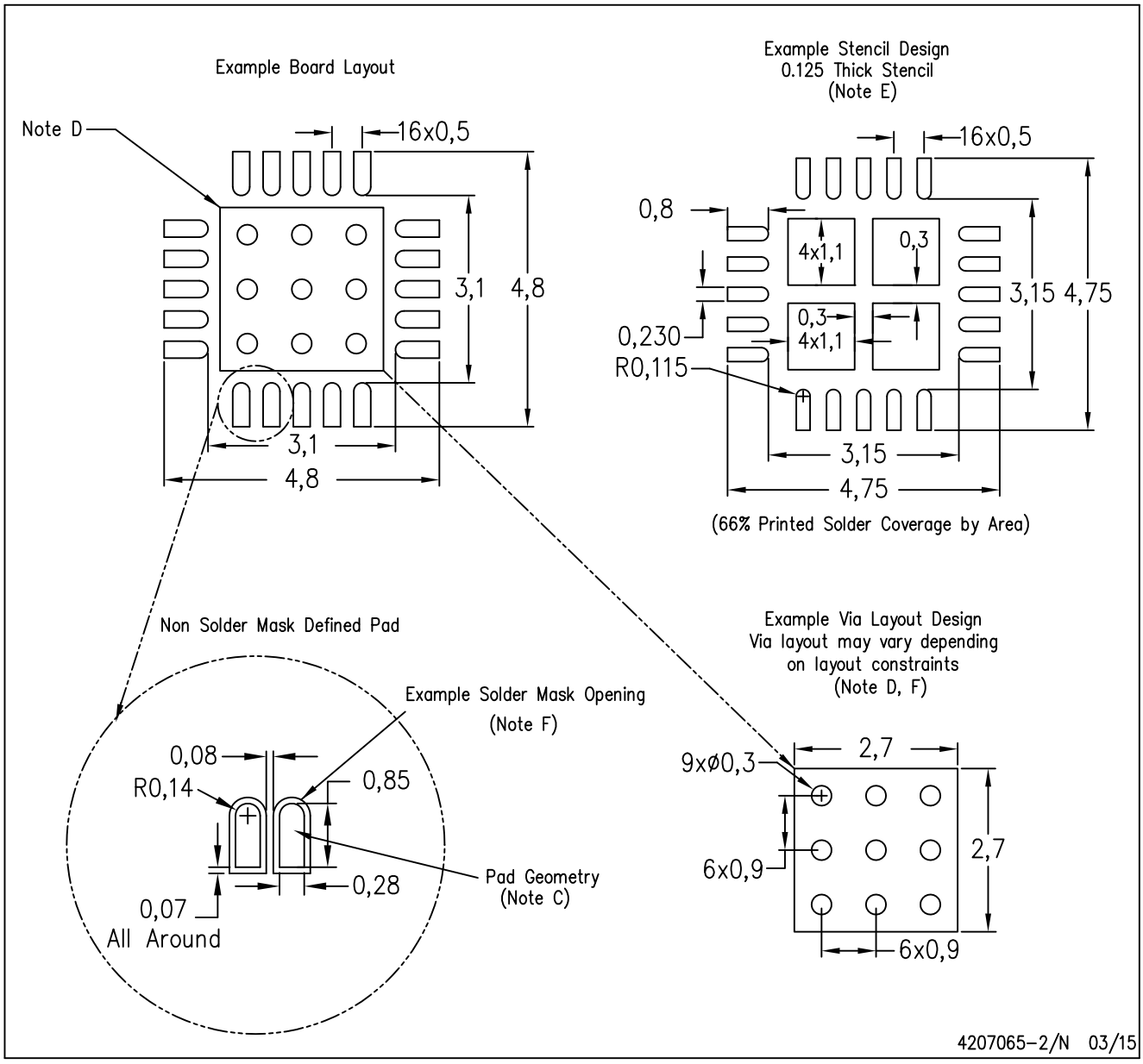

Bottom View

Exposed Thermal Pad Dimensions

4206256–2/V 05/15

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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