DRV8662 Piezo Haptic Driver with Integrated Boost Converter

1 Features

- High-Voltage Piezo Haptic Driver
  - Drives up to 100 nF at 200 V_{PP} and 300 Hz
  - Drives up to 150 nF at 150 V_{PP} and 300 Hz
  - Drives up to 330 nF at 100 V_{PP} and 300 Hz
  - Drives up to 680 nF at 50 V_{PP} and 300 Hz
  - Differential Output
- Integrated Boost Converter
  - Adjustable Boost Voltage
  - Adjustable Current Limit
  - Integrated Power FET and Diode
  - No Transformer Required
- Fast Start Up Time of 1.5 ms
- Wide Supply Voltage Range of 3.0 V to 5.5 V
- 1.8V Compatible Digital Pins
- Thermal Protection
- Available in a 4 mm × 4 mm × 0.9 mm QFN package (RGP)

2 Applications

- Mobile Phones
- Tablets
- Portable Computers
- Keyboards and Mice
- Touch Enabled Devices

3 Description

The DRV8662 is a single-chip piezo haptic driver with integrated 105 V boost switch, integrated power diode, and integrated fully-differential amplifier. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be either differential or single-ended. The DRV8662 supports four GPIO-controlled gains: 28.8 dB, 34.8 dB, 38.4 dB, and 40.7 dB.

The boost voltage is set using two external resistors, and the boost current limit is programmable via the R_{EXT} resistor. The boost converter architecture will not allow the demand on the supply current to exceed the limit set by the R_{EXT} resistor; therefore, the DRV8662 is well-suited for portable applications. This feature also allows the user to optimize the DRV8662 circuit for a given inductor based on the desired performance requirements.

A typical start-up time of 1.5 ms makes the DRV8662 an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when over driven.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8662	VQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

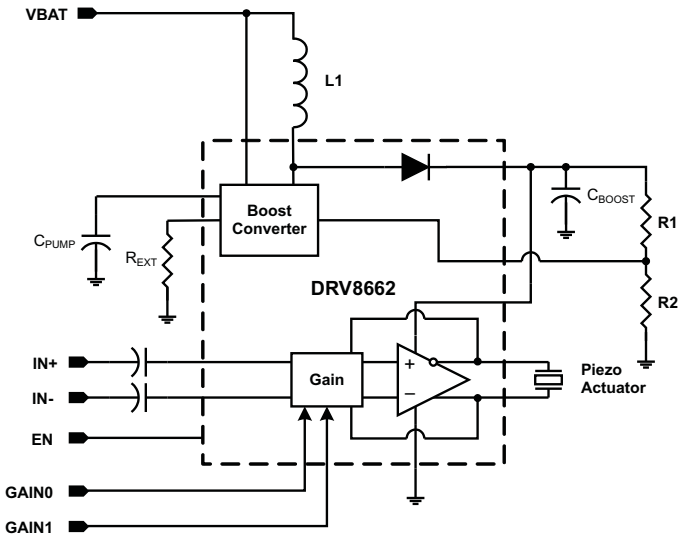


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2012) to Revision B — **Page**

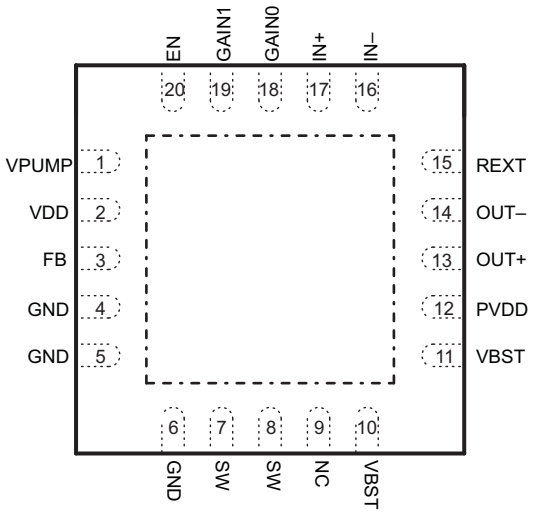
- Added Device Information and ESD Rating tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Added the Thermal Information table after the Recommend Operating Conditions table. ... 5

Changes from Original (June 2011) to Revision A — **Page**

- Added C_L, V_{IL}, V_{IH} specs to Recommended Operating Conditions table. ... 4
- Added amplifier bandwidth spec (BW) to the Electrical Characteristics table for each gain setting ... 5

6 Pin Configuration and Functions

QFN (RGP)
Top View



Pin Functions

PIN		INPUT/ OUTPUT/ POWER (I/O/P)	DESCRIPTION
NAME	NO. (RGP)		
EN	20	I	Chip enable
FB	3	I	Boost feedback
GAIN0	18	I	Gain programming pin – LSB
GAIN1	19	I	Gain programming pin – MSB
GND	4, 5, 6	P	Ground
IN+	17	I	Non-inverting input (If unused, connect to GND through capacitor)
IN–	16	I	Inverting input (If unused, connect to GND through capacitor)
OUT+	13	O	Non-inverting output
OUT–	14	O	Inverting output
PVDD	12	P	Amplifier supply voltage
REXT	15	I	Resistor to ground, sets boost current limit
SW	7, 8	P	Internal boost switch pin
VBST	10, 11	P	Boost output voltage
VDD	2	P	Power supply (connect to battery)
VPUMP	1	P	Internal Charge-pump voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Supply voltage	VDD	–0.3	6.0	V
V_I	Input voltage	IN+, IN–, EN, GAIN0, GAIN1, FB	–0.3	V_{DD} +0.3	V
	Boost/Output Voltage	PVDD, SW, OUT+, OUT–		120	V
T_A	Operating free-air temperature range		–40	70	°C
T_J	Operating junction temperature range		–40	150	°C
Storage temperature, T_{stg}			–65	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	VDD		3.0		5.5	V
V_{BST}	Boost voltage	VBST		15		105	V
V_{IN}	Differential input voltage				1.8 (1)		V
C_L	Load capacitance	VBST = 105 V, Frequency = 500 Hz, $V_{O,PP}$ = 200 V				50	nF
		VBST = 105 V, Frequency = 300 Hz, $V_{O,PP}$ = 200 V				100	
		VBST = 80 V, Frequency = 300 Hz, $V_{O,PP}$ = 150 V				150	
		VBST = 55 V, Frequency = 300 Hz, $V_{O,PP}$ = 100 V				330	
		VBST = 30 V, Frequency = 300 Hz, $V_{O,PP}$ = 50 V				680	
		VBST = 25 V, Frequency = 300 Hz, $V_{O,PP}$ = 40 V				1	µF
		VBST = 15 V, Frequency = 300 Hz, $V_{O,PP}$ = 20 V				3	
V_{IL}	Digital input low voltage	EN, GAIN0, GAIN1	V_{DD} = 3.6 V			0.75	V
V_{IH}	Digital input high voltage	EN, GAIN0, GAIN1	V_{DD} = 3.6 V	1.4			V
R_{EXT}	Current limit control resistor			6		35	kΩ
L	Inductance for Boost Converter			3.3			µH

(1) Gains are optimized for a 1.8V peak input

7.4 Thermal Information

THERMAL METRIC[1]		DRV8662 RGP (20 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	8.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, $V_{O,PP} = V_{OUT+} - V_{OUT-}$ = 200 V, C_L = 47 nF, A_V = 40 dB, L = 4.7 µH (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert I_{IL} \rvert$	Digital input low current	EN, GAIN0, GAIN1	V_{DD} = 3.6 V, V_{IN} = 0 V			1	µA
$\lvert I_{IH} \rvert$	Digital input high current	EN, GAIN0, GAIN1	V_{DD} = 3.6 V, V_{IN} = V_{DD}			5	µA
I_{SD}	Shut down current	V_{DD} = 3.6 V, V_{EN} = 0 V			13		µA
I_{DDQ}	Quiescent current	V_{DD} = 3.6 V, V_{EN} = V_{DD}, VBST = 105 V, no signal			24		mA
		V_{DD} = 3.6 V, V_{EN} = V_{DD}, VBST = 80 V, no signal			13		mA
		V_{DD} = 3.6 V, V_{EN} = V_{DD}, VBST = 55 V, no signal			9		mA
		V_{DD} = 3.6 V, V_{EN} = V_{DD}, VBST = 30 V, no signal			5		mA
R_{IN}	Input impedance	All gains			100		kΩ
A_V	Amplifier gain	GAIN<1:0> = 00			28.8		dB
		GAIN<1:0> = 01			34.8		
		GAIN<1:0> = 10			38.4		
		GAIN<1:0> = 11			40.7		
BW	Amplifier Bandwidth	GAIN<1:0> = 00, $V_{O,PP}$ = 50 V, No Load			20		kHz
		GAIN<1:0> = 01, $V_{O,PP}$ = 100 V, No Load			10		
		GAIN<1:0> = 10, $V_{O,PP}$ = 150 V, No Load			7.5		
		GAIN<1:0> = 11, $V_{O,PP}$ = 200 V, No Load			5		
$I_{BAT,AVG}$	Average battery current during operation	V_{DD} = 3.6 V, C_L = 10 nF, f = 150 Hz, $V_{O,PP}$ = 200 V			75		mA
		V_{DD} = 3.6 V, C_L = 10 nF, f = 300 Hz, $V_{O,PP}$ = 200 V			115		
		V_{DD} = 3.6 V, C_L = 47 nF, f = 150 Hz, $V_{O,PP}$ = 200 V			210		
		V_{DD} = 3.6 V, C_L = 47 nF, f = 300 Hz, $V_{O,PP}$ = 200 V			400		
THD+N	Total harmonic distortion plus noise	f = 300 Hz, $V_{O,PP}$ = 200 V			1%		

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
t_{SU}	Start-up time	V_{DD} = 3.6 V, time from EN high until boost and amplifier are fully enabled		1.5		ms

7.7 Typical Characteristics

V_{DD} = 3.6 V, R_{EXT} = 7.5 kΩ, L = 4.7 µH, Differential Input

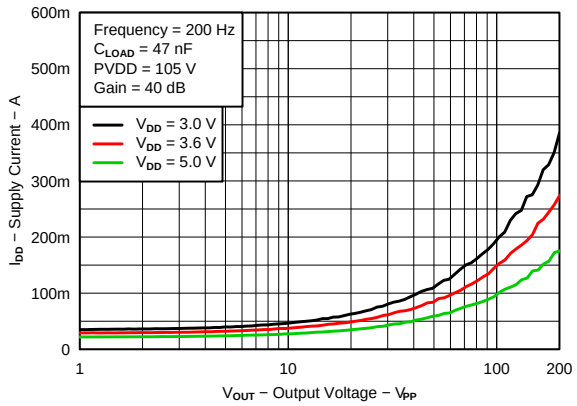


Figure 1. Supply Current vs Output Voltage

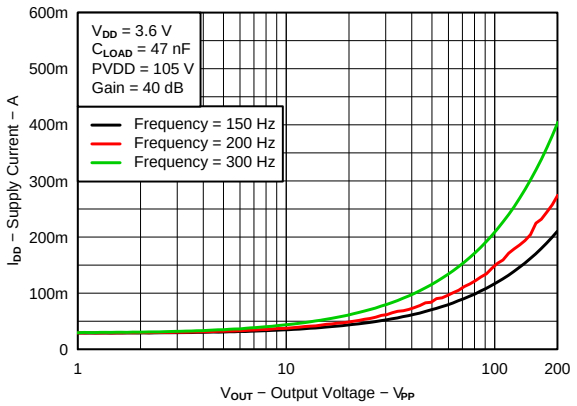


Figure 2. Supply Current vs Output Voltage

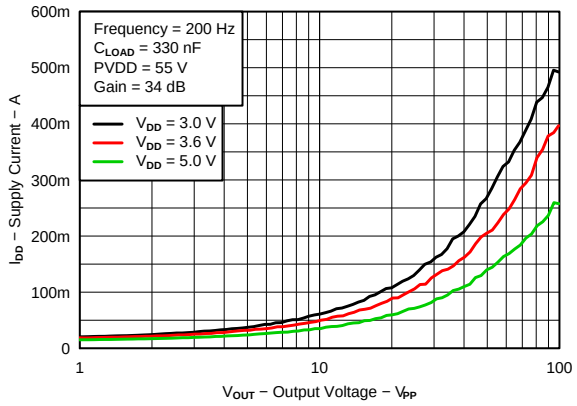


Figure 3. Supply Current vs Output Voltage

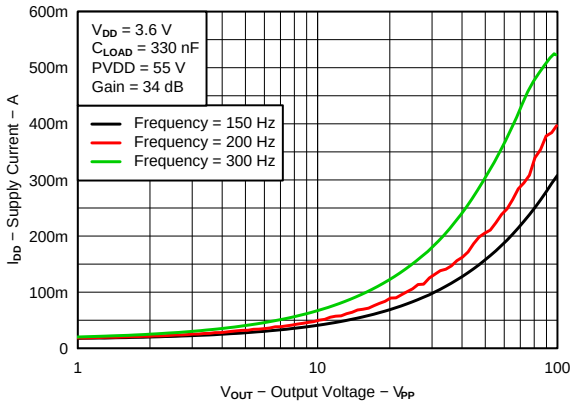


Figure 4. Supply Current vs Output Voltage

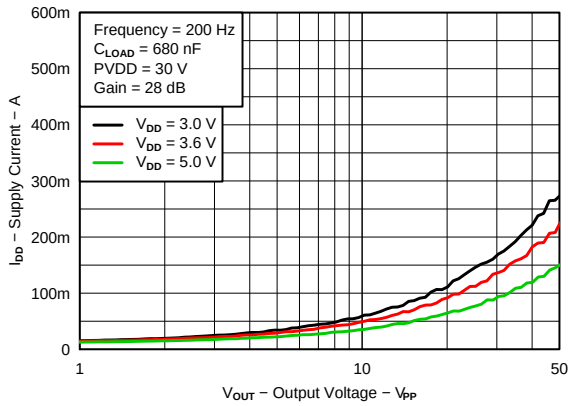


Figure 5. Supply Current vs Output Voltage

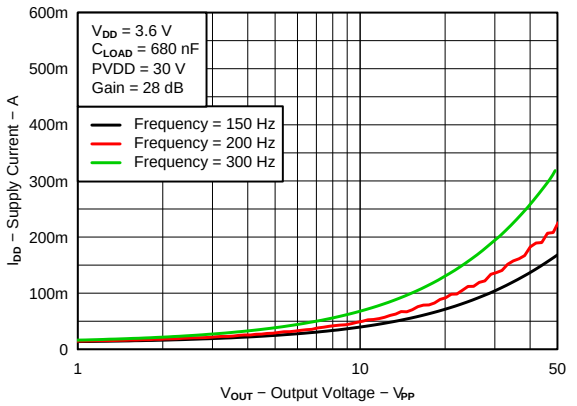


Figure 6. Supply Current vs Output Voltage

Typical Characteristics (continued)

V_{DD} = 3.6 V, R_{EXT} = 7.5 kΩ, L = 4.7 µH, Differential Input

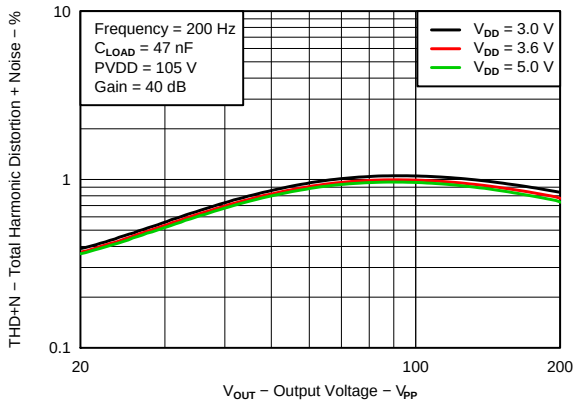


Figure 7. Total Harmonic Distortion + Noise vs Output Voltage

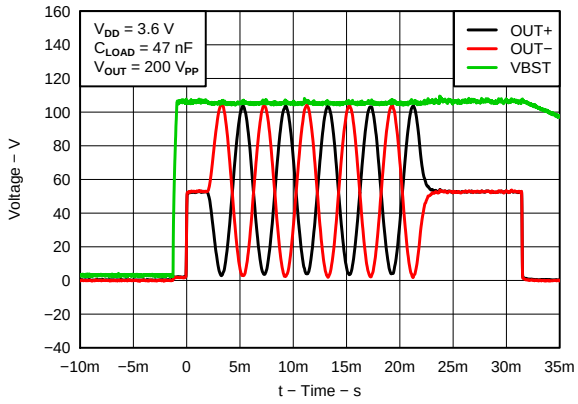


Figure 8. Typical Waveform

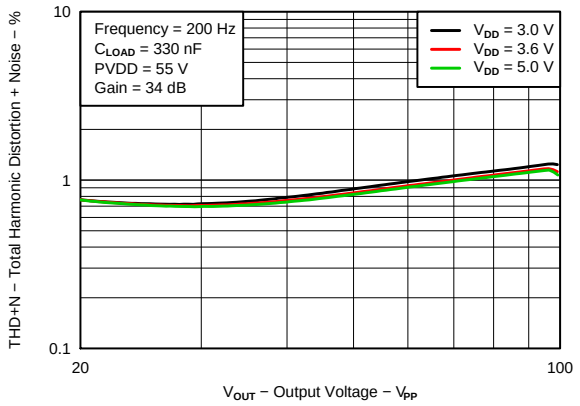


Figure 9. Total Harmonic Distortion + Noise vs Output Voltage

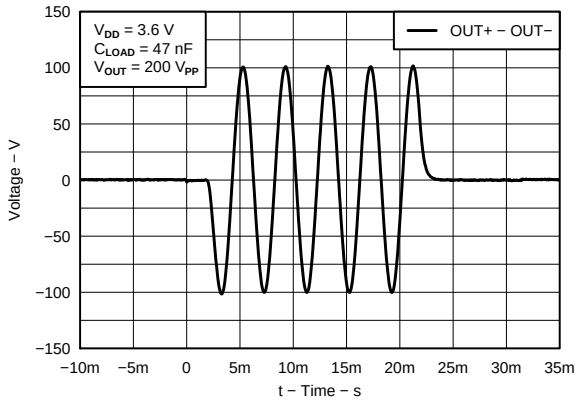


Figure 10. Typical Waveform - Differential

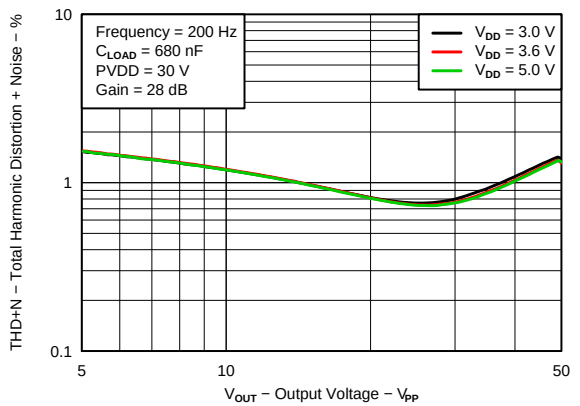


Figure 11. Total Harmonic Distortion + Noise vs Output Voltage

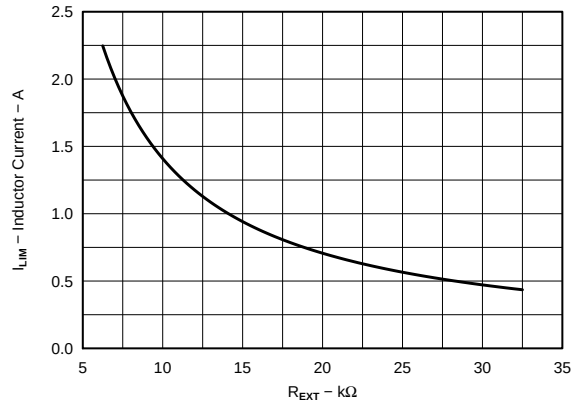


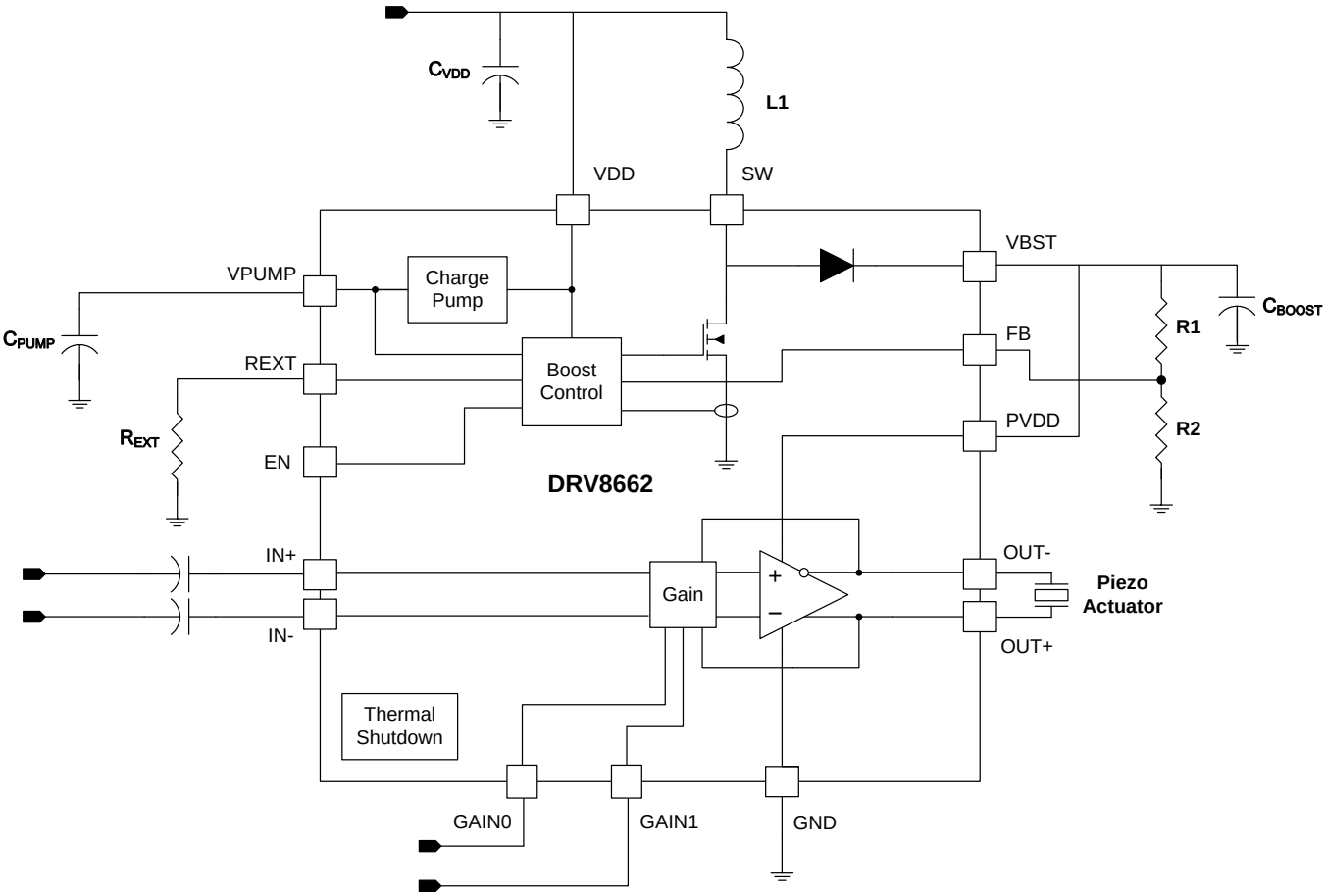
Figure 12. I_{LIM} vs R_{EXT}

8 Detailed Description

8.1 Overview

The DRV8662 accepts the typical battery range used in portable applications (3.0 V to 5.5 V) and creates a boosted supply rail with an integrated DC-DC converter. This boosted supply rail is fed to an internal, high-voltage, fully-differential amplifier that is capable of driving capacitive loads such as piezos with signals up to 200 V_{PP}. No transformer is required for boost operation. Only a single inductor is needed. The boost power FET and power diode are both integrated within the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fast Start-up (Enable Pin)

The DRV8662 features a fast startup time, which is essential for achieving low latency in haptic applications. When the EN pin transitions from low to high, the boost supply is turned on, the input capacitor is pre-charged, and the amplifier is enabled in a typical 1.5 ms total startup time. In the system application, the entire system latency should be kept to less than 30 ms total to be imperceptible to the end user. At 1.5 ms, the DRV8662 will be a small percentage of the total system latency.

8.3.2 Gain Control

The gain from IN+/IN– to OUT+/OUT– is given by the table below.

GAIN1	GAIN0	Gain (dB)
0	0	28.8
0	1	34.8
1	0	38.4
1	1	40.7

The gains are optimized to achieve approximately 50 V_{PP}, 100 V_{PP}, 150 V_{PP}, or 200 V_{PP} at the output without clipping from a 1.8 V peak single-ended input signal source.

8.3.3 Adjustable Boost Voltage

The output voltage of the integrated boost converter may be adjusted by a resistive feedback divider between the boost output voltage (VBST) and the feedback pin (FB). The boost voltage should be programmed to a value greater than the maximum peak signal voltage that the user expects to create with the DRV8662 amplifier. Lower boost voltages will achieve better system efficiency when lower amplitude signals are applied, so the user should take care not to use a higher boost voltage than necessary. The maximum allowed boost voltage is 105V.

8.3.4 Adjustable Boost Current Limit

The current limit of the boost switch may be adjusted via a resistor to ground placed on the REXT pin. The programmed current limit should be less than the rated saturation limit of the inductor selected by the user to avoid damage to both the inductor and the DRV8662. If the combination of the programmed limit and inductor saturation is not high enough, then the output current of the boost converter will not be high enough to regulate the boost output voltage under heavy load conditions. This will, in turn, cause the boosted rail to sag, possibly causing distortion of the output waveform.

8.3.5 Internal Charge Pump

The DRV8662 has an integrated charge pump to provide adequate gate drive for internal nodes. The output of this charge pump is placed on the VPUMP pin. An X5R or X7R storage capacitor of 0.1 µF with a voltage rating of 10 V or greater must be placed at this pin.

8.3.6 Thermal Shutdown

The DRV8662 contains an internal temperature sensor that will shut down both the boost converter and the amplifier when the temperature threshold is exceeded. When the die temperature falls below the threshold, the device will restart operation automatically as long as the EN pin is high. Continuous operation of the DRV8662 is not recommended. Most haptic use models only operate the DRV8662 in short bursts. The thermal shutdown function will protect the DRV8662 from damage when overdriven, but usage models which drive the DRV8662 into thermal shutdown should always be avoided.

8.4 Device Functional Modes

8.4.1 Startup/shutdown Sequencing

A simple startup sequence should be employed to maintain smooth haptic operation. If the sequence is not followed, unintended haptic events or sounds my occur. Use the following steps to play back each haptic waveform.

8.4.1.1 PWM Source

1. Send 50% duty cycle from the processor to the DRV8662 input filter. This is to allow the source and input filter to settle before the DRV8662 is fully enabled. At the same time (or on the next available processor cycle), transition the DRV8662 enable pin from logic low to logic high.
2. Wait 2 ms to ensure that the DRV8662 circuitry is fully enabled and settled.
3. Begin and complete playback of the haptic waveform. The haptic waveform PWM should end with a 50% duty cycle to bring the differential output back to 0 V.
4. Transition the DRV8662 enable pin from high to low and power down the PWM source.

8.4.1.2 DAC Source

1. Set the DAC to its mid-scale code. This is to allow the source and input capacitors to settle before the DRV8662 is fully enabled. At the same time (or on the next available processor cycle), transition the DRV8662 enable pin from logic low to logic high.
2. Wait 2 ms to ensure that the DRV8662 circuitry is fully enabled and settled.
3. Begin and complete playback of the haptic waveform. The haptic waveform should end with a mid-scale DAC code to bring the differential output back to 0 V.
4. Transition the DRV8662 enable pin from high to low and power down the DAC source.

8.4.2 Low-voltage Operation

The lowest gain setting is optimized for 50 V_{PP} with a boost voltage of 30 V. Some applications may not need 50 V_{PP}, so the user may elect to program the boost converter as low as 15 V to improve efficiency. When using boost voltages lower than 30 V, some special considerations are in order. First, to reduce boost ripple to an acceptable level, a 50 V rated, 0.22 µF boost capacitor is recommended. Second, the full-scale input range may need adjustment to avoid clipping. Normally, a 1.8 V, single-ended PWM signal will give 50 V_{PP} at the lowest gain. For example, if the boost voltage is set to 25 V for a 40 V_{PP} full-scale output signal, the full-scale input range drops to 1.44 V for single-ended PWM inputs. An input voltage divider may be desired in this case if a 1.8V I/O is used as a PWM source.

8.5 Programming

8.5.1 Programming the Boost Voltage

The boost output voltage (VBST) is programmed via two external resistors as shown in Figure 13.

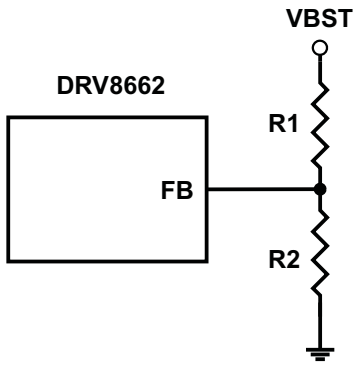


Figure 13. Boost Voltage Programming

The boost output voltage is given by Equation 1:

$$V_{BOOST} = V_{FB}\left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where V_{FB} = 1.32 V.

VBST should be programmed to a value 5.0 V greater than the largest peak voltage expected in the system to allow adequate amplifier headroom. Since the programming range for the boost voltage extends to 105 V, the leakage current through the resistor divider can become significant. It is recommended that the sum of the resistance of R1 and R2 be greater than 500 kΩ. Note that when resistor values greater than 1 MΩ are used, PCB contamination may cause boost voltage inaccuracy. Exercise caution when soldering large resistances, and clean the area when finished for best results.

8.5.2 Programing the Boost Current Limit

The peak current drawn from the supply through the inductor is set solely by the R_{EXT} resistor. Note that this peak current limit is independent of the inductance value chosen, but the inductor should be capable of handling this programmed limit. The relationship of R_{EXT} to I_{LIM} is approximated by Equation 2.

$$R_{EXT} = \left(K \frac{V_{REF}}{I_{LIM}}\right) - R_{INT} \quad (2)$$

where K = 10500, V_{REF} = 1.35 V, R_{INT} = 60 Ω, and I_{LIM} is the desired peak current limit through the inductor.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8662 is typically used in systems that require haptic feedback using high-voltage Piezo actuators. These systems typically contain an applications processor or microcontroller, which generates a haptic waveform. This section contains two examples of such systems and how to appropriately configure the input signal for the DRV8662.

9.2 Typical Application

9.2.1 DRV8662 System Diagram with DAC Input

In the following DRV8662 diagram, the DRV8662 is configured with a differential DAC input and a generic Piezo actuator. This is useful for systems that have an available DAC or analog signal generator.

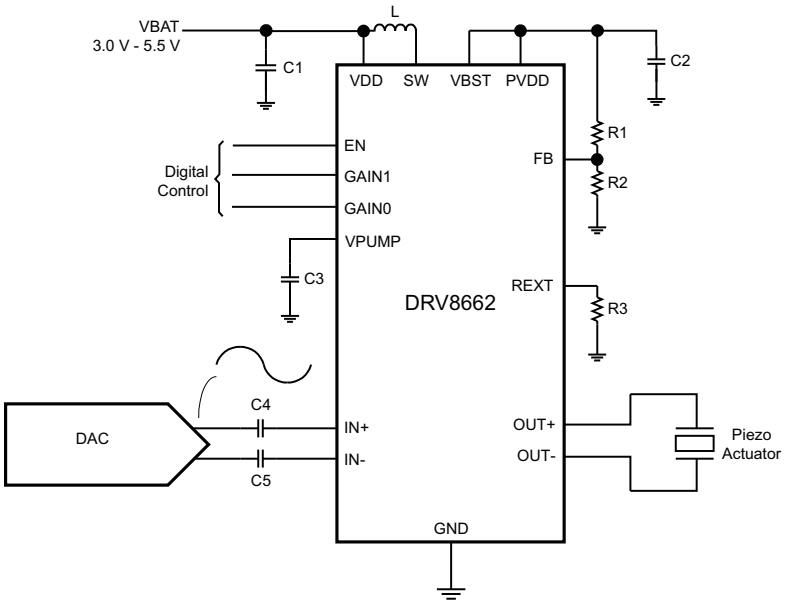


Figure 14. DRV8662 System Diagram with DAC Input

9.2.1.1 Design Requirements

For this example, use the parameters shown in Table 1.

Table 1. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.0V – 5.5V
Boost Converter	20-105V
Output Voltage	2 x Boost Converter (Vpp)
Differential Input Voltage (IN+, IN-)	1.8Vp Sine wave

Table 2 contains a list of components required for configuring the DRV8662. The components labeled “Standard” can be used “as-is”; and, the components labeled “Configure” require the designer to evaluate specific system requirements.

Table 2. List of Components

COMPONENT	DESCRIPTION	RECOMMENDED VALUE	UNIT	USE
CVDD	VDD bypass capacitor	0.1	µF	Standard
CPUMP	Voltage pump capacitor	0.1	µF	Standard
CIN+ / CIN-	IN+ / IN- AC coupling capacitors	1	µF	Standard
REXT	Boost current limit resistor	See *Programing the Boost Current Limit*	Ω	Configure
CPVDD	Boost converter output capacitor	See *Boost Capacitor Selection*	µF	Configure
L	Boost converter inductor	See *Inductor Selection*	µH	Configure
R1	Boost converter high-side feedback resistor	See *Programming the Boost Voltage*	Ω	Configure
R2	Boost converter low-side feedback resistor	See*Programming the Boost Voltage*	Ω	Configure

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

Inductor selection plays a critical role in the performance of the DRV8662. The range of recommended inductances is from 3.3 µH to 22 µH. In general, higher inductances within a given manufacturer’s inductor series have lower saturation current limits, and vice-versa. When a larger inductance is chosen, the DRV8662 boost converter will automatically run at a lower switching frequency and incur less switching losses; however, larger values of inductance may have higher equivalent series resistance (ESR), which will increase the parasitic inductor losses. Since lower values of inductance generally have higher saturation currents, they are a better choice when attempting to maximize the output current of the boost converter. The following table has sample inductors that provide adequate performance.

For inductor recommendations, see DRV8662EVM User's Guide (SLOU319)

9.2.1.2.2 Piezo Actuator Selection

There are several key specifications to consider when choosing a piezo actuator for haptics such as dimensions, blocking force, and displacement. However, the key electrical specifications from the driver perspective are voltage rating and capacitance. At the maximum frequency of 500 Hz, the DRV8662 is optimized to drive up to 50 nF at 200 V_{PP}, which is the highest voltage swing capability. It will drive larger capacitances if the programmed boost voltage is lowered and/or the user limits the input frequency range to lower frequencies (e.g. 300 Hz).

For piezo actuator recommendations, see the DRV8662EVM User's Guide (SLOU319).

9.2.1.2.3 Boost Capacitor Selection

The boost output voltage may be programmed as high as 105V. A capacitor with a voltage rating of at least the boost output voltage must be selected. Since ceramic capacitors tend to come in ratings of 100 V or 250 V, a 250 V rated 100 nF capacitor of the X5R or X7R type is recommended for the 105 V case. The selected capacitor should have a minimum working capacitance of at least 50 nF.

9.2.1.2.4 Current Consumption Calculation

It is useful to understand how the voltage driven onto a piezo actuator relates to the current consumption from the power supply. Modeling a piezo element as a pure capacitor is reasonably accurate. The equation for the current through a capacitor for an applied sinusoid is given by Equation 3:

$$I_{Capacitor(Peak)} = 2\pi \times f \times C \times V_P \quad (3)$$

where f is the frequency of the sinusoid in Hz, C is the capacitance of the piezo load in farads, and V_P is the peak voltage. At the power supply (usually a battery), the actuator current is multiplied by the boost-supply ratio and divided by the efficiency of the boost converter as shown by Equation 4.

$$I_{BAT(Peak)} = 2\pi \times f \times C \times V_P \times \frac{V_{Boost}}{V_{BAT} \times \mu_{Boost}} \quad (4)$$

Substituting typical values for the variables of this equation yields a typical peak current seen by the battery with a sine input as in Equation 5.

$$I_{BAT(Peak)} = 2\pi \times 300\ Hz \times 50\ nF \times 100 \times \frac{105}{3.6 \times 0.7} = 392\ mA \quad (5)$$

9.2.1.2.5 Input Filter Considerations

Depending on the quality of the source signal provided to the DRV8662, an input filter may be required. Some key factors to consider are whether the source is generated from a DAC or from PWM and the out-of-band content generated. If proper anti-image rejection filtering is used to eliminate image components, the filter can possibly be eliminated depending on the magnitude of the out-of-band components. If PWM is used, at least a 1st order RC filter is required. The PWM sample rate should be greater than 30 kHz to keep the PWM ripple from reaching the piezo element and dissipating unnecessary power. A 2nd order RC filter may be desirable to further eliminate out-of-band signal content to further drive down power dissipation and eliminate audible noise.

9.2.1.3 Application Curves

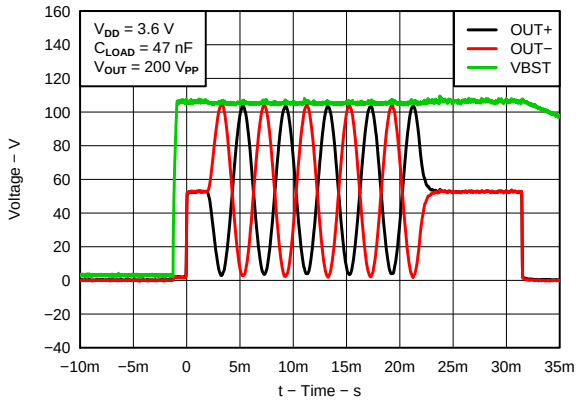


Figure 15. Typical Waveform

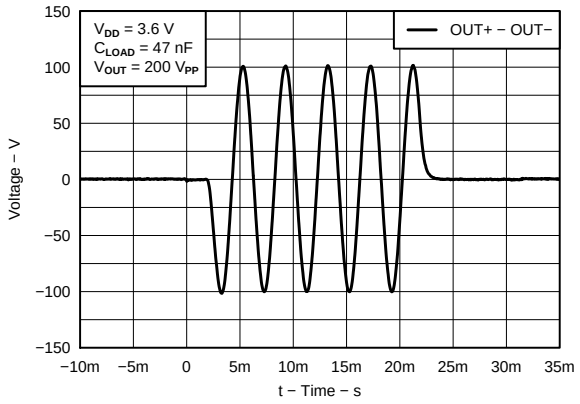


Figure 16. Typical Waveform – Differential

9.2.2 DRV8662 System Diagram with Filtered Single-Ended PWM Input

The DRV8662 can be used with a PWM input signal for systems that do not have an available DAC or analog output. Most piezo actuator systems require a PWM input filter to remove any unwanted noise.

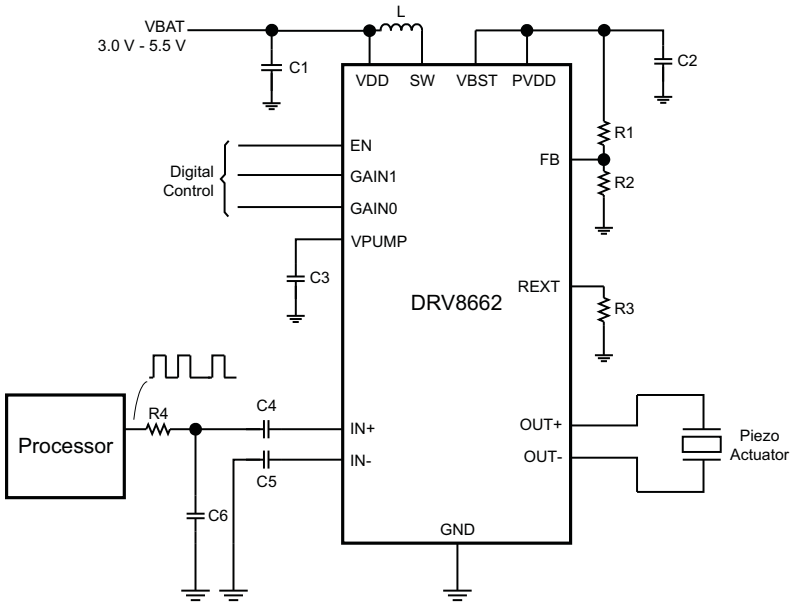


Figure 17. DRV8662 System Diagram with Filtered Single-Ended PWM Input

9.2.2.1 Design Requirements

For this example, use the parameters shown in Table 3.

Table 3. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.0V – 5.5V
Boost Converter	20-105V
Output Voltage	2 x Boost Converter (Vpp)
Differential Input Voltage (IN+, IN-)	1.8Vp PWM

Table 4 contains a list of components required for configuring the DRV8662. The components labeled “Standard” can be used “as-is”; and, the components labeled “Configure” require the designer to evaluate specific system requirements.

Table 4. List of Components

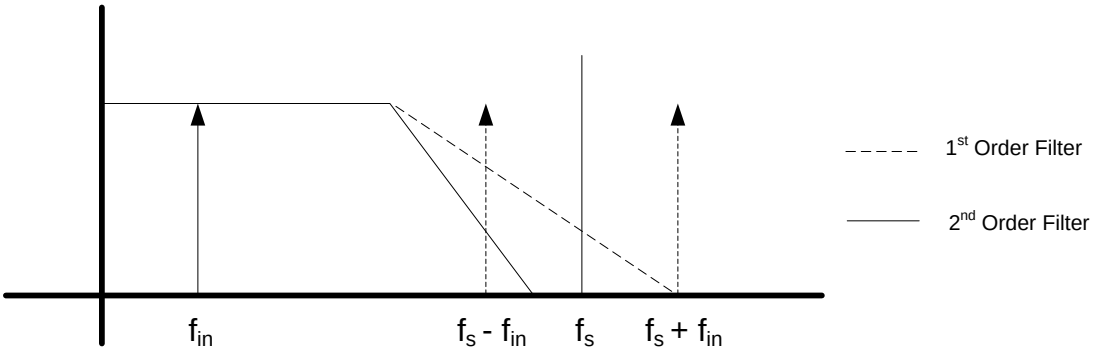
COMPONENT	DESCRIPTION	RECOMMENDED VALUE	UNIT	USE
CVDD	VDD bypass capacitor	0.1	µF	Standard
CPUMP	Voltage pump capacitor	0.1	µF	Standard
CIN+ / CIN-	IN+ / IN- AC coupling capacitors	1	µF	Standard
REXT	Boost current limit resistor	See *Programing the Boost Current Limit*	Ω	Configure
CPVDD	Boost converter output capacitor	See *Boost Capacitor Selection*	µF	Configure
L	Boost converter inductor	See *Inductor Selection*	µH	Configure
R1	Boost converter high-side feedback resistor	See *Programming the Boost Voltage*	Ω	Configure
R2	Boost converter low-side feedback resistor	See*Programming the Boost Voltage*	Ω	Configure

9.2.2.2 Detailed Design Procedure

Use the following section for designing the DRV8662 input filter. See the *DRV8662 System with DAC Input Detailed Design Procedure* for the remaining design.

9.2.2.2.1 Input Filter Design

When using a PWM input, a low-pass filter is required. The primary parameters for determining the input filter are the PWM input frequency and sample rate. Because haptic waveforms are typically less than 500Hz, the input filter must attenuate frequencies above 500 Hz. For samples rates above 20 kHz, a simple first-order RC filter is recommended; however, for sample rates much lower (such as 8 kHz), a first-order filter may not sufficiently attenuate the high-frequency content. Thus, for lower sampling rates, a second-order RC filter may be required. The *DRV8662EVM User's Guide* contains example filter configurations for both first-order and second-order filters. The DRV8662EVM default configuration uses a second-order, differential filter, but it can be replaced by a first-order, single-ended or differential filter.



Apply these criteria to select an input filter:

1. First-order RC filters, both single-ended and differential, are recommended for 20 kHz and higher data sample rates. The first-order filters have adequate settling time and the fewest components.
2. Second-order filters are recommended for noiseless operation when using a lower data sample rate where a sharper cutoff is necessary.
3. The attenuation at the PWM carrier frequency should be at least –40 dB for haptic applications.

9.2.2.3 Application Curves

See *DRV8662 System with DAC Input Application Curves*.

10 Power Supply Recommendations

The recommended voltage supply range for the DRV8662 is 2.3V to 5.5V. For proper operation, place a 0.1µF low equivalent series resistance (ESR) supply-bypass capacitor of X5R or X7R type near the VDD pin with a voltage rating of at least 10V.

The internal charge pump requires a 0.1µF capacitor of X5R or X7R type with a voltage rating of 10V or greater be placed between the VPUMP pin and GND for proper operation and stability. Do not use the charge pump as a voltage source for any other devices.

11 Layout

11.1 Layout Guidelines

- To achieve optimum device performance, use of the thermal footprint outlined by this datasheet is recommended. See land pattern diagram for exact dimensions. The DRV8662 power pad must be soldered directly to the thermal pad on the printed circuit board. The printed circuit board thermal pad should be connected to the ground net with thermal vias to any existing backside/internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended.
- Another key layout consideration is to keep the boost programming resistors (R1 and R2) as close as possible to the FB pin of the DRV8662. Care should be taken to avoid getting the FB trace near the SW trace.

11.2 Layout Example

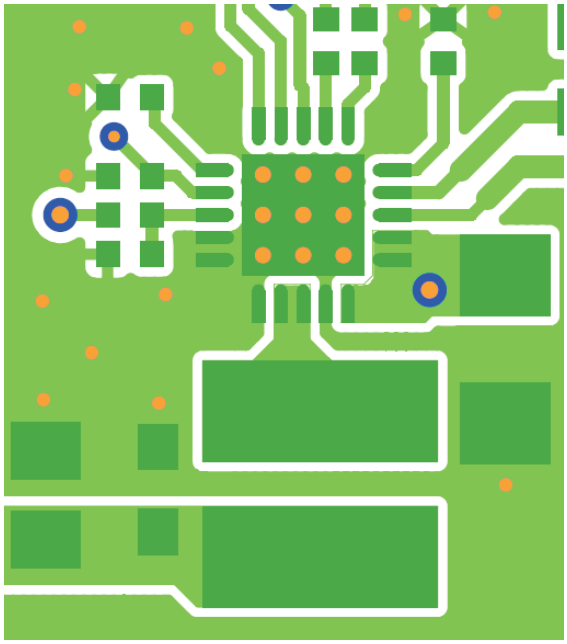


Figure 18. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

DRV8662EVM User's Guide (SLOU319)

DRV8662 Configuration Guide (SLOA198)

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8662RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	8662	Samples
DRV8662RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	8662	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

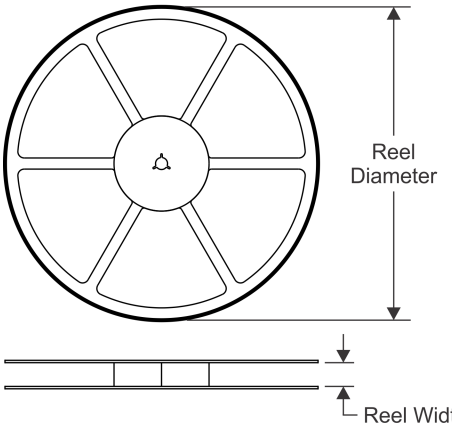
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

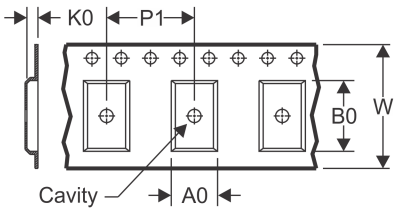
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

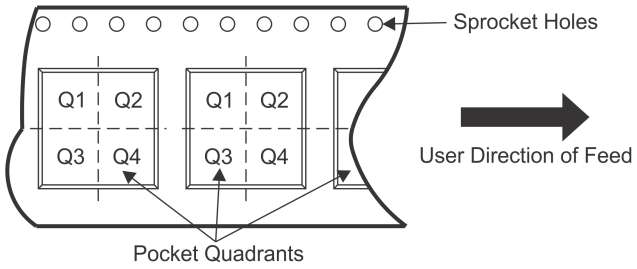


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

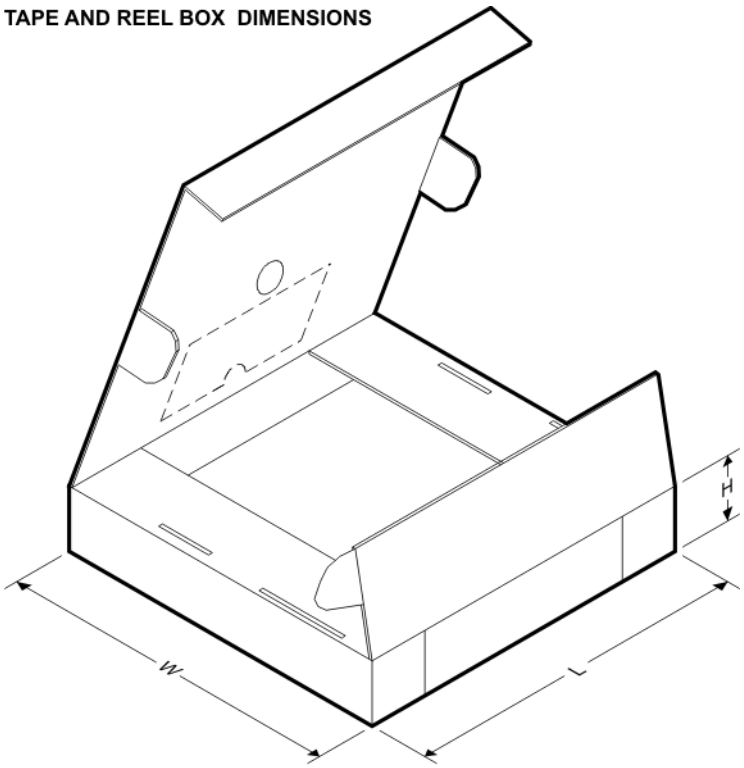
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8662RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8662RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

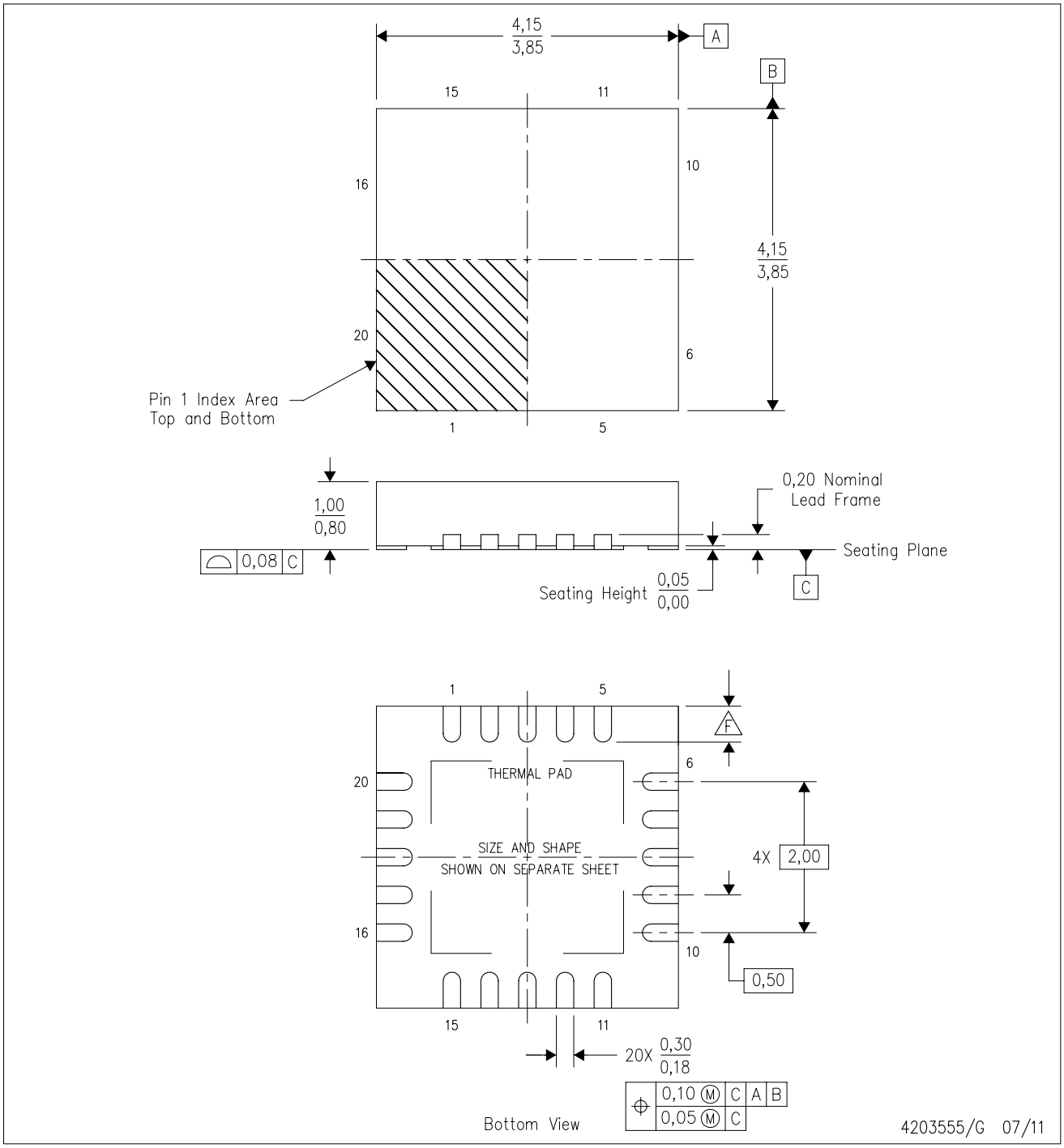
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8662RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
DRV8662RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

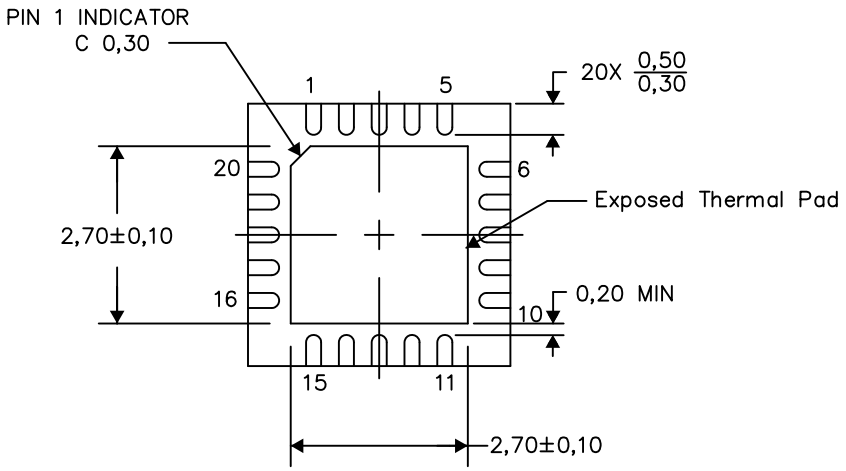
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



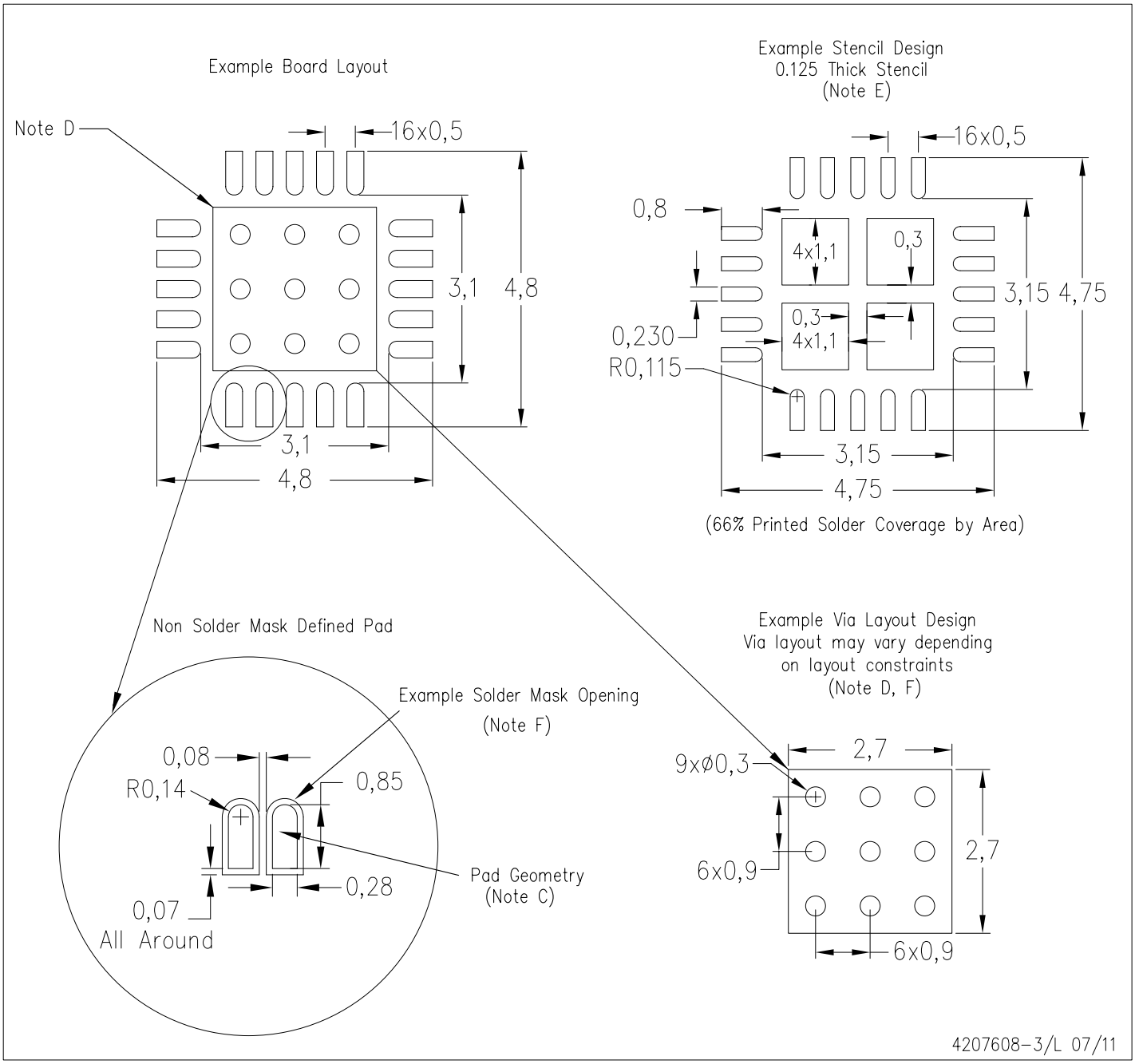
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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