DRV8813 Dual-Bridge Motor Controller IC

1 Features

- 8.2-V to 45-V Operating Supply Voltage Range
- 2.5-A Maximum Drive Current at 24 V and T_A = 25°C
- Dual H-Bridge Current Control Motor Driver
  - Drive a Bipolar Stepper or Two DC Motors
  - Four Level Winding Current Control
- Multiple Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Industry Standard Parallel Digital Control Interface
- Low Current Sleep Mode
- Built In 3.3-V Reference Output
- Small Package and Footprint
- Protection Features
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8813 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, and can drive a bipolar stepper motor or two DC motors. The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings. The DRV8813 can supply up to 2.5-A peak or 1.75-A RMS output current (with proper heatsinking at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout and overtemperature.

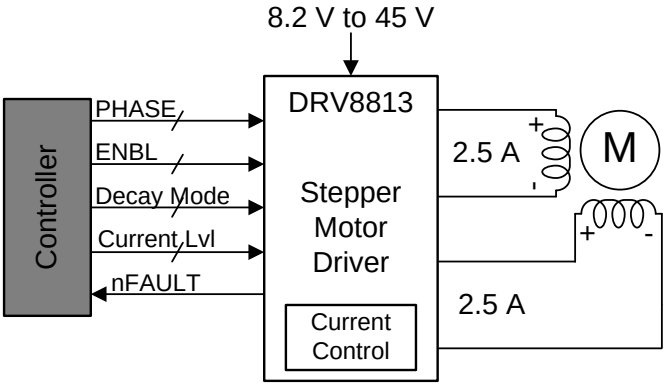
The DRV8813 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8813	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

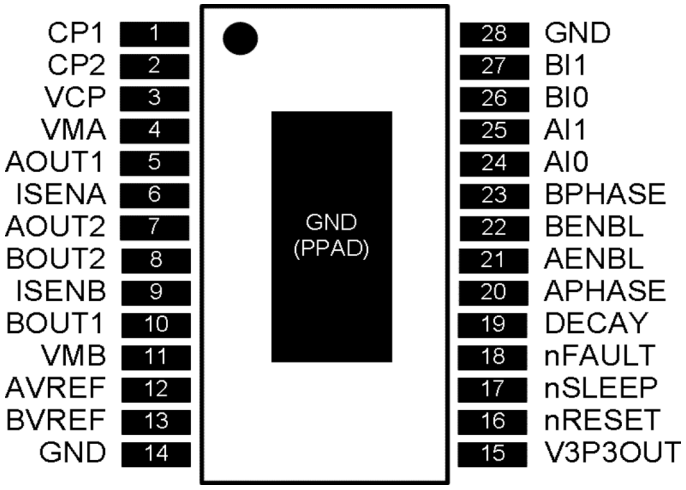
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2013) to Revision E **Page**

- Updated *Features* section ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed External Components text for VMA and VMB rows. ... 3
- Changed MAX value for VMx row in *Absolute Maximum Ratings*. ... 4
- Added Power supply ramp rate row to *Absolute Maximum Ratings* ... 4
- Changed MIN value for ISENSEx pin voltage paramter from –0.3 to –0.8 ... 4
- Changed MIN value for Continuous motor drive output current paramter from –2.5 to 0 ... 4

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF, 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
GND	14, 28	—	Device ground	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF, 16-V ceramic capacitor and a 1-MΩ resistor to VM.
VMA	4	—	Bridge A power supply	Connect to motor supply (8.2 V to 45 V). Both pins must be connected to the same supply, bypassed with a 0.1 uF capacitor to GND, and connected to appropriate bulk capacitance.
VMB	11	—	Bridge B power supply	
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CONTROL				
AENBL	21	I	Bridge A enable	Logic high to enable bridge A. Internal pulldown.
APHASE	20	I	Bridge A phase (direction)	Logic high sets AOUT1 high, AOUT2 low. Internal pulldown.
AI0	24	I	Bridge A current set	Sets bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0 Internal pulldown.
AI1	25	I		
AVREF	12	I	Bridge A current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (for example, V3P3OUT).
BENBL	22	I	Bridge B enable	Logic high to enable bridge B. Internal pulldown.
BI0	26	I	Bridge B current set	Sets bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0 Internal pulldown.
BI1	27	I		
BPHASE	23	I	Bridge B phase (direction)	Logic high sets BOUT1 high, BOUT2 low. Internal pulldown.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
BVREF	13	I	Bridge B current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (for example, V3P3OUT).
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay. Internal pulldown and pullup.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT				
AOUT1	5	O	Bridge A output 1	Connect to motor winding A
AOUT2	7	O	Bridge A output 2	
BOUT1	10	O	Bridge B output 1	Connect to motor winding B
BOUT2	8	O	Bridge B output 2	
ISENA	6	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	9	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
VMx	Power supply voltage	–0.3	50	V
	Power supply ramp rate		1	V/µs
	Digital pin voltage	–0.5	7	V
VREF	Input voltage	–0.3	4	V
	ISENSEx pin voltage(3)	–0.8	0.8	V
	Peak motor drive output current, t < 1 µS	Internally limited		A
	Continuous motor drive output current(4)	0	2.5	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Transients of ±1V for less than 25 ns are acceptable
(4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage(1)	8.2		45	V
V_{REF}	VREF input voltage(2)	1		3.5	V
I_{V3P3}	V3P3OUT load current	0		1	mA
f_{PWM}	Externally applied PWM frequency	0		100	kHZ

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at VREF from 0 V to 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8813 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.2	3.3	3.4	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2.2		5.25	V
V_{HYS}	Input hysteresis		0.3	0.45	0.6	V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode	0		0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_{IN}	Input current				±40	µA
R_{PU}	Internal pullup resistance (to 3.3 V)			130		kΩ
R_{PD}	Internal pulldown resistance			80		kΩ

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.2		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.25	0.32	
	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.2		
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.25	0.32	
I_{OFF}	Off-state leakage current		–20		20	µA
MOTOR DRIVER						
f_{PWM}	Internal current control PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		µs
t_R	Rise time		30		200	ns
t_F	Fall time		30		200	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		3			A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	µA
V_{TRIP}	xISENSE trip voltage	xVREF = 3.3 V, 100% current setting	635	660	685	mV
		xVREF = 3.3 V, 71% current setting	445	469	492	
		xVREF = 3.3 V, 38% current setting	225	251	276	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics

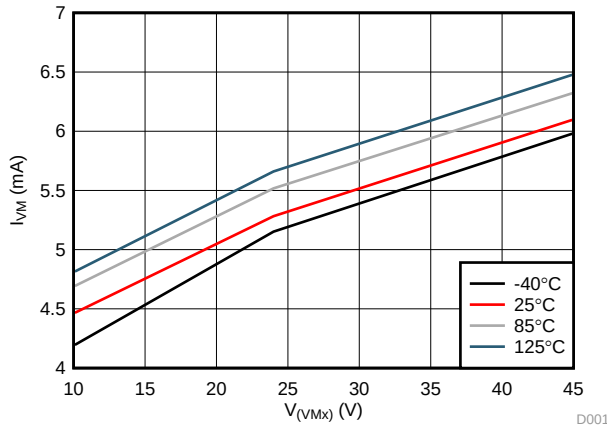


Figure 1. I_{VMx} vs $V_{(VMx)}$

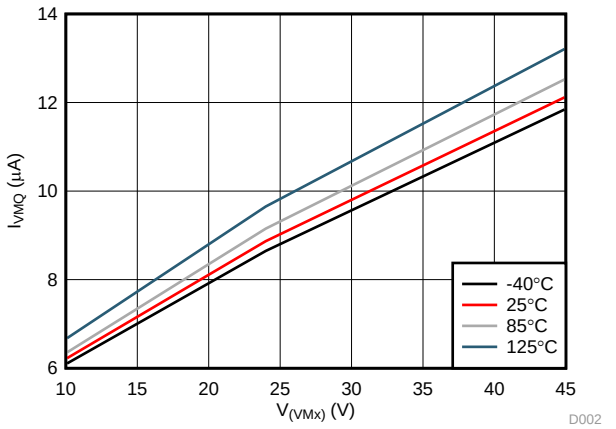


Figure 2. I_{VMxQ} vs $V_{(VMx)}$

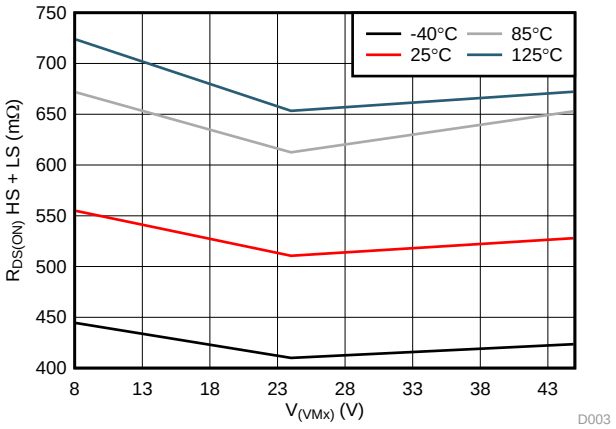


Figure 3. $R_{DS(ON)}$ vs $V_{(VMx)}$

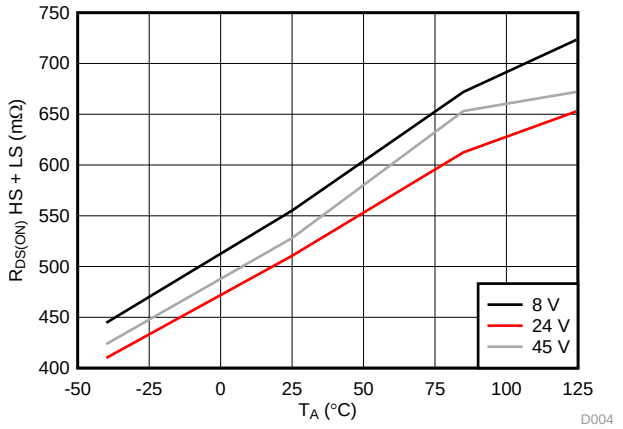


Figure 4. $R_{DS(ON)}$ vs Temperature

7 Detailed Description

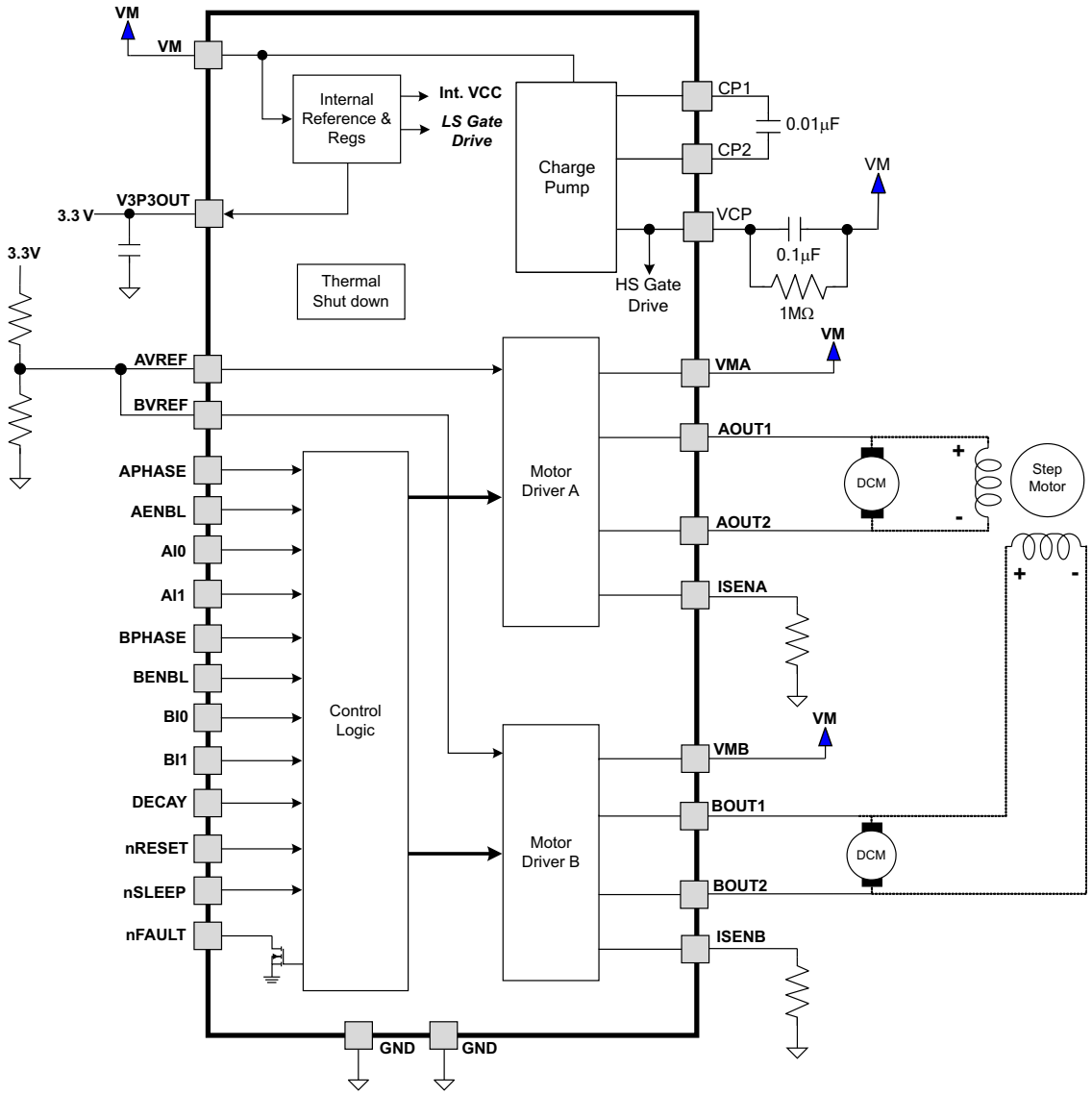
7.1 Overview

The DRV8813 is an integrated motor driver solution for a bipolar stepper motor or two brushed DC motors. The device integrates two NMOS H-bridges, current sense, regulation circuitry, and detailed fault detection. The DRV8813 can be powered with a supply voltage from 8.2 V to 45 V, and is capable of providing an output current up to 2.5 A full-scale.

A PHASE/ENBL interface allows for simple interfacing to the controller circuit. The winding current control allows the external controller to adjust the regulated current that is provided to the motor. The current regulation is highly configurable, with three decay modes of operation. Fast, slow, and mixed decay can be selected depending on the application requirements.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8813 contains two H-bridge motor drivers with current-control PWM circuitry. Figure 5 shows a block diagram of the motor control circuitry. A bipolar stepper motor is shown, but the drivers can also drive two separate DC motors.

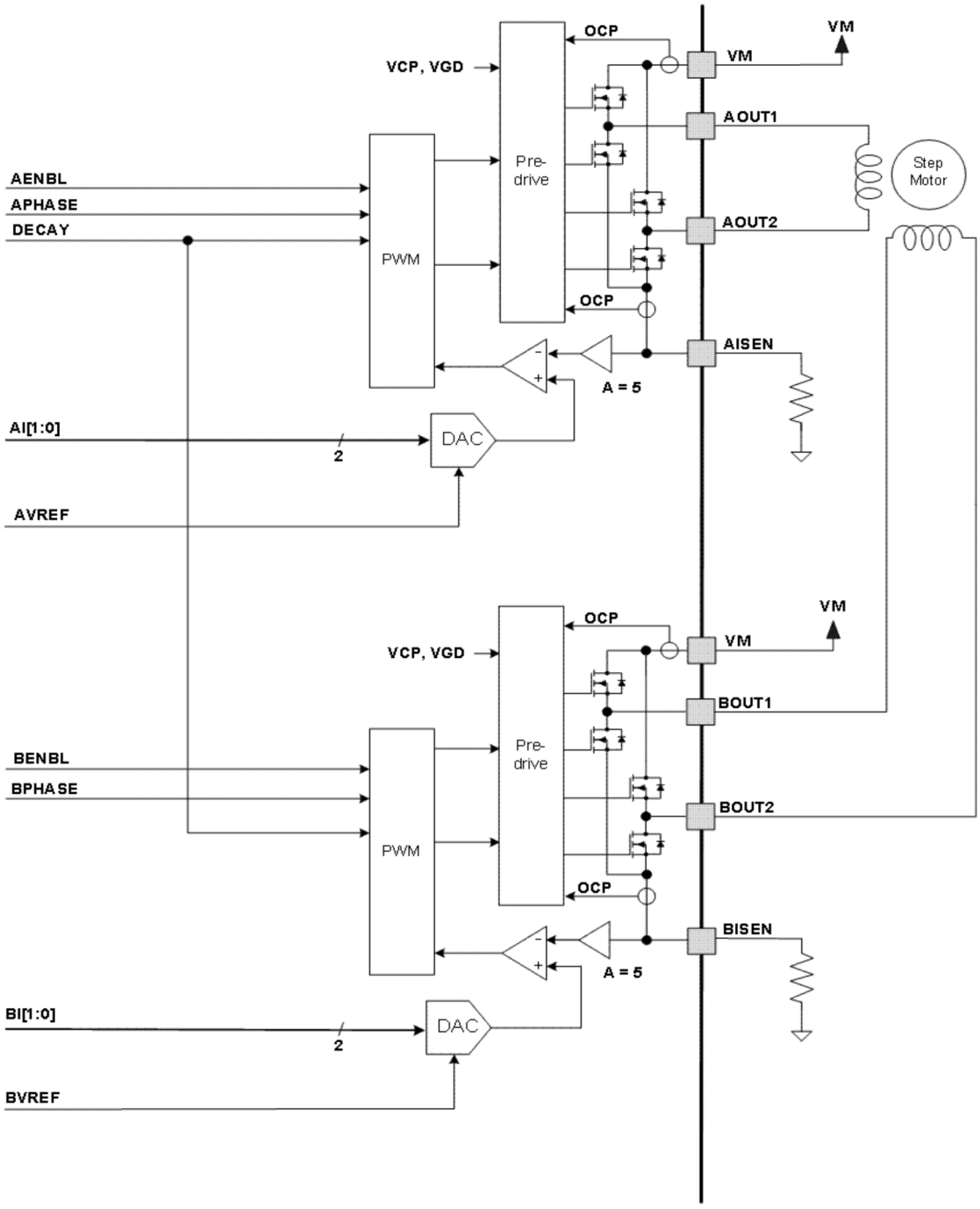


Figure 5. Motor Control Circuitry

There are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

Feature Description (continued)

7.3.2 Protection Circuits

The DRV8813 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge disables and the nFAULT pin drives low. The device remains disabled until either nRESET pin is applied, or VM is removed and reapplied.

Overcurrent conditions on both high and low side devices; that is, a short to ground, supply, or across the motor winding results in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge disables and the nFAULT pin drives low. Once the die temperature has fallen to a safe level, operation automatically resumes.

7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic resets. Operation resumes when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Bridge Control

The xPHASE input pins control the direction of current flow through each H-bridge. The xENBL input pins enable the H-bridge outputs when active high. Table 1 shows the logic.

Table 1. H-Bridge Logic

xENBL	xPHASE	xOUT1	xOUT2
0	X	Z	Z
1	1	H	L
1	0	L	H

The control inputs have internal pulldown resistors of approximately 100 kΩ.

7.4.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

If the current regulation feature is not needed, it can be disabled by connecting the xISENSE pins directly to ground and connecting the xVREF pins to V3P3.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 100%, 71%, 38% of full-scale, plus zero.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current is 2.5 V / (5 × 0.25 Ω) = 2 A.

Two input pins per H-bridge (xI1 and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The xI0 and xI1 pins have internal pulldown resistors of approximately 100 kΩ. The function of the pins is shown in Table 2.

Table 2. H-Bridge Pin Functions

xI1	xI0	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
1	1	0% (Bridge disabled)
1	0	38%
0	1	71%
0	0	100%

When both xI bits are 1, the H-bridge is disabled and no current flows.

Example:

If a 0.25-Ω sense resistor is used and the VREF pin is 2.5 V, the chopping current is 2 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current is 2 A × 0.71 = 1.42 A, and at the 38% setting (xI1, xI0 = 10) the current is 2 A × 0.38 = 0.76 A. If (xI1, xI0 = 11) the bridge disables and no current flows.

7.4.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 6 as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6 as case 3.

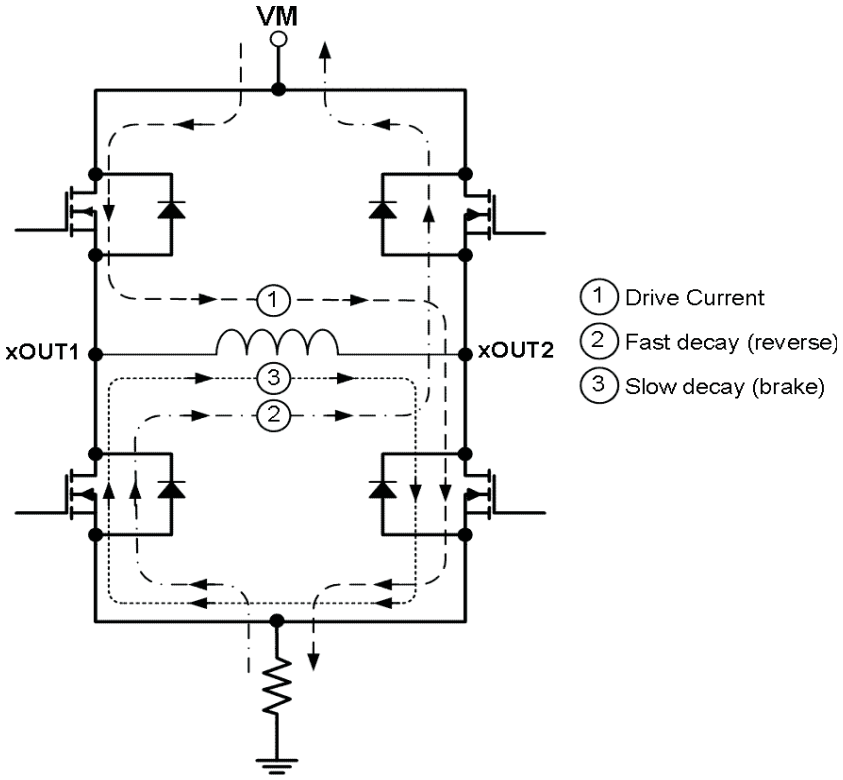


Figure 6. Decay Mode

The DRV8813 supports fast decay, slow decay, and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven. The DECAY pin sets the decay mode for both H-bridges.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

7.4.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. The blanking time also sets the minimum on time of the PWM.

7.4.5 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low puts the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state, all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) must to pass before the motor driver becomes fully operational. The nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals must be driven to logic high for device operation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8813 can be used to control a bipolar stepper motor. The PHASE/ENBL interface controls the outputs and current control can be implemented with the internal current regulation circuitry. Detailed fault reporting is provided with the internal protection circuits and nFAULT pin.

8.2 Typical Application

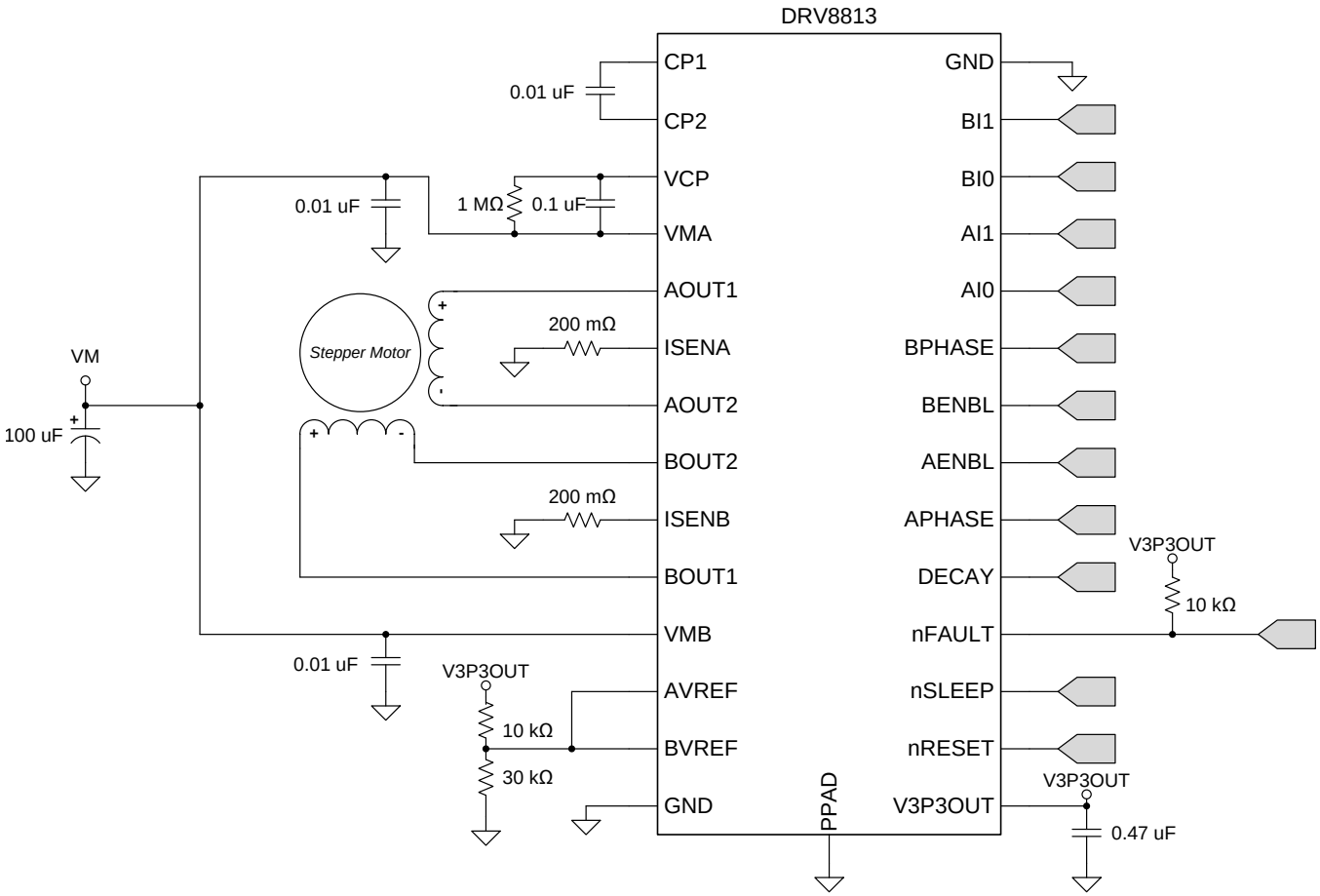


Figure 7. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 3 shows the design parameters for this application.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24 V
Motor Winding Resistance	R_L	3.9 Ω
Motor Winding Inductance	I_L	2.9 mH
Sense Resistor Value	R_{SENSE}	200 mΩ
Target Full-Scale Current	I_{FS}	1.25 A

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8813 is set for 5 V/V.

$$I_{FS}(A) = \frac{xVREF(V)}{A_V \times R_{SENSE}(\Omega)} = \frac{xVREF(V)}{5 \times R_{SENSE}(\Omega)} \quad (2)$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω, xVREF should be 1.25 V.

8.2.2.2 Decay Modes

The DRV8813 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8813 places the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

8.2.2.3 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $Irms^2 \times R$. For example, if the rms motor current is 2-A and a 100-mΩ sense resistor is used, the resistor dissipates 2 $A^2 \times 0.1\ \Omega$ = 0.4 W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curves

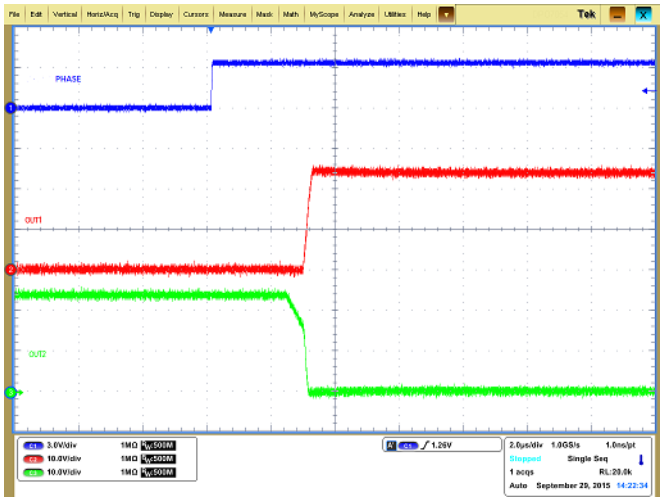


Figure 8. Direction Change

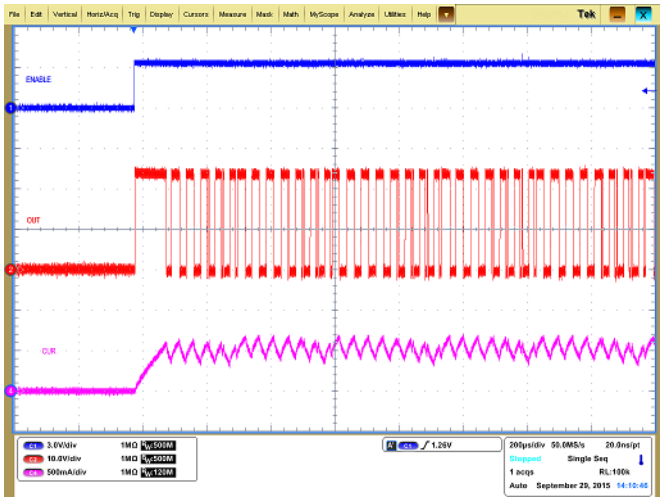


Figure 9. Current Limiting

9 Power Supply Recommendations

The DRV8813 is designed to operate from an input voltage supply (VMx) range from 8.2 V to 45 V. Two 0.1-µF ceramic capacitors rated for VMx must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor start-up current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. You should size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

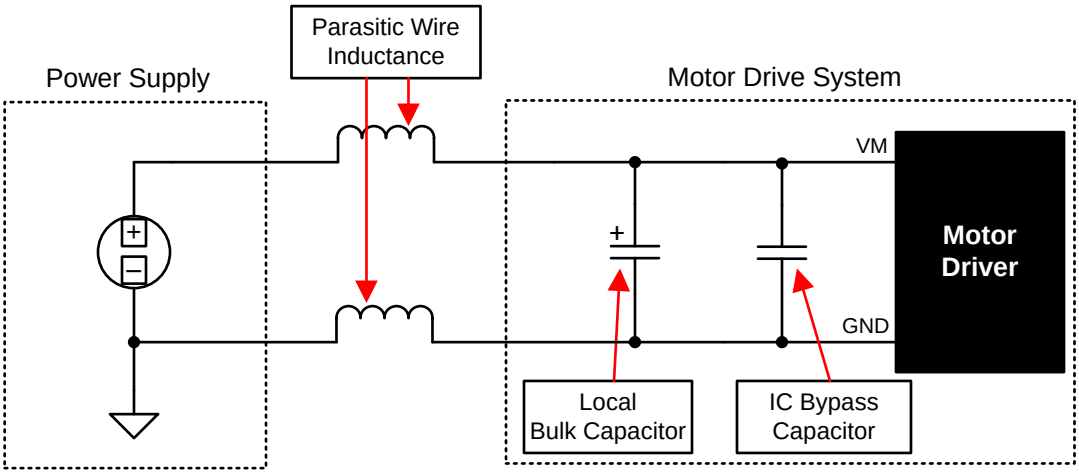


Figure 10. Setup of Motor Drive System With External Power Supply

9.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8813. It is okay for digital input signals to be present before VMx is applied. After VMx is applied to the DRV8813, it begins operation based on the status of the control pins.

10 Layout

10.1 Layout Guidelines

- The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VMx. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.
- The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8813.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.01-µF rated for VMx. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1-µF rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-MΩ resistor between VCP and VMA.
- Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

10.2 Layout Example

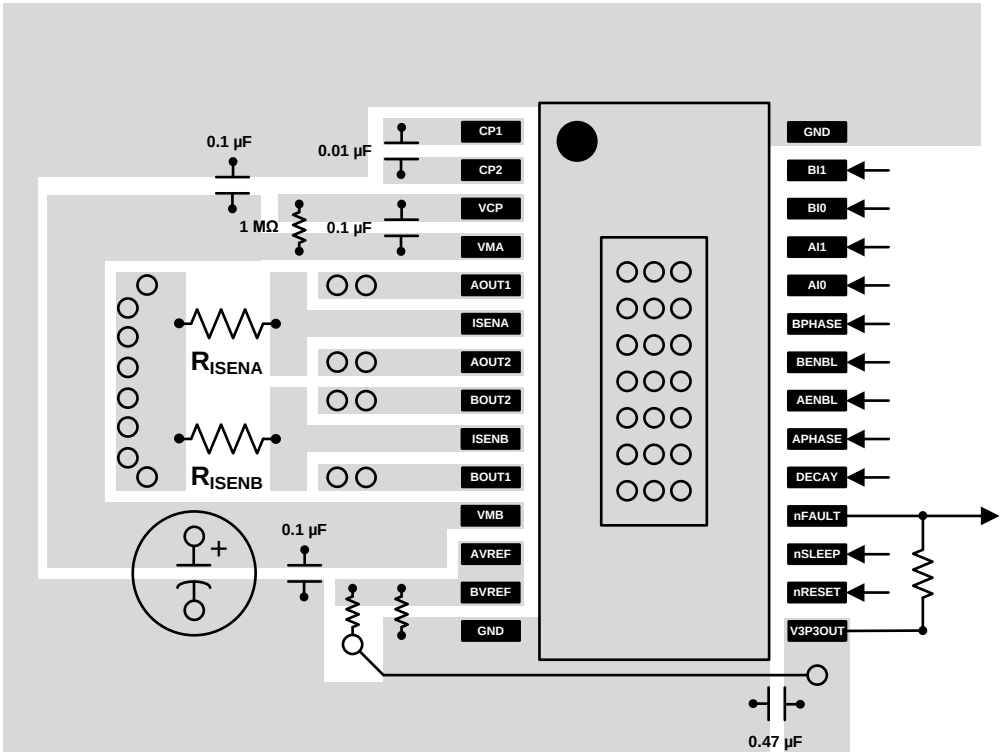


Figure 11. DRV8813 Layout Example

10.3 Thermal Considerations

10.3.1 Thermal Protection

The DRV8813 has thermal shutdown (TSD) as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Thermal Considerations (continued)

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multilayer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI application report*PowerPAD™ Thermally Enhanced Package* SLMA002, and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

10.4 Power Dissipation

Power dissipation in the DRV8813 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 3.

$$P_{TOT} = 4 \times R_{DS(ON)} \times \left(I_{OUT(RMS)}\right)^2 \quad (3)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding.
- $I_{OUT(RMS)}$ is equal to the approximately 0.7× the full-scale output current setting.

The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*, SLMA002.
- *PowerPAD™ Made Easy*, SLMA004.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8813PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8813	Samples
DRV8813PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8813	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

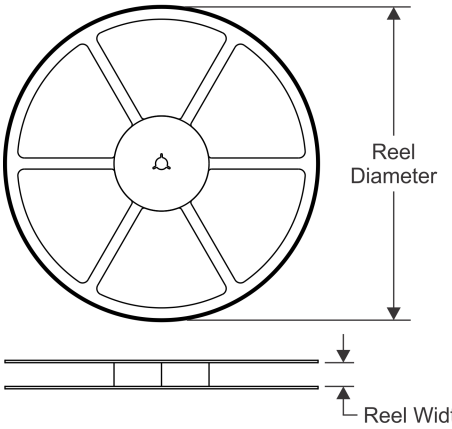
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

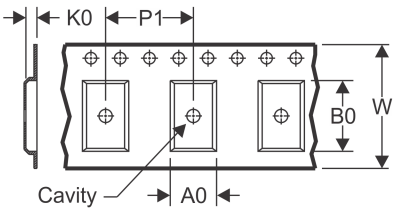
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

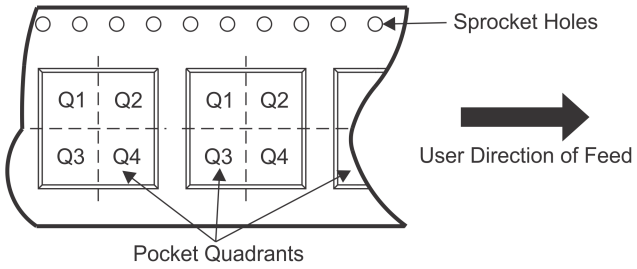


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

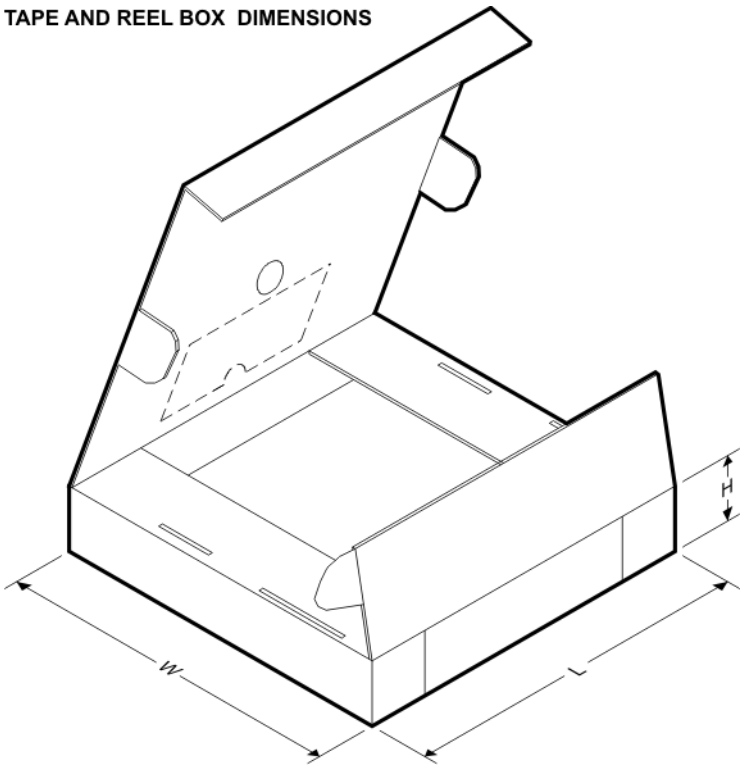
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8813PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

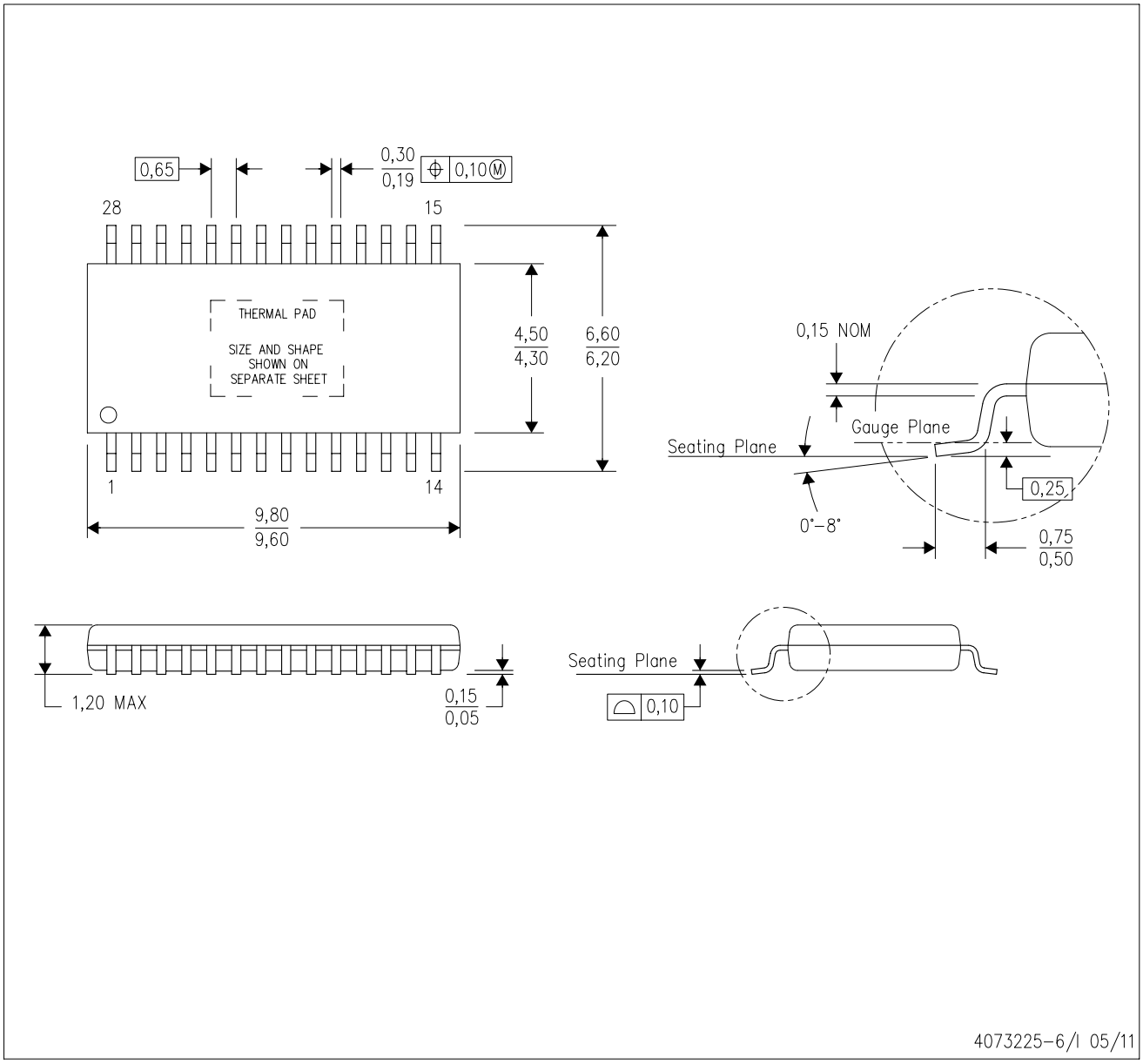
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8813PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

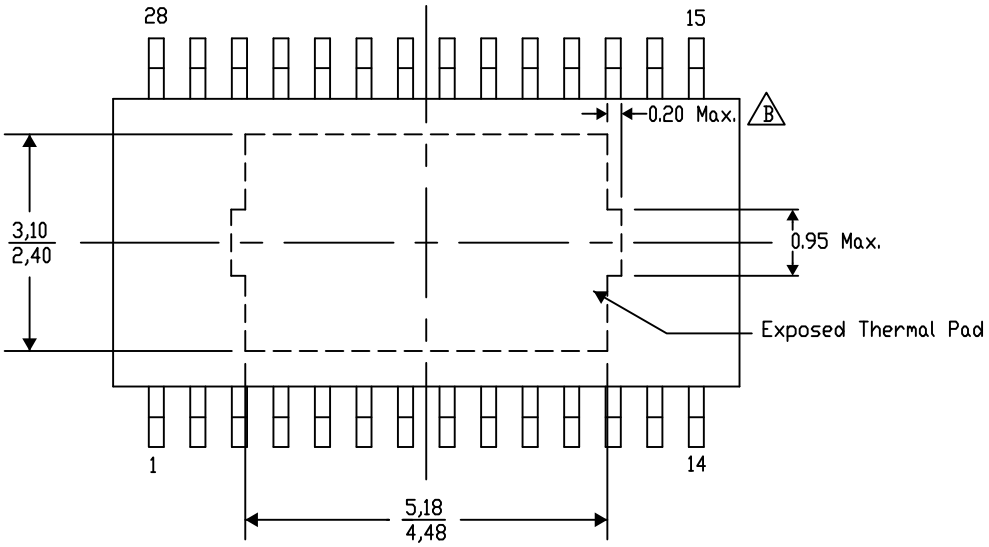
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

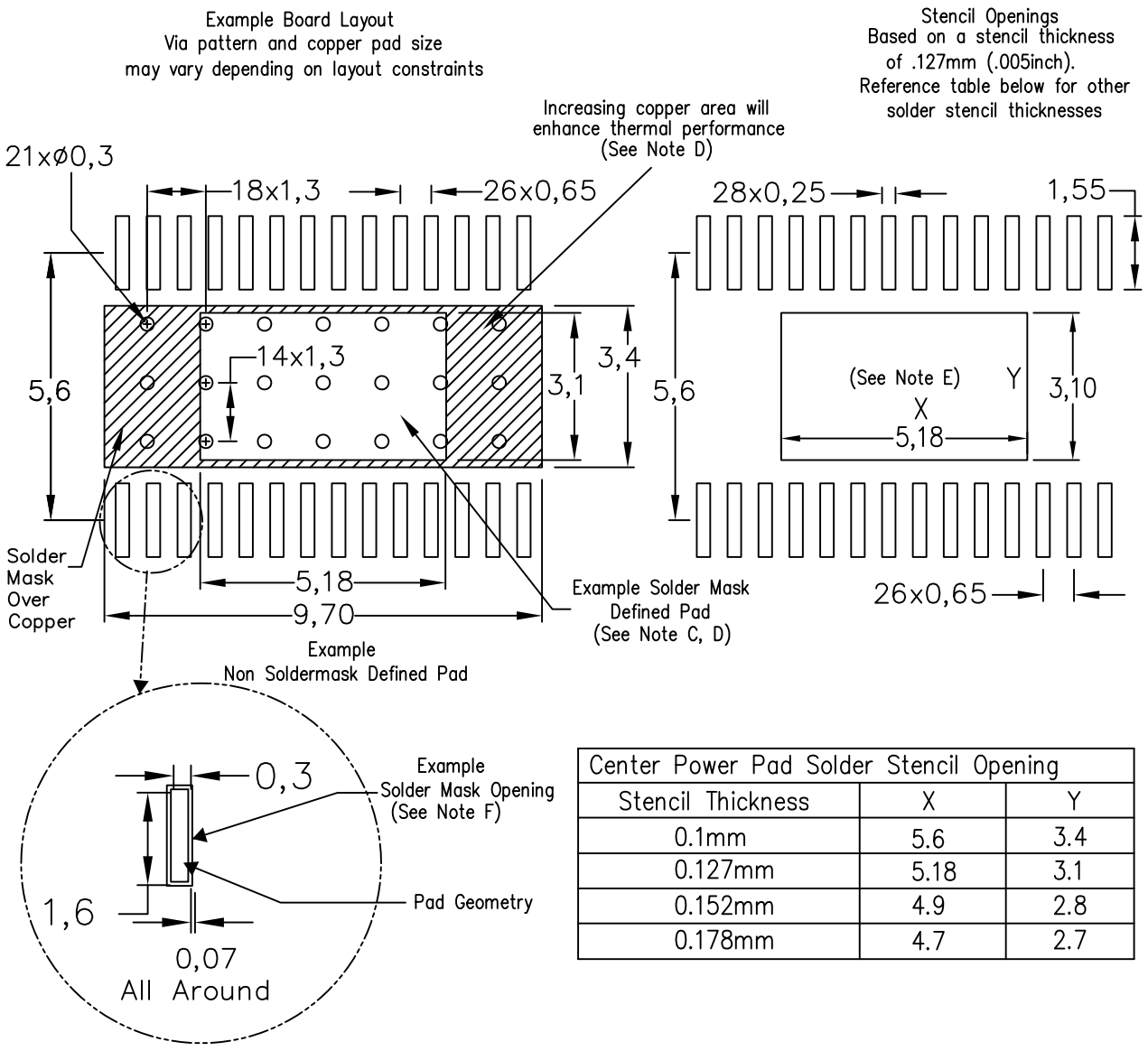
4206332–38/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	3.4
0.127mm	5.18	3.1
0.152mm	4.9	2.8
0.178mm	4.7	2.7

4207609–22/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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