DS34C87T CMOS Quad TRI-STATE Differential Line Driver

Check for Samples: DS34C87T

FEATURES

- **TTL Input Compatible**
- **Typical Propagation Delays: 6 ns**
- **Typical Output Skew: 0.5 ns**
- **Outputs Won't Load Line When V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **Operation from Single 5V Supply**
- **TRI-STATE Outputs for Connection to System Buses**
- **Low Quiescent Current**
- **Available in Surface Mount**

DESCRIPTION

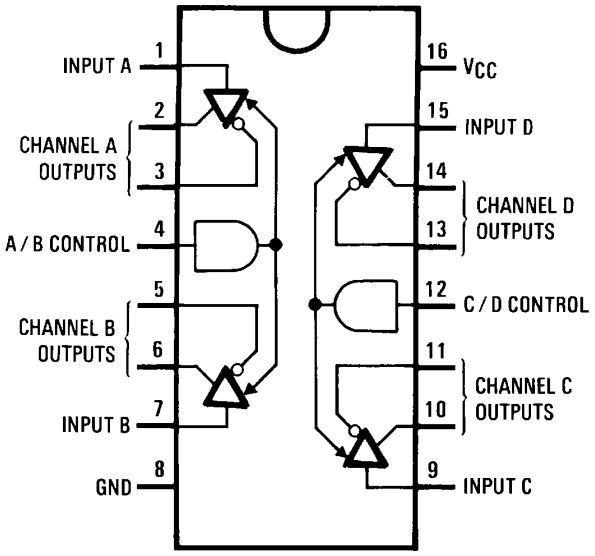
The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Connection and Logic Diagrams

Top View



See PIN DESCRIPTIONS for details.

Figure 1. PDIP Package
See Package Numbers D0016A or NFG0016E

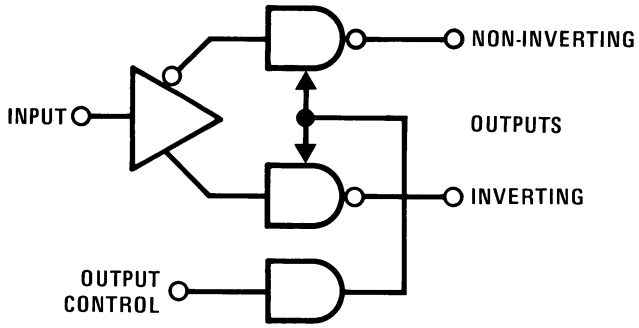


Figure 2. Logic Diagram

Truth Table(1)

Input	Control	Non-Inverting	Inverting
	Input	Output	Output
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high performance)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK} , I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C(5)	
PDIP Package	1736 mW
SOIC Package	1226 mW
Lead Temperature (T_L)	
(Soldering 4 sec)	260°C
This device does not meet 2000V ESD rating.(6)	

(1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.
(2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provide conditions for actual device operation.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥ 1500V Outputs ≥ 1000V EIAJ (0Ω, 200 pF) All Pins ≥ 350V
(4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(5) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG0016E Package 13.89 mW/°C, and D0016A Package 9.80 mW/°C.
(6) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥ 1500V Outputs ≥ 1000V EIAJ (0Ω, 200 pF) All Pins ≥ 350V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A) DS34C87T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics[1]

V_{CC} = 5V ±10% (unless otherwise specified)

Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = -20$ mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 48$ mA			0.3	0.5	V
V_T	Differential Output Voltage	$R_L = 100\ \Omega$ See[2]		2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	$R_L = 100\ \Omega$ See[2]				0.4	V
V_{OS}	Common Mode Output Voltage	$R_L = 100\ \Omega$ See[2]			2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	$R_L = 100\ \Omega$ See[2]				0.4	V
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}				±1.0	µA
I_{CC}	Quiescent Supply Current	$I_{OUT} = 0$ µA,					
		$V_{IN} = V_{CC}$ or GND			200	500	µA
		$V_{IN} = 2.4V$ or $0.5V$[3]			0.8	2.0	mA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Control = V_{IL}			±0.5	±5.0	µA
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND See[2] and [4]		−30		−150	mA
I_{OFF}	Power Off Output Leakage Current	$V_{CC} = 0V$ See[2]	$V_{OUT} = 6V$			100	µA
			$V_{OUT} = -0.25V$			−100	µA

(1) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) See EIA Specification RS-422 for exact test conditions.
(3) Measured per input. All other inputs at V_{CC} or GND.
(4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics[1]

V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (Figure 3, Figure 4, Figure 5, Figure 6)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		6	11	ns
Skew	See[2]	S1 Open		0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time[3]	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time[3]	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance[4]			100		pF
C_{IN}	Input Capacitance			6		pF

(1) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
(4) C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V^2CC f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

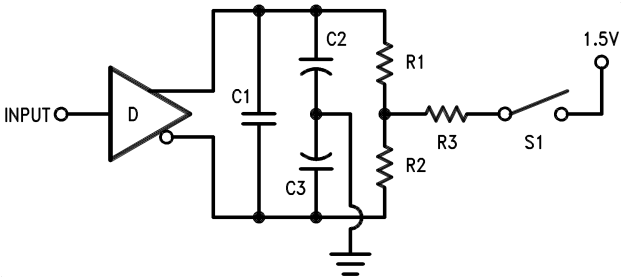
Comparison Table of Switching Characteristics into “LS-Type” Load[1]

V_{CC} = 5V, T_A = +25°C, t_r ≤ 6 ns, t_f ≤ 6 ns (Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11)

Parameter		Test Conditions	DS34C87		DS3487		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output		6	10	10	15	ns
Skew	See[2]		1.5	2.0			ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times		4	7	10	15	ns
t_{PHZ}	Output Disable Time See[3]	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	8	11	17	25	ns
t_{PLZ}	Output Disable Time See[3]	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	7	10	15	25	ns
t_{PZH}	Output Enable Time	C_L = 50 pF, R_L = ∞, S1 Open, S2 Closed	11	19	11	25	ns
t_{PZL}	Output Enable Time	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Open	14	21	15	25	ns

(1) This table is provided for comparison purposes only. The values in this table for the DS34C87 reflect the performance of the device but are not tested or ensured.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

Figure 3. AC Test Circuit

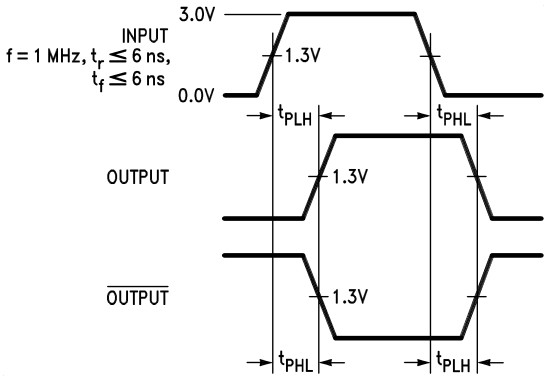
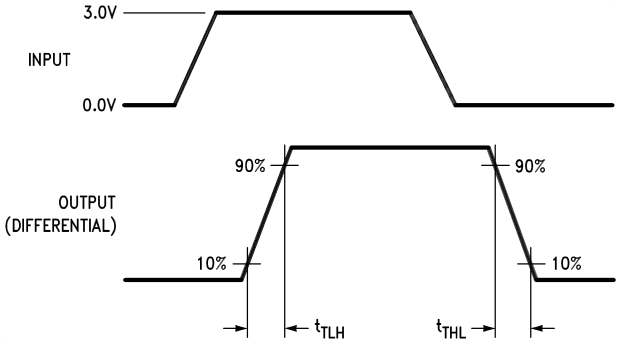


Figure 4. Propagation Delays



Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq$ 6ns

Figure 6. Differential Rise and Fall Times

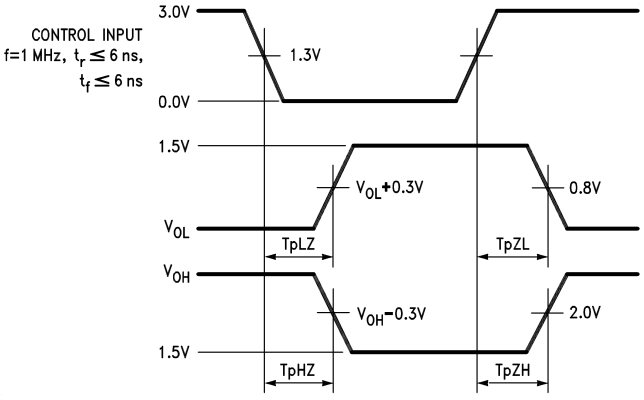


Figure 5. Enable and Disable Times

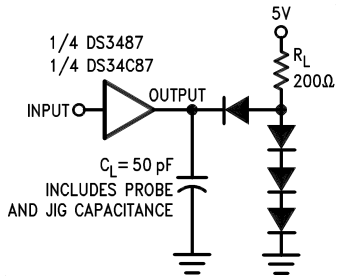


Figure 7. Propagation Delays Test Circuit for "LS-Type" Load

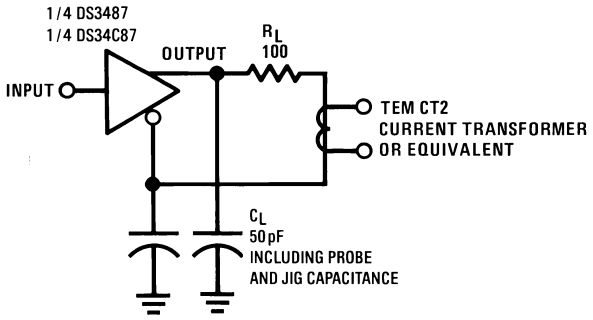


Figure 8. Differential Rise and Fall Times Test Circuit for "LS-Type" Load

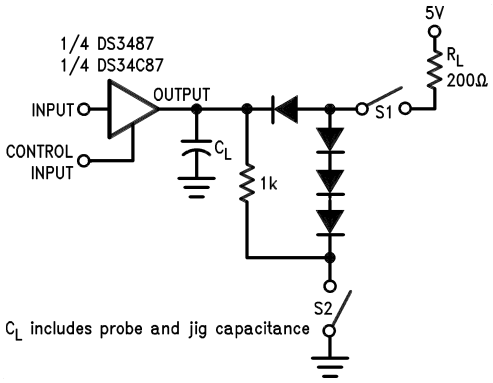


Figure 9. Load Enable and Disable Times Test Circuit for "LS-Type" Load

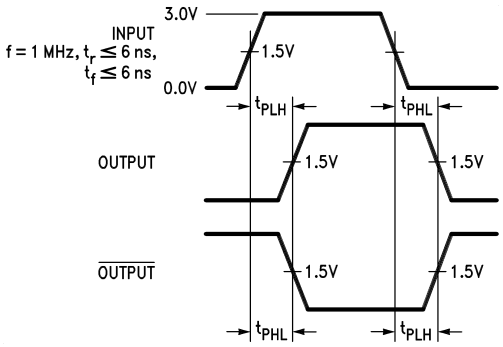


Figure 10. Load Propagation Delays for "LS-Type" Load

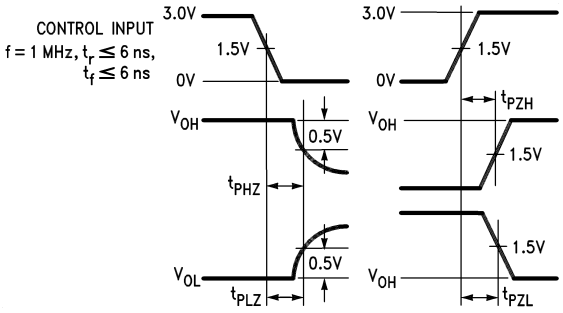
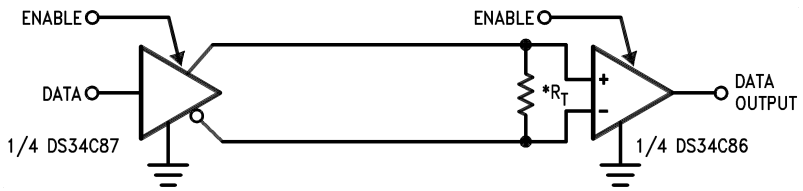


Figure 11. Load Enable and Disable Times for "LS-Type" Load

TYPICAL APPLICATIONS



*R_T is optional although highly recommended to reduce reflection.

PIN DESCRIPTIONS

Pin Number (PDIP or SOIC package)	**Pin Name**	**Function**
1	INPUT A	Channel A - TTL/CMOS input
2	OUTPUT A - True	True Output for Channel A, RS422 Levels
3	OUTPUT A - Inverting	Inverting Output for Channel A, RS422 Levels
4	A/B CONTROL	Enable Pin for Channels A and B, Active High, TTL/CMOS Levels
5	OUTPUT B - Inverting	Inverting Output for Channel B, RS422 Levels
6	OUTPUT B - True	True Output for Channel B, RS422 Levels
7	INPUT B	Channel B - TTL/CMOS input
8	GND	Ground Pin (0 V)
9	INPUT C	Channel C - TTL/CMOS input
10	OUTPUT C - True	True Output for Channel C, RS422 Levels
11	OUTPUT C - Inverting	Inverting Output for Channel C, RS422 Levels
12	C/D CONTROL	Enable Pin for Channels C and D, Active High, TTL/CMOS Levels
13	OUTPUT D - Inverting	Inverting Output for Channel D, RS422 Levels
14	OUTPUT D - True	True Output for Channel D, RS422 Levels
15	INPUT D	Channel D - TTL/CMOS input
16	V_{CC}	Power Supply Pin, 5.0V typical

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34C87TM	LIFEBUY	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS34C87TM	
DS34C87TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-260C-UNLIM	-40 to 85	DS34C87TM	Samples
DS34C87TMX	LIFEBUY	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS34C87TM	
DS34C87TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34C87TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

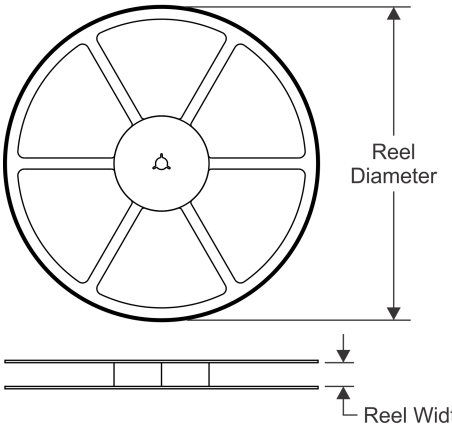
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

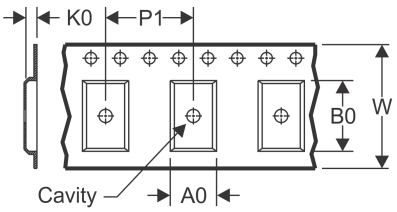
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

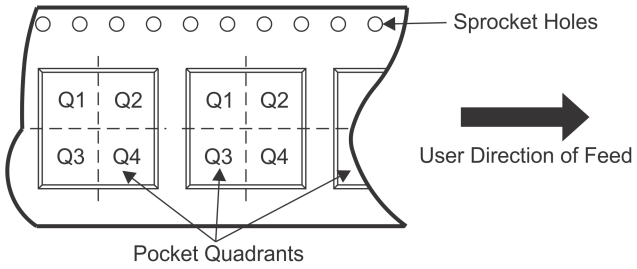


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

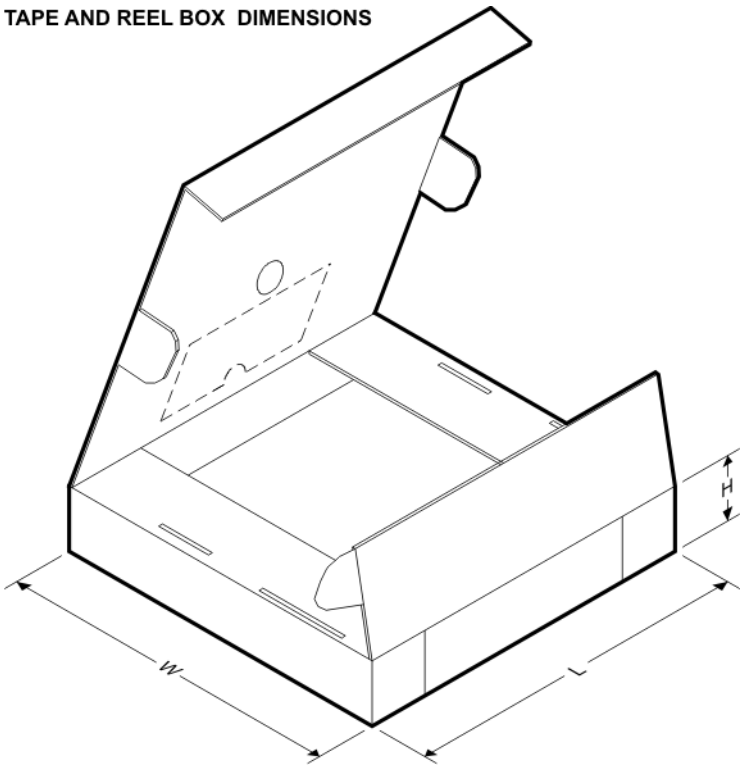
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34C87TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS34C87TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

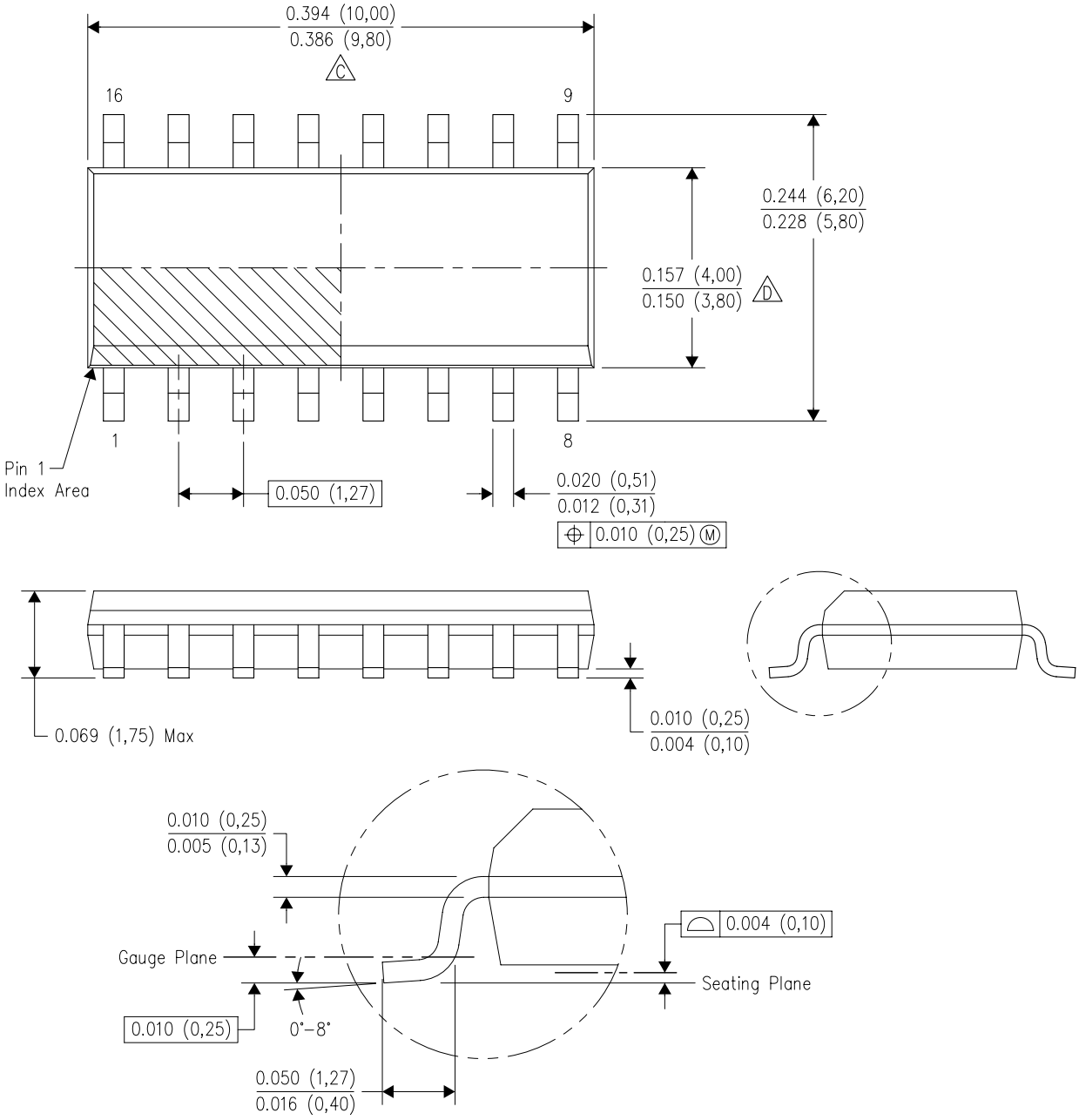
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34C87TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS34C87TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265