DS90LV110T 1 to 10 LVDS Data/Clock Distributor

Check for Samples: DS90LV110T

FEATURES

- **Low jitter 800 Mbps fully differential data path**
- **145 ps (typ) of pk-pk jitter with PRBS = 2^{23}–1 data pattern at 800 Mbps**
- **Single +3.3 V Supply**
- **Less than 413 mW (typ) total power dissipation**
- **Balanced output impedance**
- **Output channel-to-channel skew is 35ps (typ)**
- **Differential output voltage (V_{OD}) is 320mV (typ) with 100Ω termination load.**
- **LVDS receiver inputs accept LVPECL signals**
- **Fast propagation delay of 2.8 ns (typ)**
- **Receiver input threshold < ±100 mV**
- **28 lead TSSOP package**
- **Conforms to ANSI/TIA/EIA-644 LVDS standard**

DESCRIPTION

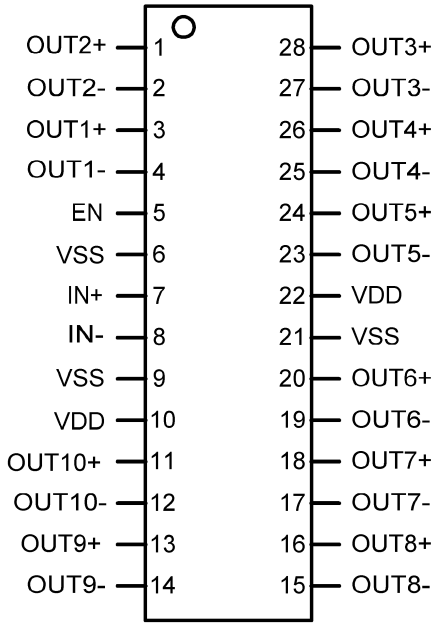
DS90LV110 is a 1 to 10 data/clock distributor utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The design allows connection of 1 input to all 10 outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential 1 to 10 signal distribution / fanout replacing multi-drop bus applications for higher speed links with improved signal quality. It can also be used for clock distribution up to 400MHz.

The DS90LV110 accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

The LVDS outputs can be put into TRI-STATE by use of the enable pin.

For more details, please refer to the APPLICATION INFORMATION section of this datasheet.

Connection Diagram



Order Number DS90LV110TMTC
PW0028A Package

Block Diagram

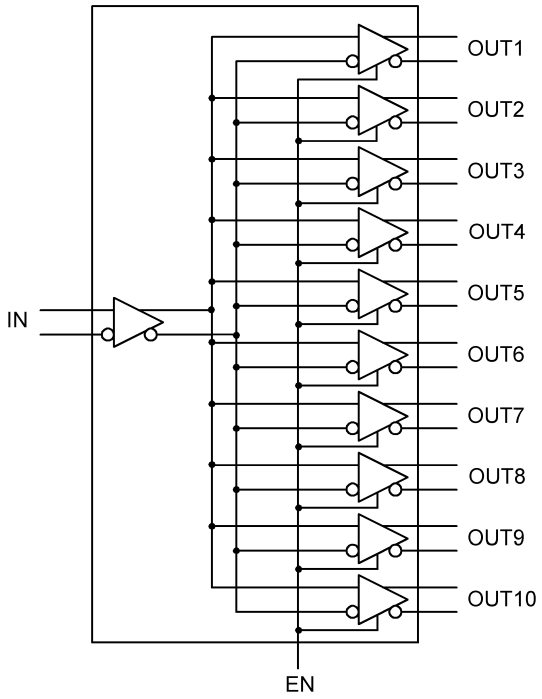


Figure 1. Block Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{DD}-V_{SS})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage (EN)	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage (IN+, IN−)	−0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT−)	−0.3V to +4V
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
28 Lead TSSOP	2.115 W
Package Derating	
28 Lead TSSOP	16.9 mW/°C above +25°C
θ_{JA} (4-Layer, 2 oz. Cu, JEDEC)	
28 Lead TSSOP	59.1 °C/Watt
ESD Rating:	
(HBM, 1.5kΩ, 100pF)	> 4 kV
(EIAJ, 0Ω, 200pF)	> 250 V

(1) “Absolute Maximum Ratings” are these beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. Electrical Characteristics provides conditions for actual device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD} - V_{SS})	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{DD}	V
Operating Free Air Temperature	-40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (EN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		V_{SS}		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V or 2.0V; V_{DD} = 3.6V		±7	±20	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V or 0.8V; V_{DD} = 3.6V		±7	±20	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.8	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	320	450	mV
		R_L = 100Ω, V_{DD} = 3.3V, T_A = 25°C	260	320	425	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	|mV|
V_{OS}	Offset Voltage (2)		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	|mV|
I_{OZ}	Output TRI-STATE Current	EN = 0V, V_{OUT} = V_{DD} or GND		±1	±10	µA
I_{OFF}	Power-Off Leakage Current	V_{DD} = 0V; V_{OUT} = 3.6V or GND		±1	±10	µA
I_{SA},I_{SB}	Output Short Circuit Current	V_{OUT+} OR V_{OUT-} = 0V or V_{DD}		12	24	|mA|
I_{SAB}	Both Outputs Shorted (3)	V_{OUT+} = V_{OUT-}		6	12	|mA|
LVDS RECEIVER DC SPECIFICATIONS (IN)						
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or +1.2V or +3.25V, V_{DD} = 3.3V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100mV, V_{DD} = 3.3V	0.05		3.25	V
I_{IN}	Input Current	V_{IN} = +3.0V, V_{DD} = 3.6V or 0V		±1	±10	µA
		V_{IN} = 0V, V_{DD} = 3.6V or 0V		±1	±10	µA
SUPPLY CURRENT						
I_{CCD}	Total Supply Current	R_L = 100Ω, C_L = 5 pF, 400 MHz, EN = High		125	195	mA
		No Load, 400 MHz, EN = High		80	125	mA
I_{CCZ}	TRI-STATE Supply Current	EN = Low		15	29	mA

(1) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
(2) V_{OS} is defined as (V_{OH} + V_{OL}) / 2.
(3) Only one output can be shorted at a time. Don't exceed the package absolute maximum rating.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LHT}	Output Low-to-High Transition Time, 20% to 80%, Figure 5 (1)			390	550	ps
T_{HLT}	Output High-to-Low Transition Time, 80% to 20%, Figure 5 (1)			390	550	ps
T_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) (2)	V_{ID} = 300mV; PRBS=2^{23}-1 data; V_{CM} = 1.2V at 800 Mbps (NRZ)		145		ps
T_{RJ}	LVDS Clock Jitter, Random (2)	V_{ID} = 300mV; V_{CM} = 1.2V at 400 MHz clock		2.8		ps
T_{PLHD}	Propagation Low to High Delay, Figure 6		2.2	2.8	3.6	ns
T_{PHLD}	Propagation High to Low Delay, Figure 6		2.2	2.8	3.6	ns
T_{SKEW}	Pulse Skew $\lvert T_{PLHD} - T_{PHLD} \rvert$ (1)			20	340	ps
T_{CCS}	Output Channel-to-Channel Skew, Figure 7 (1)			35	91	ps
T_{PHZ}	Disable Time (Active to TRI-STATE) High to Z, Figure 2			3.0	6.0	ns
T_{PLZ}	Disable Time (Active to TRI-STATE) Low to Z, Figure 2			1.8	6.0	ns
T_{PZH}	Enable Time (TRI-STATE to Active) Z to High, Figure 2			10.0	23.0	ns
T_{PZL}	Enable Time (TRI-STATE to Active) Z to Low, Figure 2			7.0	23.0	ns

(1) The parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage and temperature) range.

(2) The measurement used the following equipment and test setup: HP8133A pattern/pulse generator), 5 feet of RG-142 cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with the RG-142 cable exhibit a T_{DJ} = 26ps and T_{RJ} = 1.3 ps

AC TIMING DIAGRAMS

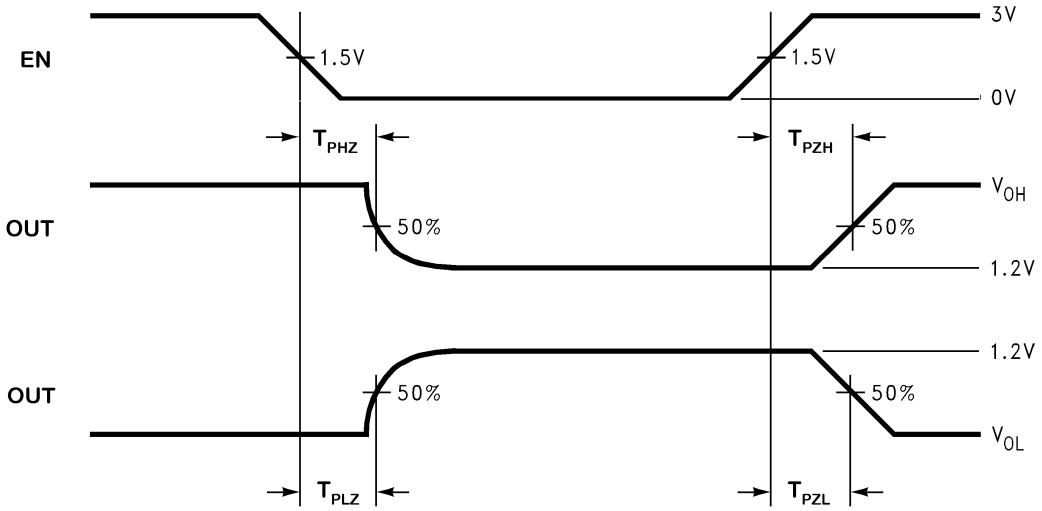


Figure 2. Output active to TRI-STATE and TRI-STATE to active output time

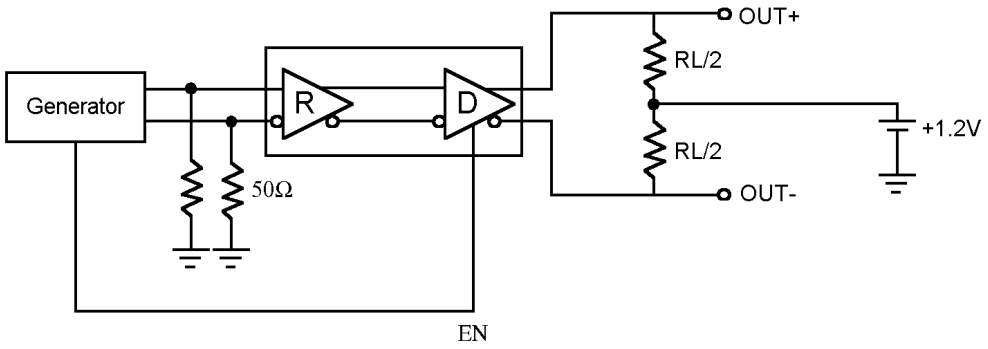


Figure 3. LVDS Driver TRI-STATE Circuit

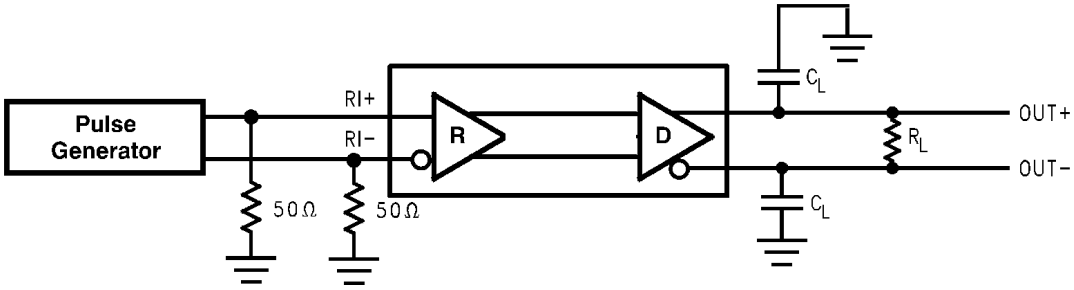


Figure 4. LVDS Output Load

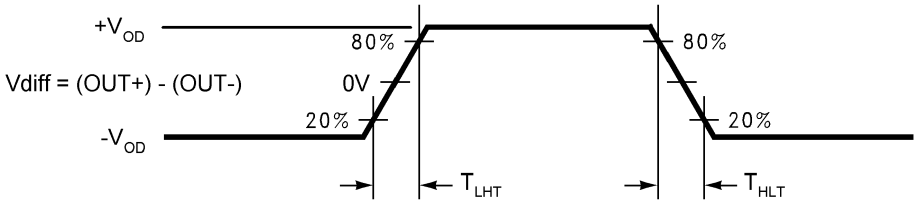


Figure 5. LVDS Output Transition Time

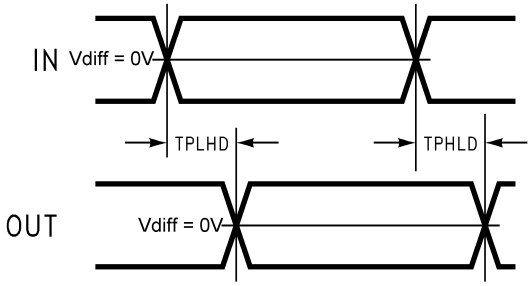


Figure 6. Propagation Delay Low-to-High and High-to-Low

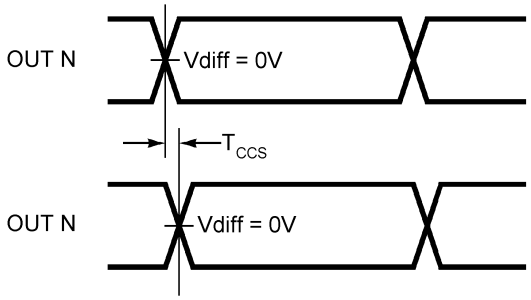


Figure 7. Output 1 to 10 Channel-to-Channel Skew

APPLICATION INFORMATION

Input Fail-Safe

The receiver inputs of the DS90LV110 do not have internal fail-safe biasing. For point-to-point and multi-drop applications with a single source, fail-safe biasing may not be required. When the driver is off, the link is in-active. If fail-safe biasing is required, this can be accomplished with external high value resistors. The IN+ should be pull to Vcc with 10kΩ and the IN− should be pull to Gnd with 10kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion. See AN-1194(SNLA051) for additional information.

LVDS Inputs Termination

The LVDS Receiver input must have a 100Ω termination resistor placed as close as possible across the input pins.

Unused Control Inputs

The EN control input pin has internal pull down device. If left open, the 10 outputs will default to TRI-STATE.

Expanding the Number of Output Ports

To expand the number of output ports, more than one DS90LV110 can be used. Total propagation delay through the devices should be considered to determine the maximum expansion. Adding more devices will increase the output jitter due to each pass.

PCB Layout and Power System Bypass

Circuit board layout and stack-up for the DS90LV110 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV110 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see Application Note: AN-1108(SNLA008) for additional information.

Multi-Drop Applications

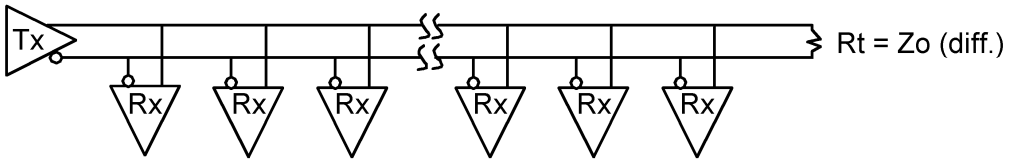


Figure 8. Multi-Drop Applications

Point-to-Point Distribution Applications

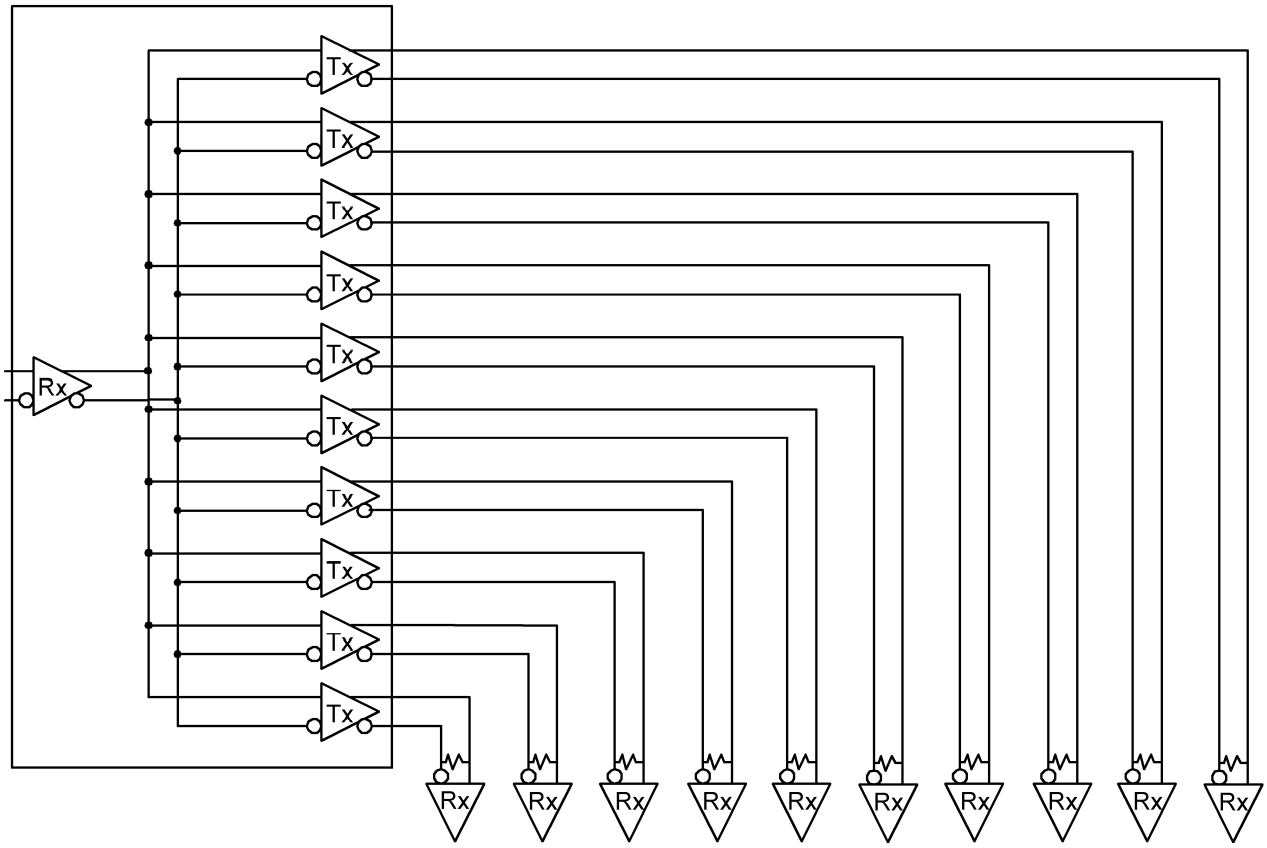


Figure 9. Point-to-Point Distribution Applications

For applications operating at data rate greater than 400Mbps, a point-to-point distribution application should be used. This improves signal quality compared to multi-drop applications due to no stub PCB trace loading. The only load is a receiver at the far end of the transmission line. Point-to-point distribution applications will have a wider LVDS bus lines, but data rate can increase well above 400Mbps due to the improved signal quality.

PIN DESCRIPTIONS

Pin Name	# of Pin	Input/Output	Description
IN+	1	I	Non-inverting LVDS input
IN -	1	I	Inverting LVDS input
OUT+	10	O	Non-inverting LVDS Output
OUT -	10	O	Inverting LVDS Output
EN	1	I	This pin has an internal pull-down when left open. A logic low on the Enable puts all the LVDS outputs into TRI-STATE and reduces the supply current.
V_{SS}	3	P	Ground (all ground pins must be tied to the same supply)
V_{DD}	2	P	Power Supply (all power pins must be tied to the same supply)

INPUT INTERFACING

The DS90LV110 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS90LV110 can be DC-coupled with all common differential drivers (that is, LVPECL, LVDS, CML). Figure 10, Figure 11, and Figure 12 illustrate typical DC-coupled interface to common differential drivers.

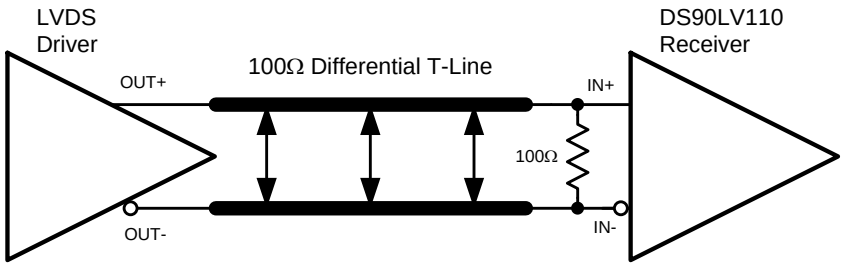


Figure 10. Typical LVDS Driver DC-Coupled Interface to DS90LV110 Input

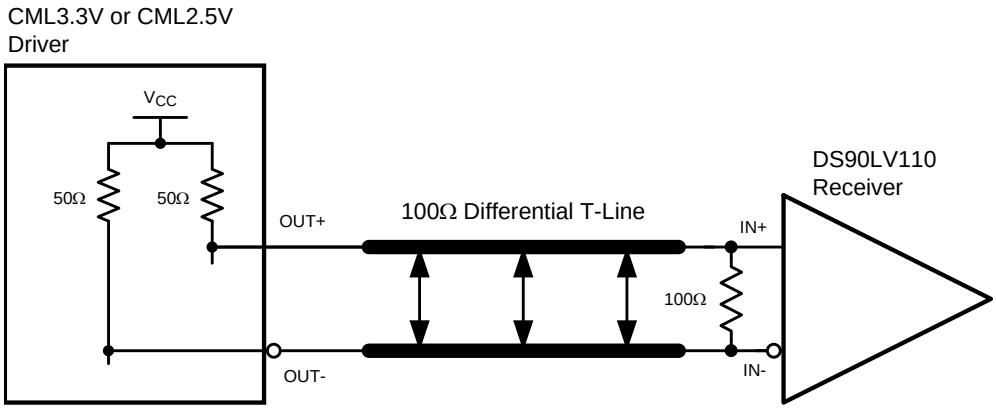


Figure 11. Typical CML Driver DC-Coupled Interface to DS90LV110 Input

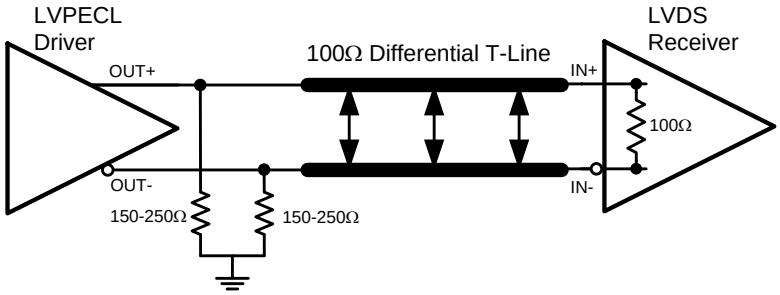


Figure 12. Typical LVPECL Driver DC-Coupled Interface to DS90LV110 Input

OUTPUT INTERFACING

The DS90LV110 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 13 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

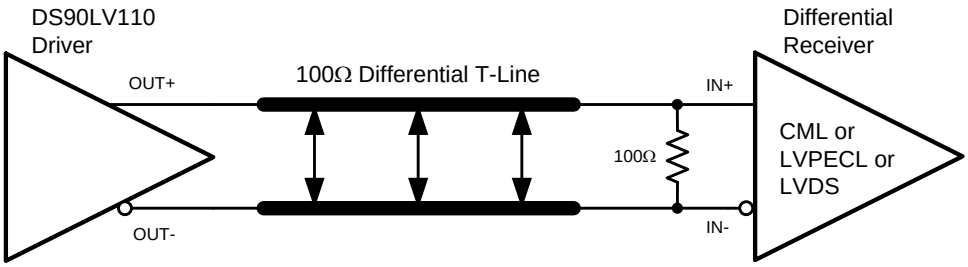
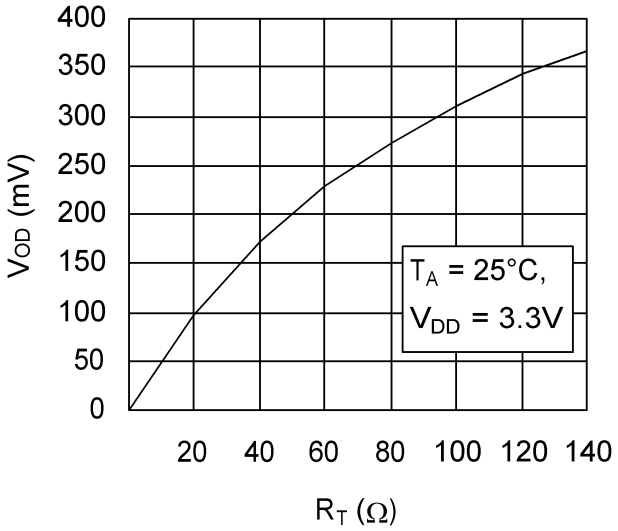


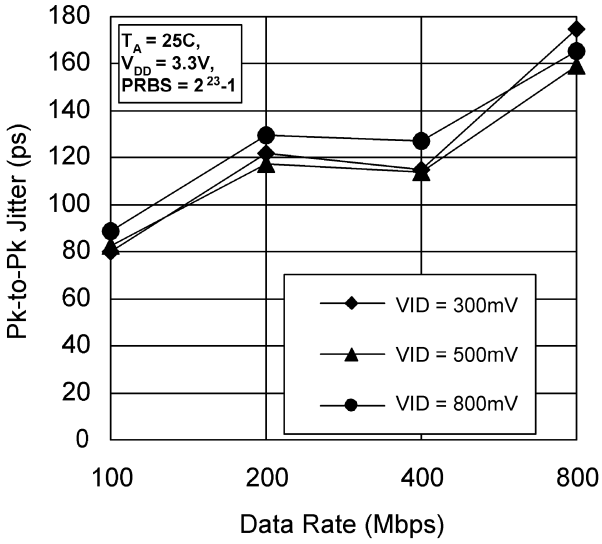
Figure 13. Typical DS90LV110 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

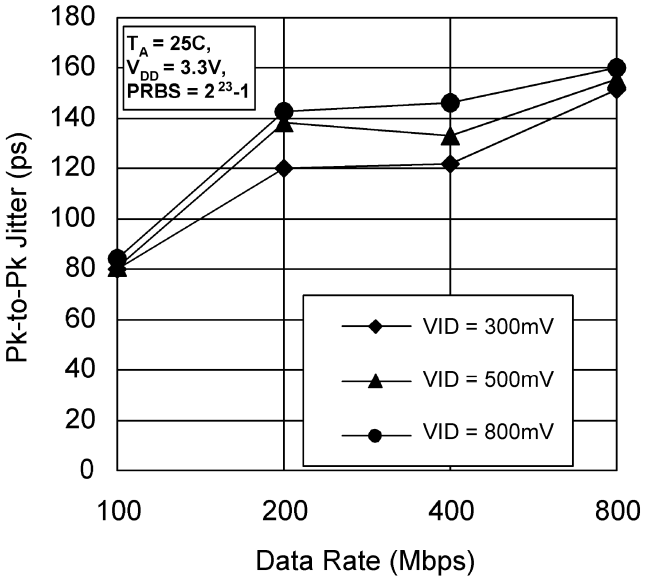
Output Voltage (V_{OD}) vs. Resistive Load (R_L)



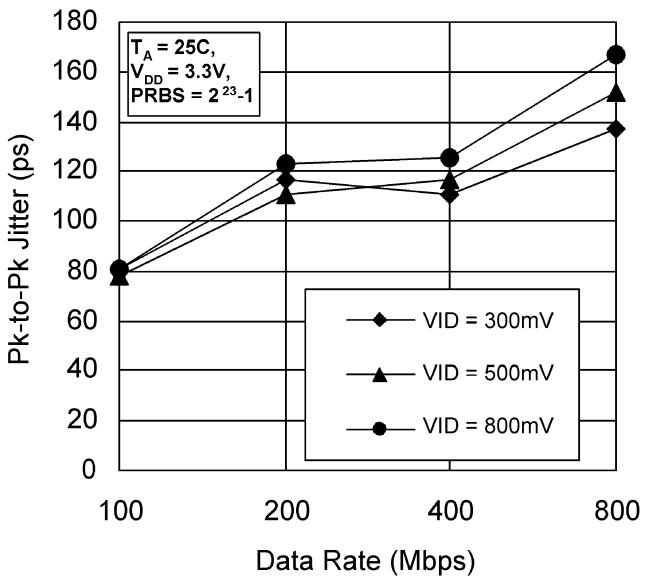
Peak-to-Peak Output Jitter at V_{CM} = +0.4V vs. VID



Peak-to-Peak Output Jitter at V_{CM} = +1.2V vs. VID



Peak-to-Peak Output Jitter at V_{CM} = +2.9V vs. VID



REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV110TMTC	NRND	TSSOP	PW	28	48	TBD	Call TI	Call TI	-40 to 85	DS90LV 110TMTC	
DS90LV110TMTC/NOPB	ACTIVE	TSSOP	PW	28	48	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS90LV 110TMTC	Samples
DS90LV110TMTCX/NOPB	ACTIVE	TSSOP	PW	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS90LV 110TMTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

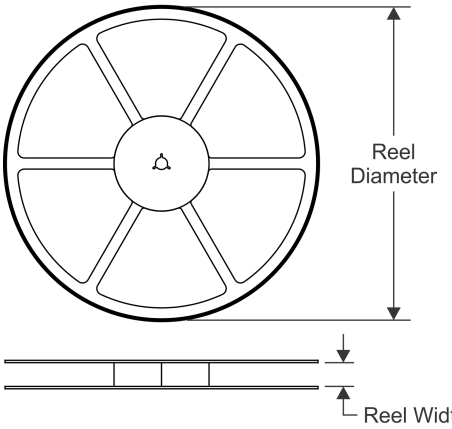
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

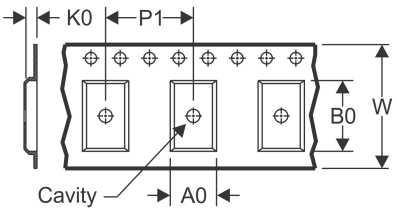
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

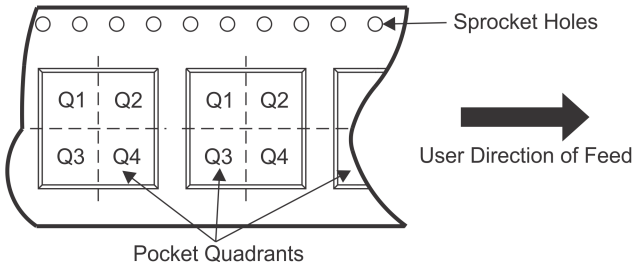


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

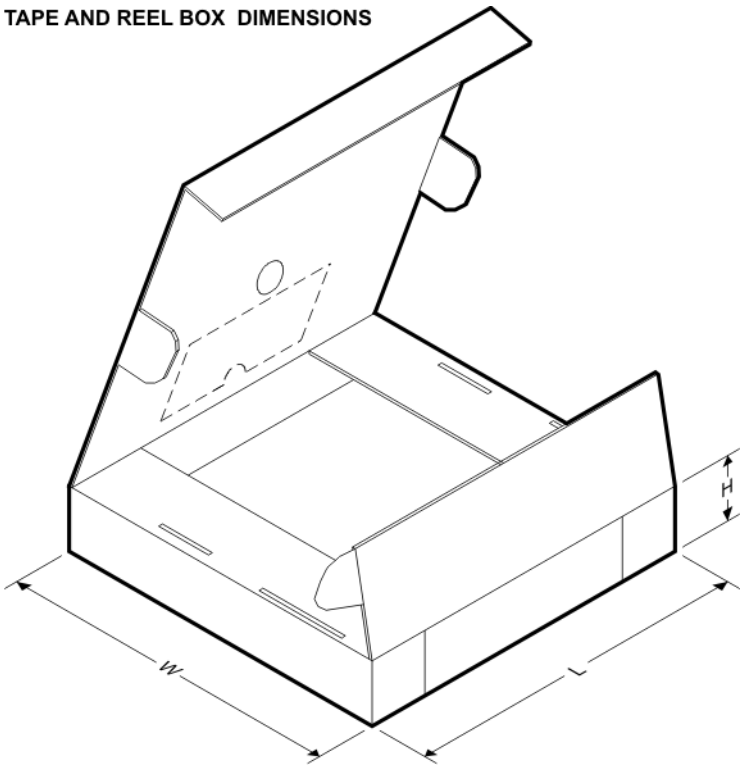
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV110TMTCX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

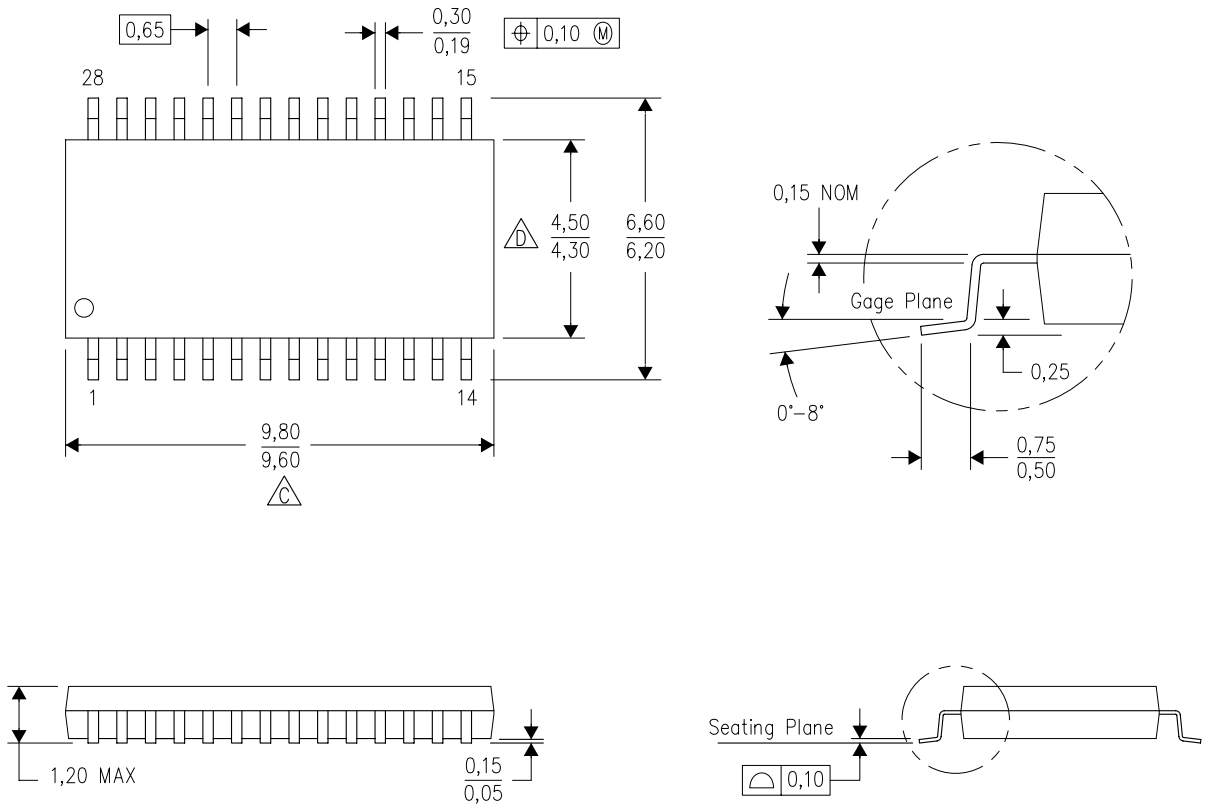
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV110TMTCX/NOPB	TSSOP	PW	28	2500	367.0	367.0	38.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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