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# FCA35N60

## N-Channel SuperFET<sup>®</sup> MOSFET

600 V, 35 A, 98 mΩ

### Features

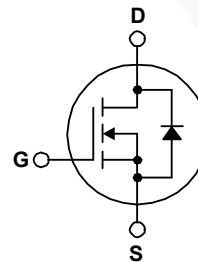
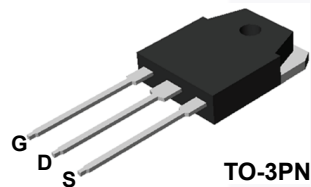
- 650V @ T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 79 mΩ
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 139 nC )
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 340 pF )
- 100% Avalanche Tested

### Applications

- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET<sup>®</sup> MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings

T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FCA35N60	Unit
V <sub>DSS</sub>	Drain to Source Voltage	600	V
V <sub>GSS</sub>	Gate-Source voltage	±30	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	35
		- Continuous (T <sub>C</sub> = 100°C)	22.2
I <sub>DM</sub>	Drain Current	- Pulsed (Note 1)	105
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	1455	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	35	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	31.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	312.5
		- Derate Above 25°C	2.5
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FCA35N60	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max.	0.4	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max.	42	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCA35N60	FCA35N60	TO-3PN	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}, T_J = 25^\circ\text{C}$	600	-	-	V
		$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}, T_J = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	-	0.6	-	V/ $^\circ\text{C}$
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 16\ \text{A}$	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 600\ \text{V}, V_{GS} = 0\ \text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\ \text{V}, T_C = 125^\circ\text{C}$	-	-	10	
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30\ \text{V}, V_{DS} = 0\ \text{V}$	-	-	$\pm 100$	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 17.5\ \text{A}$	-	0.079	0.098	$\Omega$
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40\ \text{V}, I_D = 17.5\ \text{A}$	-	28.8	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	-	4990	6640	pF
C <sub>oss</sub>	Output Capacitance		-	2380	3170	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	140	-	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 480\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	-	113	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	$V_{DS} = 0\ \text{V to } 480\ \text{V}, V_{GS} = 0\ \text{V}$	-	340	-	pF
Q <sub>g</sub>	Total Gate Charge at 10V	$V_{DS} = 480\ \text{V}, I_D = 35\ \text{A}, V_{GS} = 10\ \text{V}$ (Note 4)	-	139	181	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	31	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	69	-	nC
ESR	Equivalent Series Resistance (G-S)		$f = 1\ \text{MHz}$	-	1.4	-

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 300\ \text{V}, I_D = 35\ \text{A}, V_{GS} = 10\ \text{V}, R_G = 4.7\ \Omega$ (Note 4)	-	34	78	ns
t <sub>r</sub>	Turn-On Rise Time		-	120	250	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	105	220	ns
t <sub>f</sub>	Turn-Off Fall Time		-	73	155	ns

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	35	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	105	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_{SD} = 35\ \text{A}$	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0\ \text{V}, I_{SD} = 35\ \text{A}, di_F/dt = 100\ \text{A}/\mu\text{s}$	-	614	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	16.3	-	$\mu\text{C}$

#### Notes:

- 1: Repetitive rating; pulse-width limited by maximum junction temperature.
- 2:  $I_{AS} = 17.5\ \text{A}, V_{DD} = 50\ \text{V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
- 3:  $I_{SD} \leq 35\ \text{A}, di/dt \leq 200\ \text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
- 4: Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

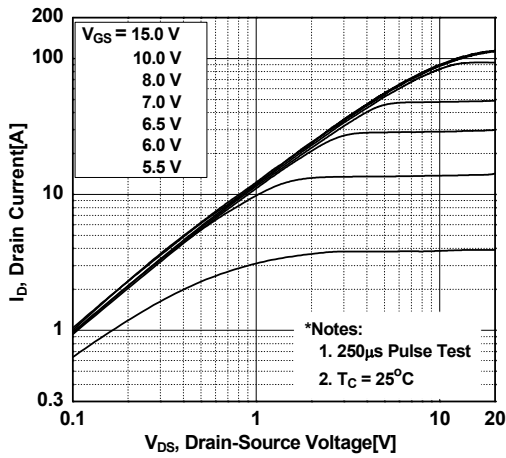


Figure 2. Transfer Characteristics

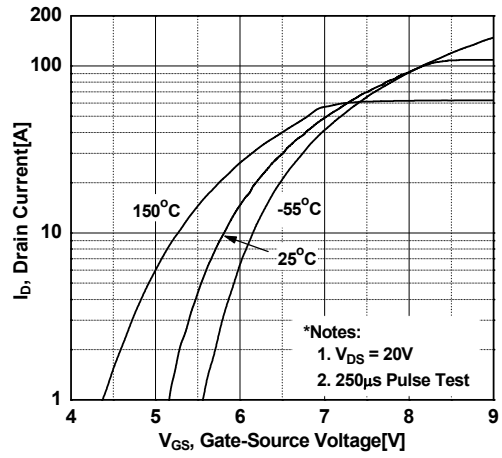


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

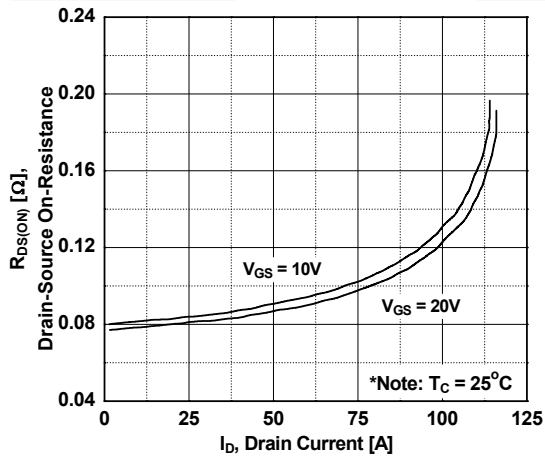


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

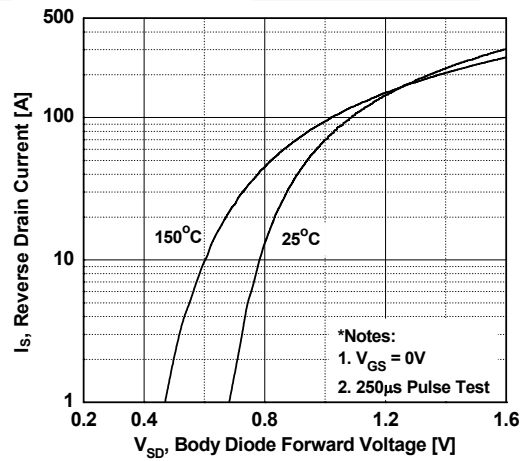


Figure 5. Capacitance Characteristics

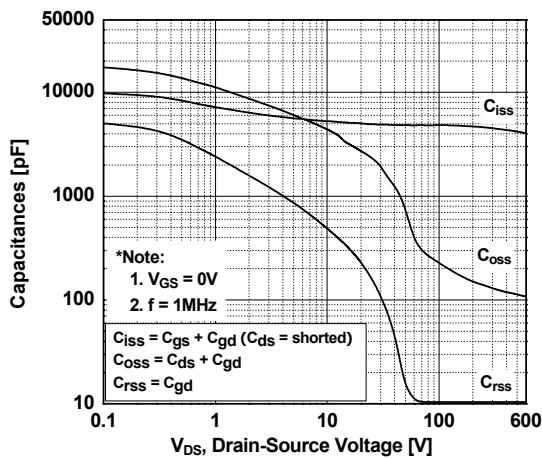
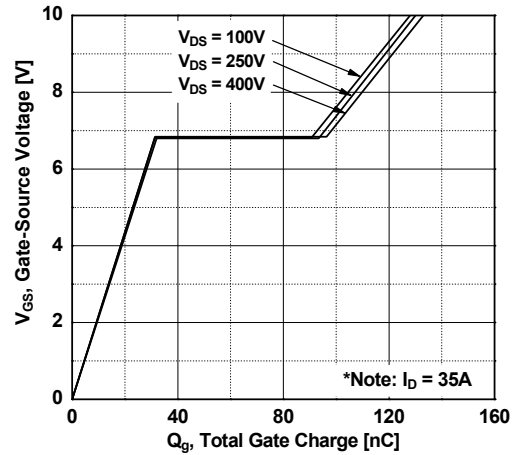
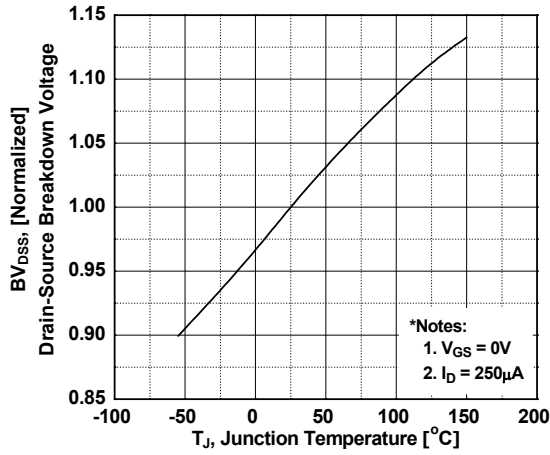


Figure 6. Gate Charge Characteristics

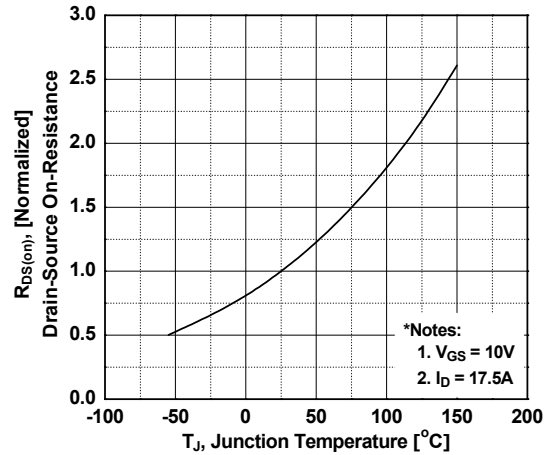


**Typical Performance Characteristics** (Continued)

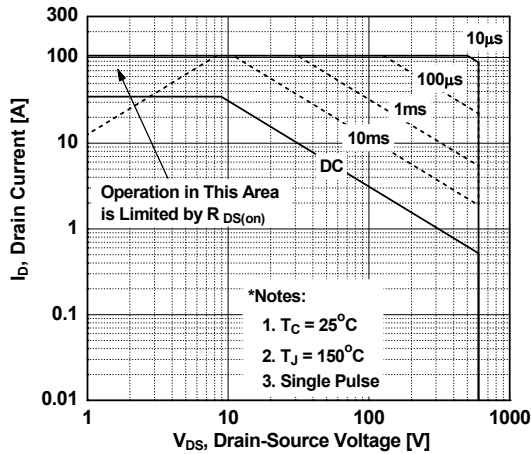
**Figure 7. Breakdown Voltage Variation vs. Temperature**



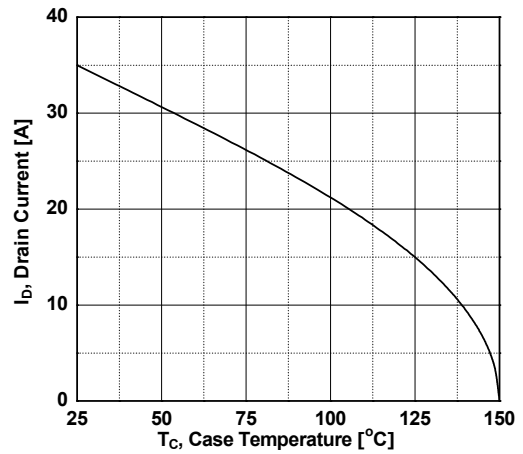
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

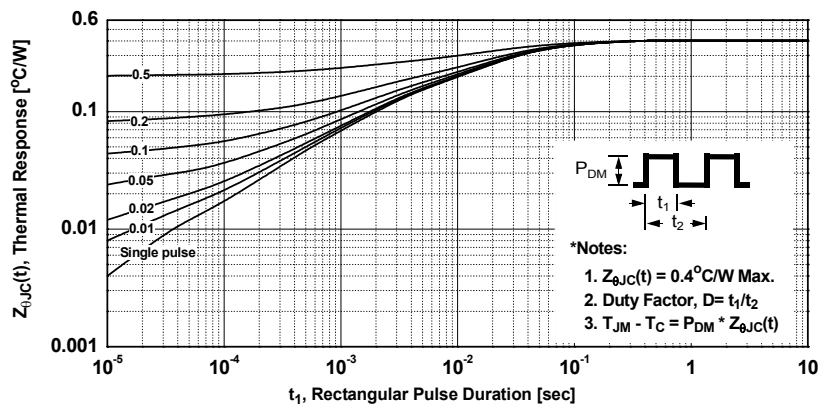




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

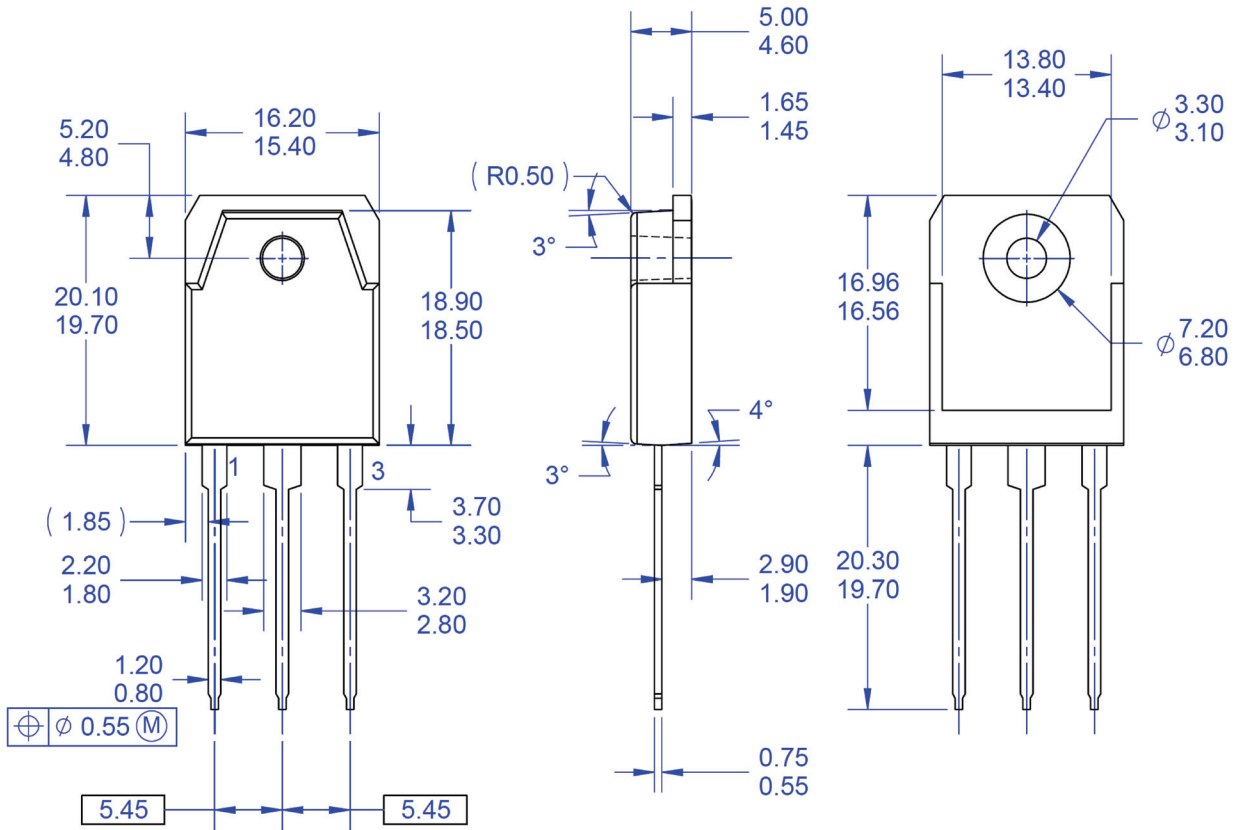


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



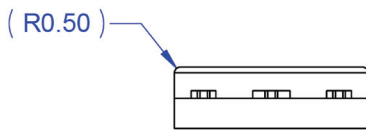
Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

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- DIMENSION AND TOLERANCING PER ASME14.5-2009.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
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**Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65**

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