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July 2014

# FCH130N60

## N-Channel SuperFET® II MOSFET

### 600 V, 28 A, 130 mΩ

## Features

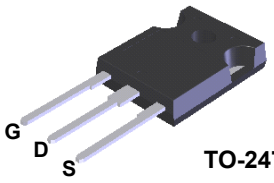
- 650 V @ $T_J$ = 150°C
- Typ. $R_{DS(on)}$ = 112 mΩ
- Ultra Low Gate Charge (Typ. $Q_g$ = 54 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 240 pF)
- 100% Avalanche Tested
- RoHS Compliant

## Applications

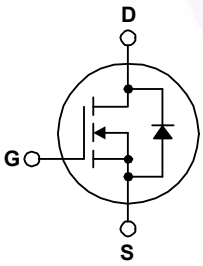
- Telecom / Sever Power Supplies
- Industrial Power Supplies
- AC-DC Power Supply

## Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.




TO-247




## Absolute Maximum Ratings $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | | | FCH130N60 | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | | 600 | V |
| $V_{GSS}$ | Gate to Source Voltage | - DC | | ±20 | V |
| | | - AC | (f > 1 Hz) | ±30 | |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C) | | 28 | A |
| | | - Continuous ($T_C$ = 100°C) | | 18 | |
| $I_{DM}$ | Drain Current | - Pulsed | (Note 1) | 84 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy | | (Note 2) | 720 | mJ |
| $I_{AR}$ | Avalanche Current | | (Note 1) | 6 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | | (Note 1) | 2.78 | mJ |
| dv/dt | MOSFET dv/dt | | | 100 | V/ns |
| | Peak Diode Recovery dv/dt | | (Note 3) | 20 | |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | | 278 | W |
| | | - Derate Above 25°C | | 2.2 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering,1/8" from Case for 5 Seconds | | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | FCH130N60 | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 0.45 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | 40 | |

## Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| FCH130N60 | FCH130N60 | TO-247 | Tube | N/A | N/A | 30 units |

## Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 25°C | 600 | - | - | V |
| | | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 150°C | 650 | - | - | |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 10 mA, Referenced to 25°C | - | 0.67 | - | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 480 V, $V_{GS}$ = 0 V, $T_C$ = 125°C | - | 2.5 | - | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.5 | - | 3.5 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 14 A | - | 112 | 130 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 14 A | - | 26 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 380 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 2700 | 3590 | pF |
| $C_{oss}$ | Output Capacitance | | - | 65 | 85 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 2.85 | - | pF |
| $C_{oss(eff.)}$ | Effective Output Capacitance | $V_{DS}$ = 0 V to 480 V, $V_{GS}$ = 0 V | - | 240 | - | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 380 V, $I_D$ = 14 A, $V_{GS}$ = 10 V (Note 4) | - | 54 | 70 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 12 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 14 | - | nC |
| ESR | Equivalent Series Resistance | f = 1 MHz | - | 1 | - | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 380 V, $I_D$ = 14 A, $V_{GS}$ = 10 V, $R_g$ = 4.7 Ω (Note 4) | - | 25 | 60 | ns |
| $t_r$ | Turn-On Rise Time | | - | 16 | 42 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 65 | 140 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 4 | 18 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 28 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 84 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 14 A | - | - | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_{SD}$ = 14 A, $dI_F/dt$ = 100 A/μs | - | 376 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 7.6 | - | μC |

**Notes:**

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS}$ = 6 A, $V_{DD}$ = 50 V, $R_G$ = 25 Ω, starting $T_J$ = 25°C.
3. $I_{SD}$ ≤ 14 A, di/dt ≤ 200 A/μs, $V_{DD}$ ≤ $BV_{DSS}$, starting $T_J$ = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

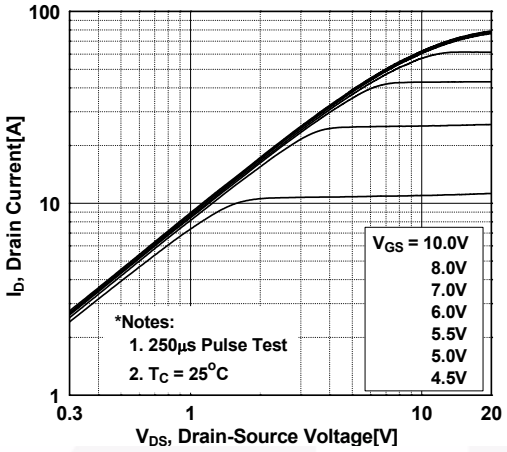



**Figure 2. Transfer Characteristics**

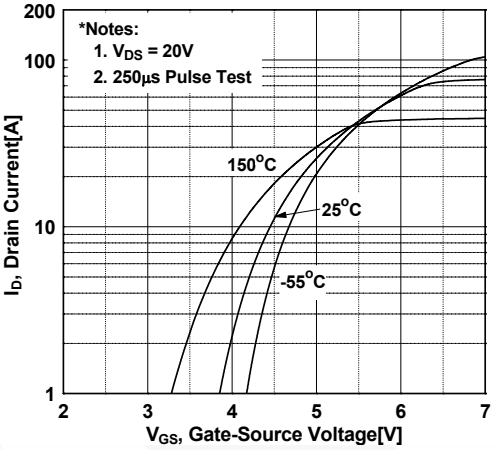



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

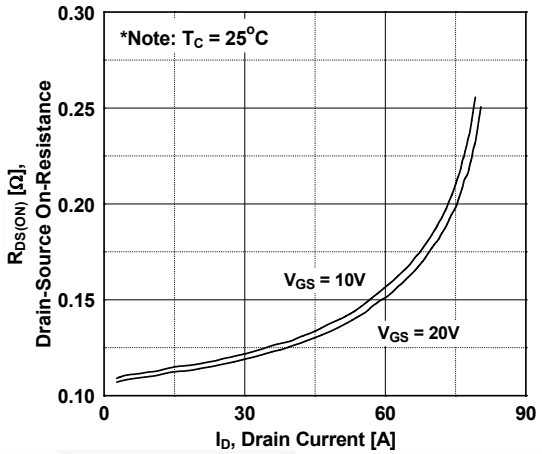



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

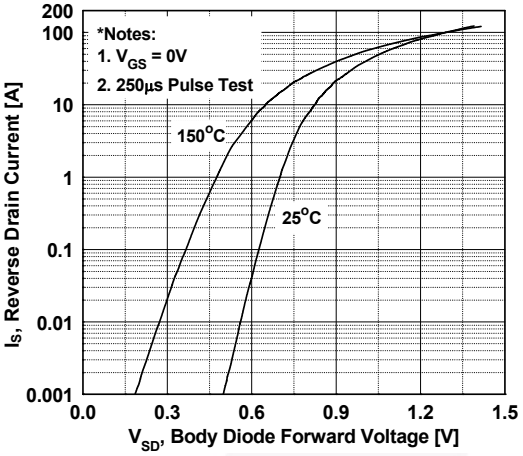



**Figure 5. Capacitance Characteristics**

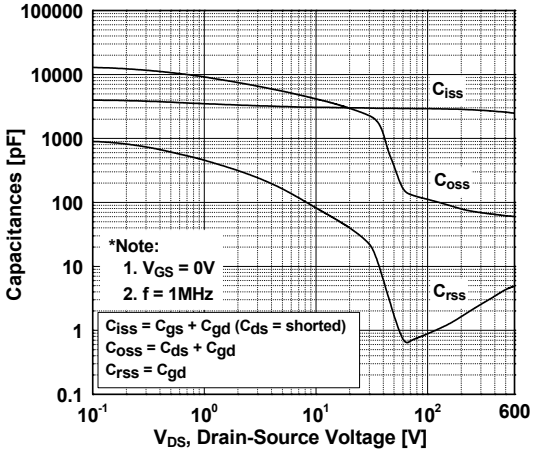
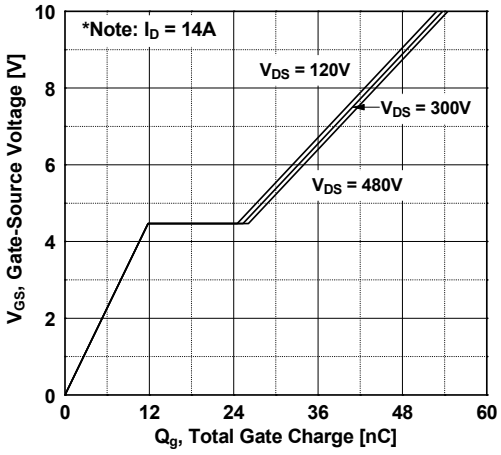



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

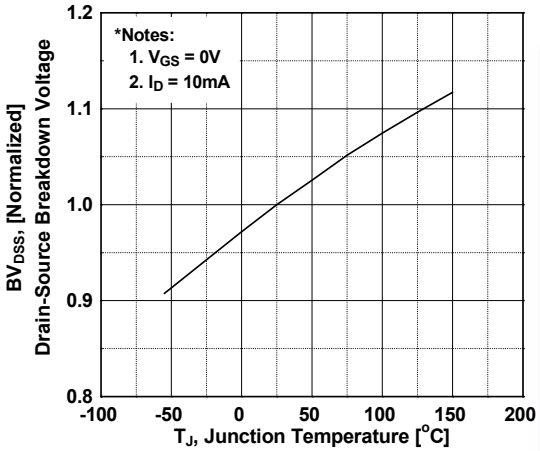



**Figure 8. On-Resistance Variation vs. Temperature**

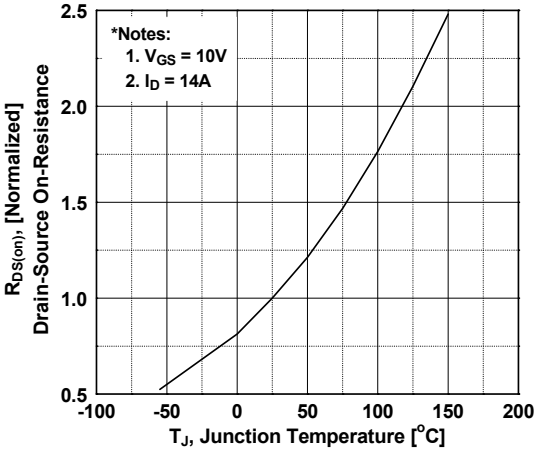



**Figure 9. Maximum Safe Operating Area**

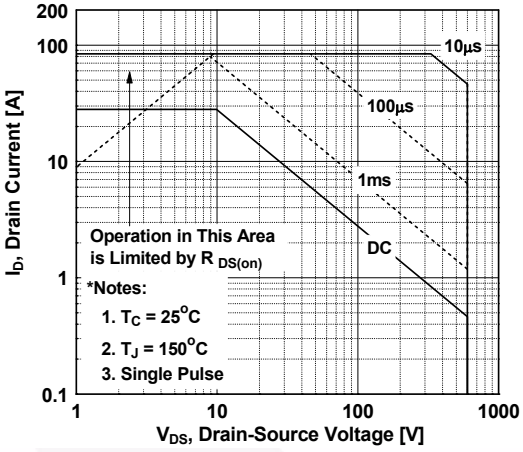



**Figure 10. Maximum Drain Current vs. Case Temperature**

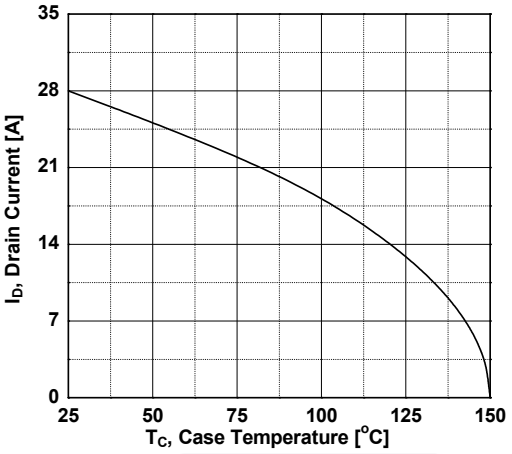
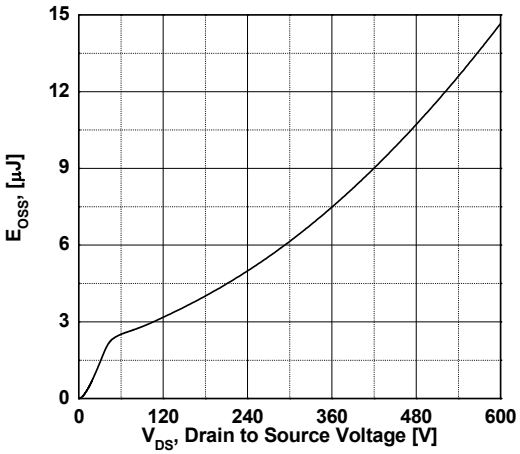
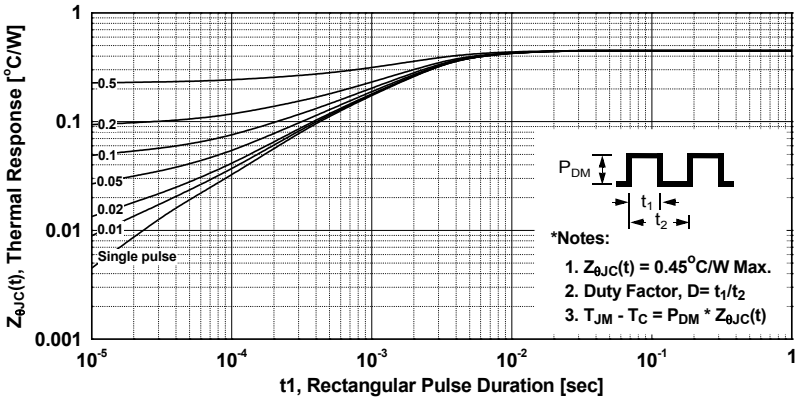



**Figure 11. Eoss vs. Drain to Source Voltage**



## Typical Performance Characteristics (Continued)

**Figure 12. Transient Thermal Response Curve**



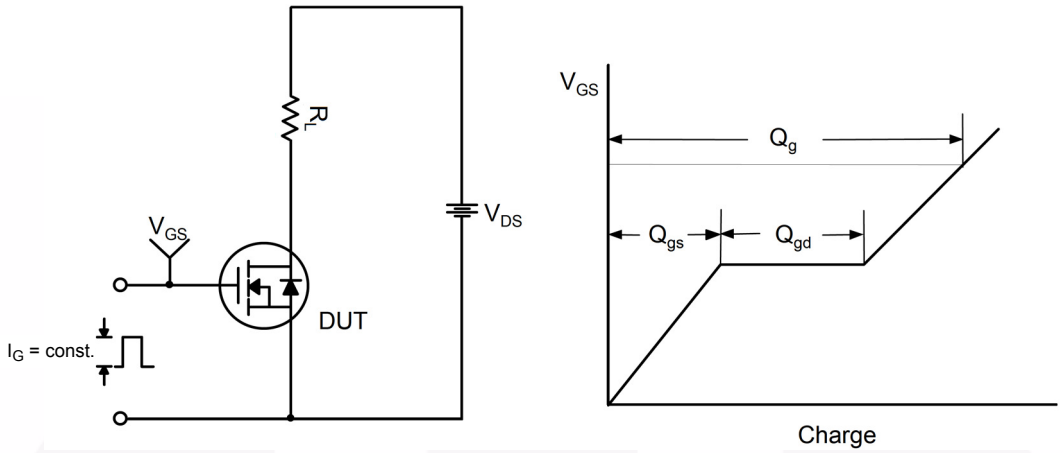



**Figure 13. Gate Charge Test Circuit & Waveform**

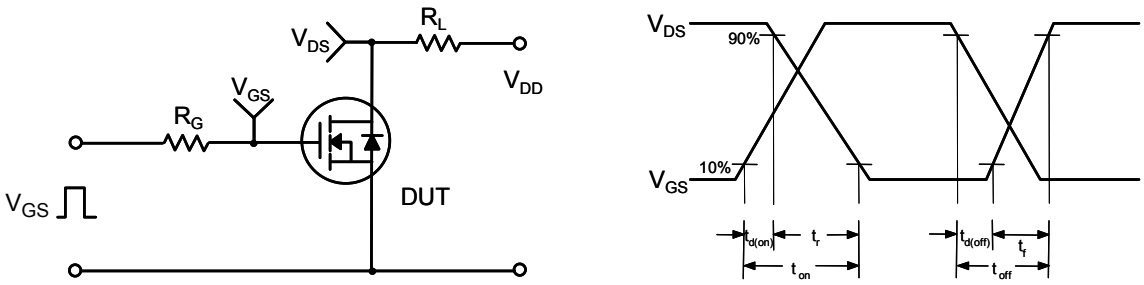



**Figure 14. Resistive Switching Test Circuit & Waveforms**

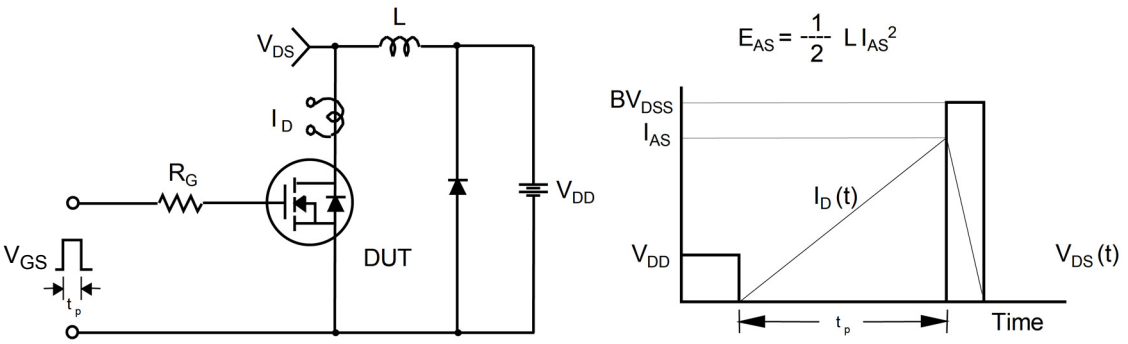



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

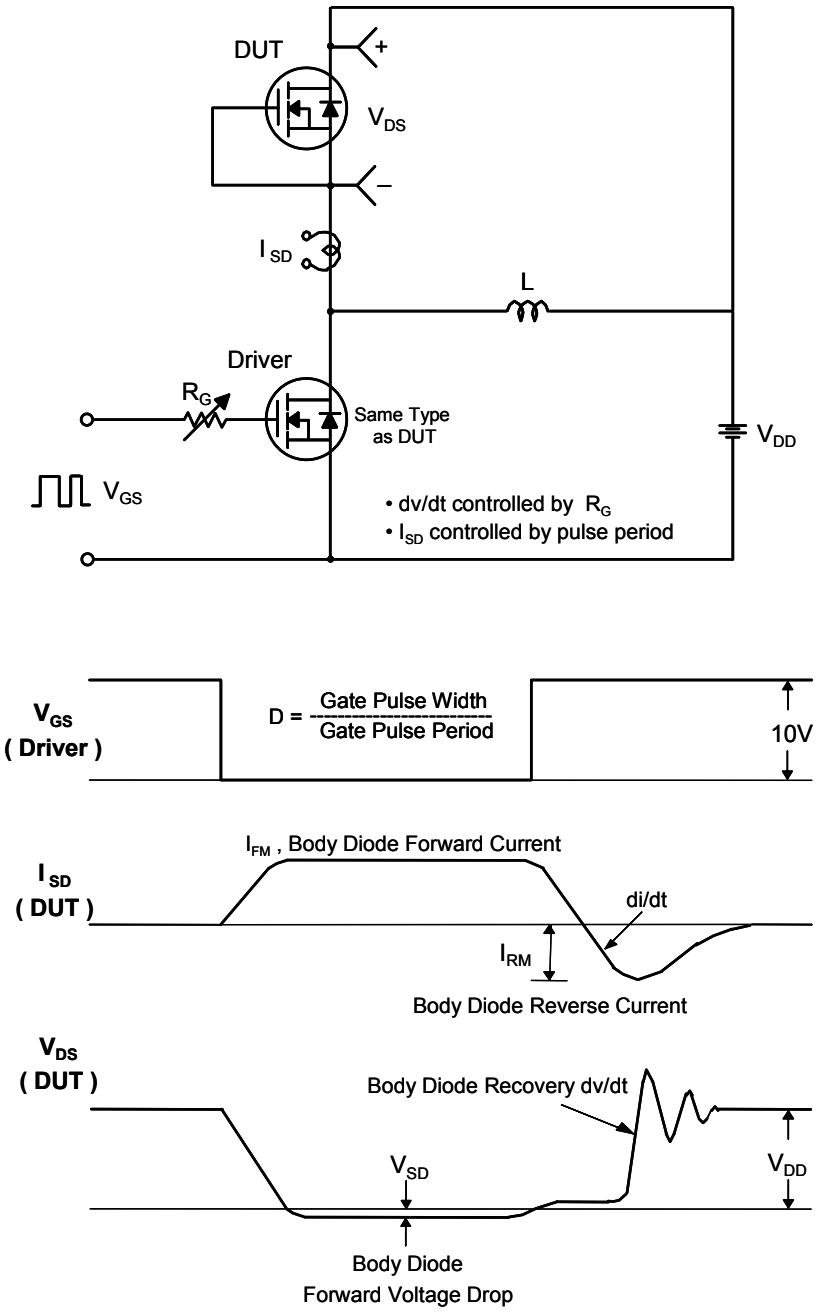
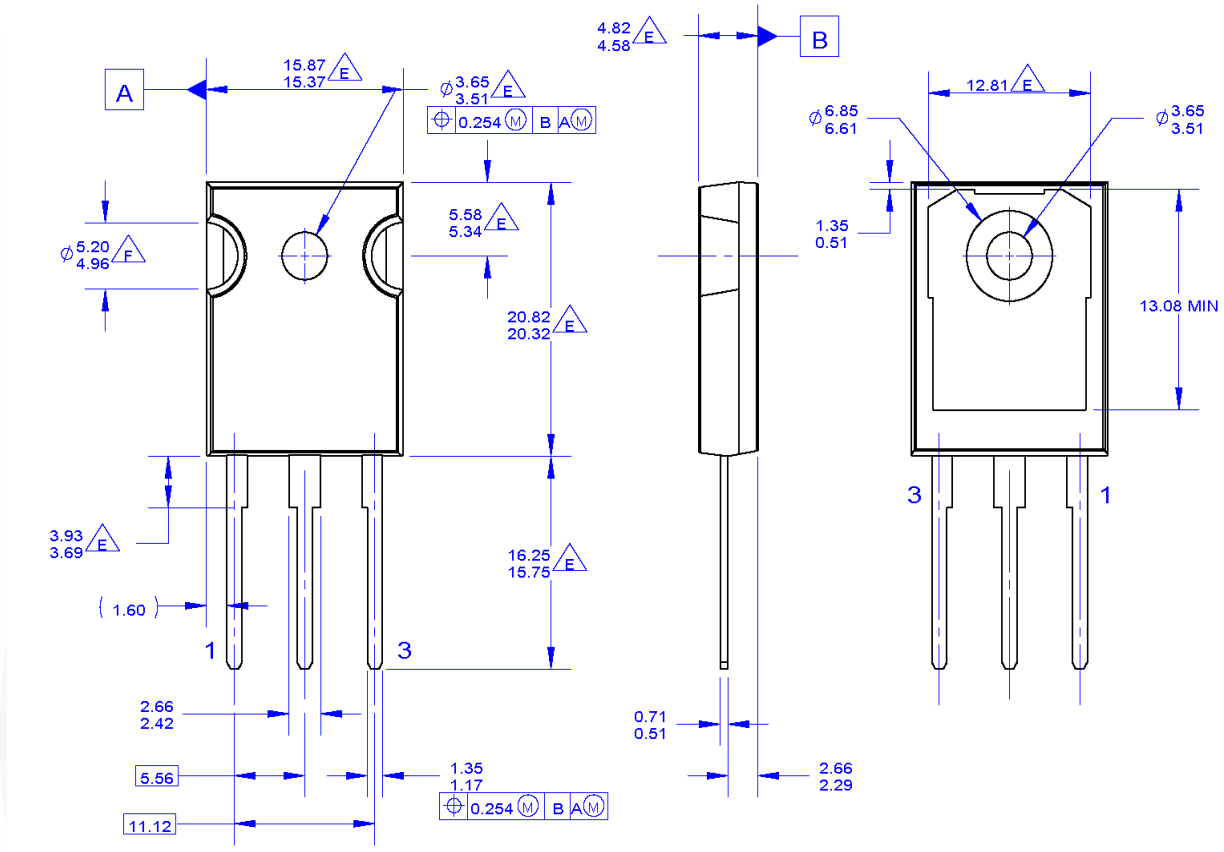



**Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

## Mechanical Dimensions

TO-247 3L

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F NOTCH MAY BE SQUARE
G. DRAWING FILENAME: MKT-TO247A03_REV03

**Figure 17. TO-247,Molded, 3 Lead, Jedec Variation AB**

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| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
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Rev. I68

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