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FAIRCHILD SEMICONDUCTOR®

November 2013

FCH47N60NF

N-Channel SupreMOS® FRFET® MOSFET

600 V, 45.8 A, 65 mΩ

Features

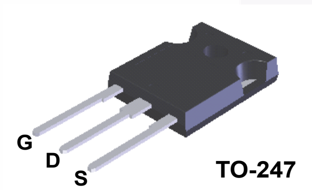
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 57.5 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 240 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 420 pF)
- 100% Avalanche Tested
- RoHS Compliant

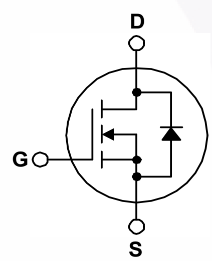
Application

- Solar Inverter
- AC-DC Power Supply

Description

The SupreMOS® MOSFET is Fairchild Semiconductor's next generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest Rsp on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SupreMOS FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCH47N60NF	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	45.8	A
		- Continuous (T_C = 100°C)	28.9	
I_{DM}	Drain Current	- Pulsed (Note 1)	137.4	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	2926	mJ
I_{AR}	Avalanche Current	(Note 1)	15.3	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.7	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt	(Note 3)	50	V/ns
P_D	Power Dissipation	(T_C = 25°C)	368	W
		- Derate Above 25°C	2.94	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCH47N60NF	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.34	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH47N60NF	FCH47N60NF	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V, T_C = 25°C	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	-	0.78	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 480 V, V_{GS} = 0 V	-	-	10	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_C = 125°C	-	-	100	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 23.5 A	-	57.5	65.0	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 23.5 A	-	52	100	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	4600	6120	pF
C_{oss}	Output Capacitance		-	195	260	pF
C_{rss}	Reverse Transfer Capacitance		-	3.0	5.0	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	108	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 380 V, V_{GS} = 0 V	-	492	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 23.5 A, V_{GS} = 10 V (Note 4)	-	121	157	nC
Q_{gs}	Gate to Source Gate Charge		-	23	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	47	-	nC
ESR	Equivalent Series Resistance(G-S)	f = 1 MHz	-	0.9	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 23.5 A, R_G = 4.7 Ω (Note 4)	-	34	78	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	117	244	ns
t_f	Turn-Off Fall Time		-	4	18	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	47	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	141	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 23.5 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 23.5 A, dI_F/dt = 100 A/µs	-	169	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.3	-	µC

Notes:
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 15.3 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 45.8 A, di/dt ≤ 1200 A/µs, V_{DD} ≤ 380 V, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

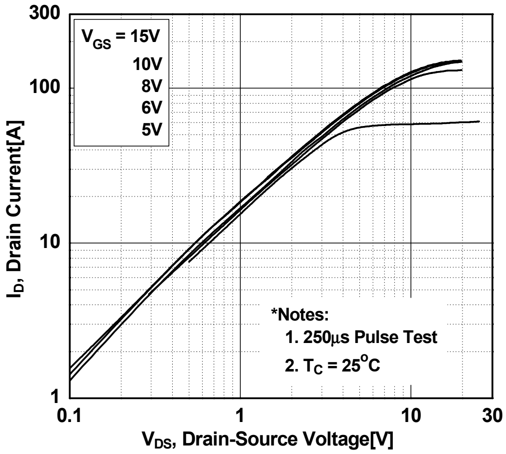


Figure 2. Transfer Characteristics

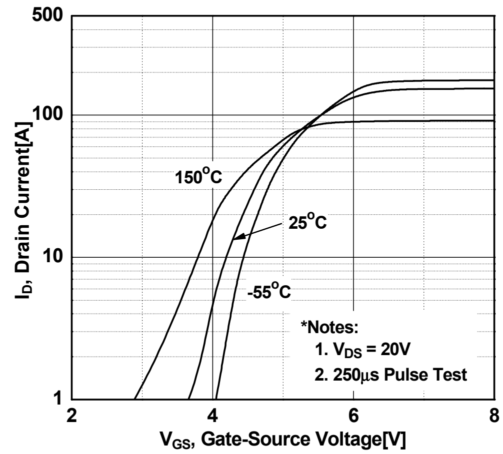


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

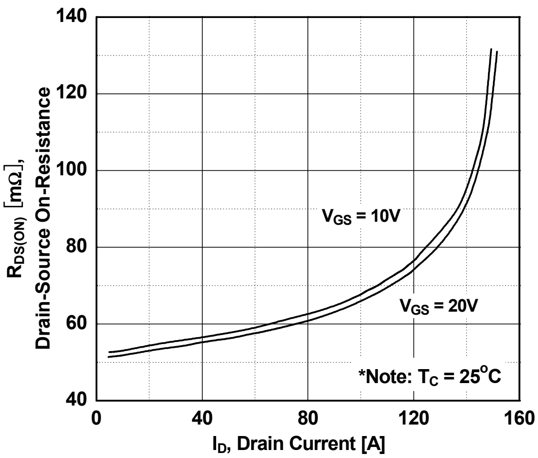


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

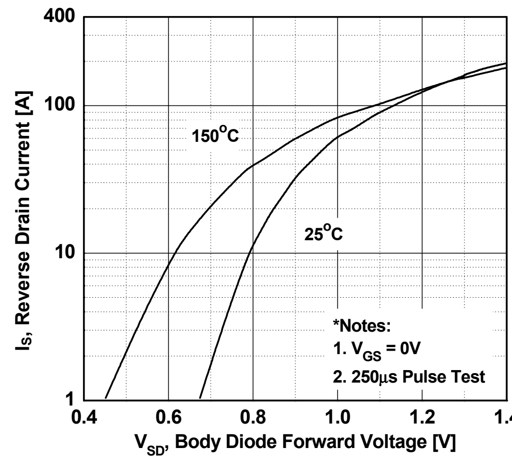


Figure 5. Capacitance Characteristics

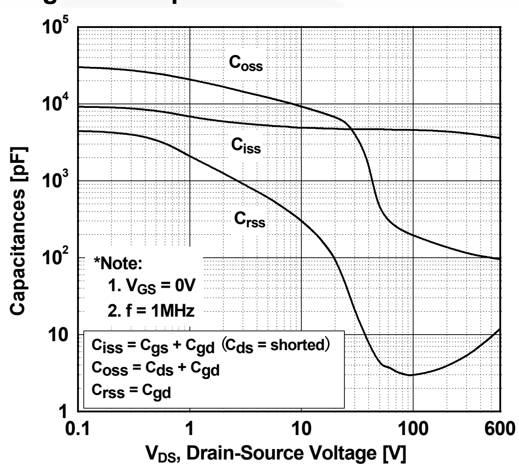
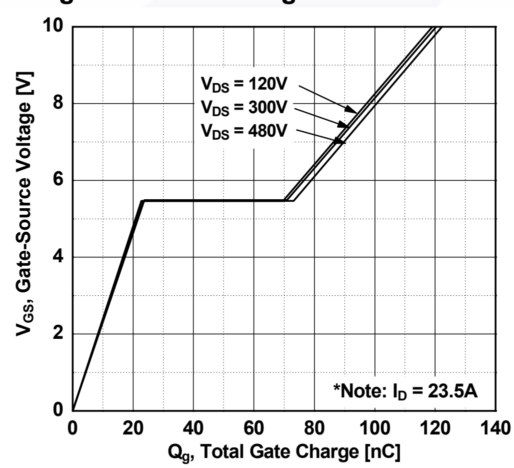


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

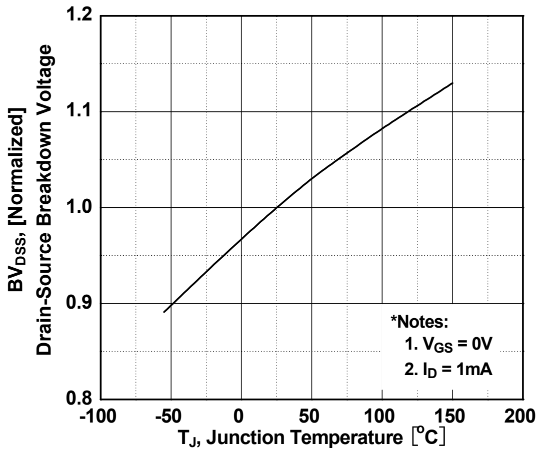


Figure 8. On-Resistance Variation vs. Temperature

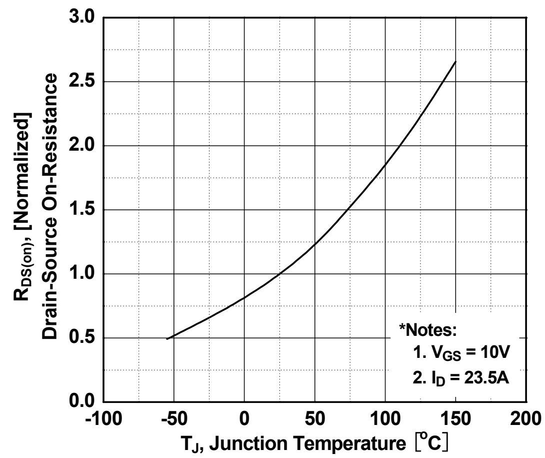


Figure 9. Maximum Safe Operating Area

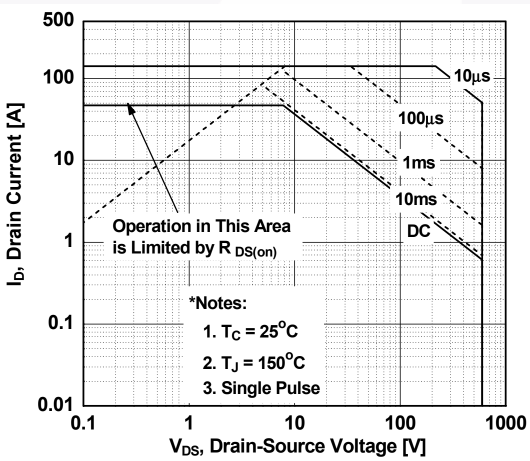


Figure 10. Maximum Drain Current vs. Case Temperature

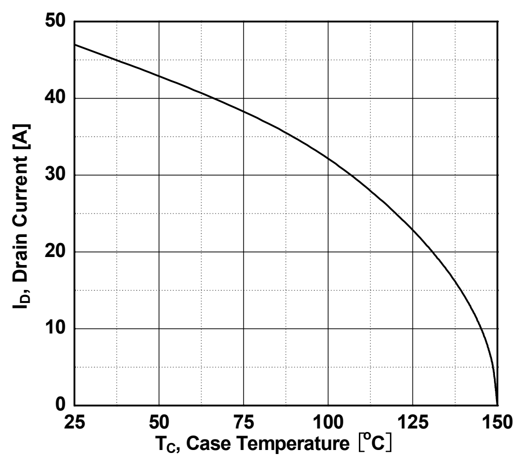
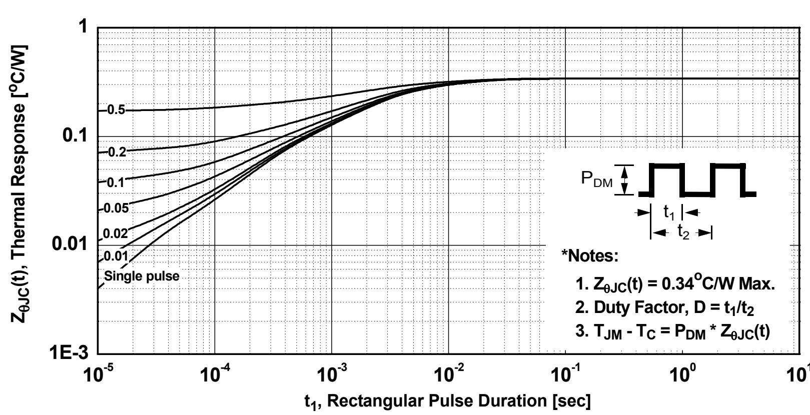


Figure 11. Transient Thermal Response Curve



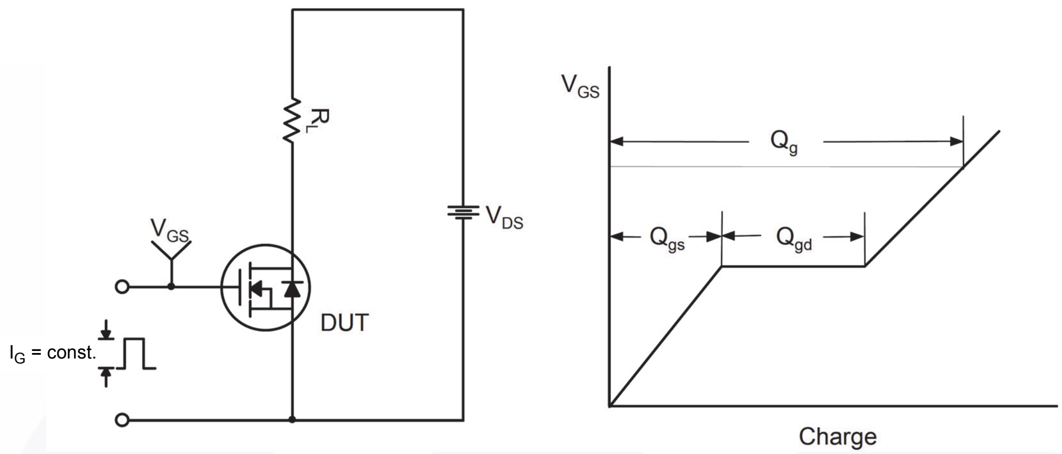


Figure 12. Gate Charge Test Circuit & Waveform

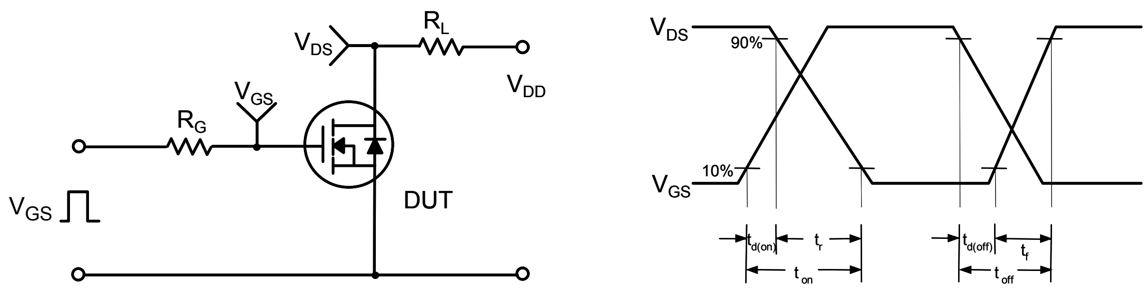


Figure 13. Resistive Switching Test Circuit & Waveforms

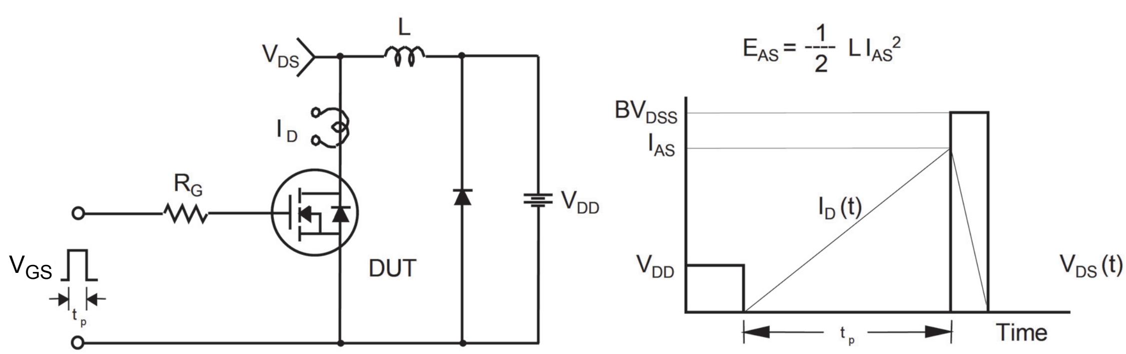


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

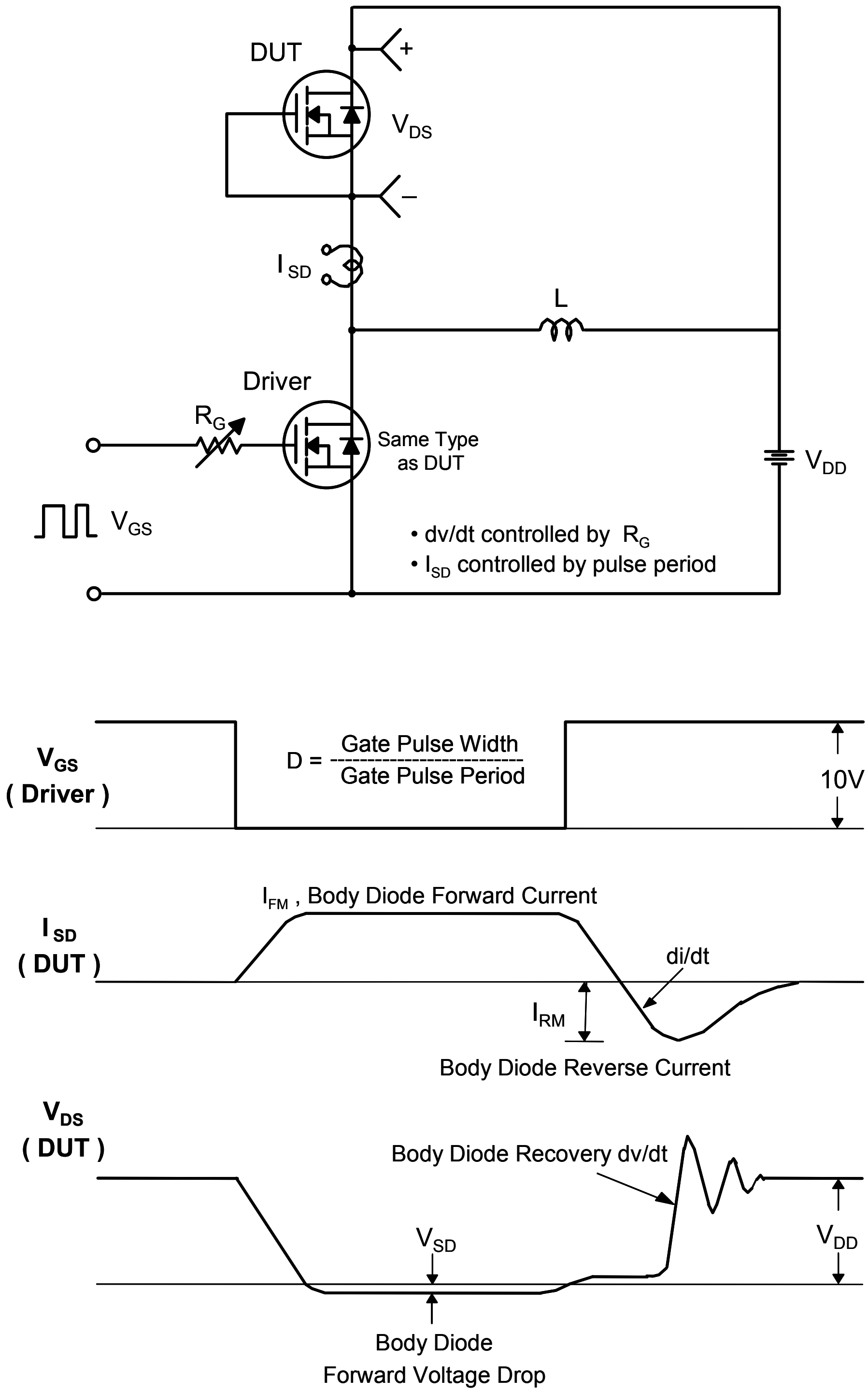
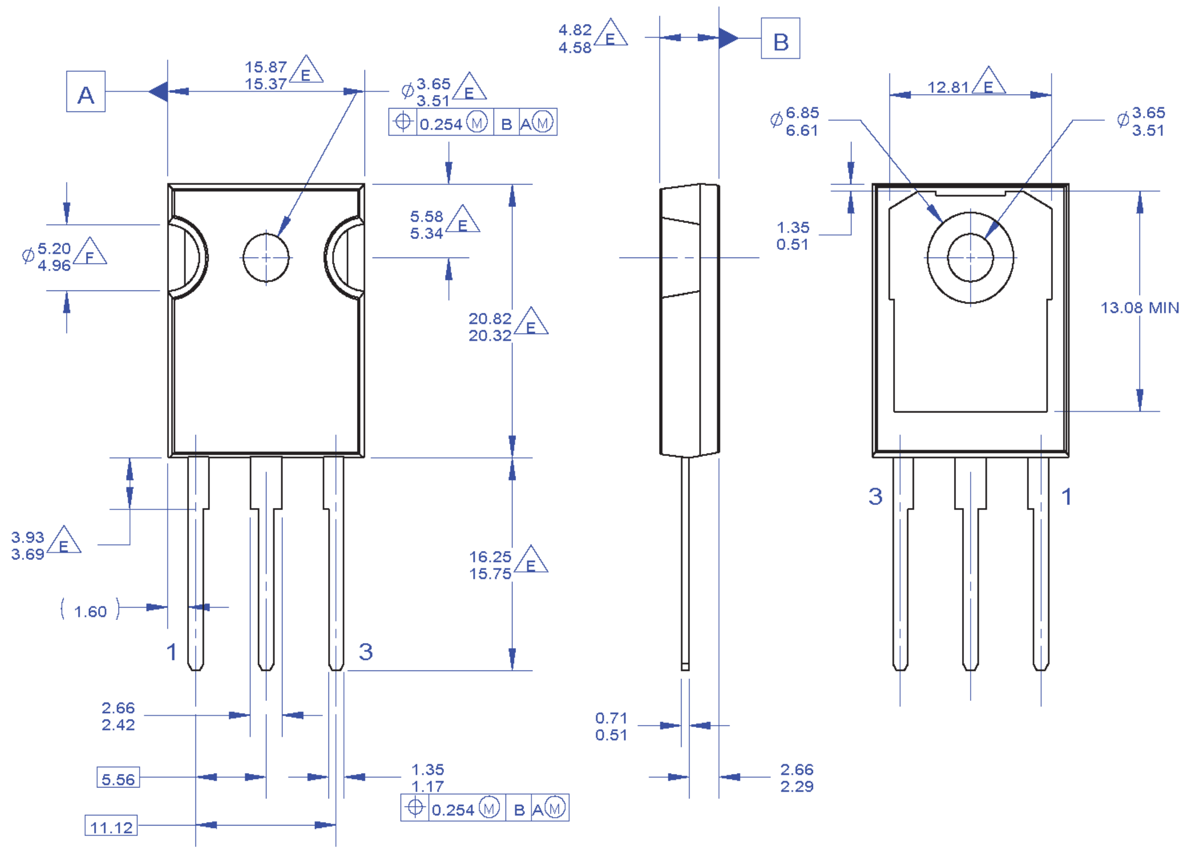


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



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E. DOES NOT COMPLY JEDEC STANDARD VALUE

F. NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 16. TO-247, Molded, 3-Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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