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FDD5612

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60V N-Channel PowerTrench[®] MOSFET

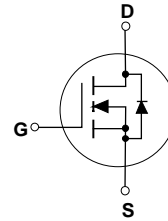
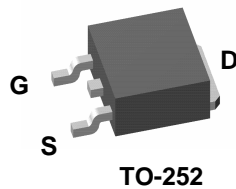
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 18 A, 60 V. $R_{DS(ON)} = 55\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 64\text{ m}\Omega @ V_{GS} = 6\text{ V}$
- Optimized for use in high frequency DC/DC converters.
- Low gate charge.
- Very fast switching.



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1)	18	A
	Drain Current – Pulsed (Note 1a)	5.4	
P_D	Maximum Power Dissipation (Note 1)	42	W
	(Note 1a)	3.8	
	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
		(Note 1b)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5612	FDD5612	13"	16mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 1)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30\text{ V}, I_D = 5.4\text{ A}$			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				5.4	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		62		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.4\text{ A}$ $V_{GS} = 6\text{ V}, I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 5.4\text{ A}, T_J = 125^\circ\text{C}$		36 42 64	55 64 103	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5.4\text{ A}$		15		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		660		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		79		pF
C_{riss}	Reverse Transfer Capacitance			36		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 1\text{ A}$		8	16	ns
t_r	Turn-On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		4	8	ns
$t_{d(off)}$	Turn-Off Delay Time			24	38	ns
t_f	Turn-Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 5.4\text{ A}$		7.5	11	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		2.5		nC
Q_{gd}	Gate-Drain Charge			3		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current				2.7	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.7\text{ A}$ (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab.

$R_{\theta JA}$ is the guaranteed design while $R_{\theta JA}$ is determined by the user's design. $R_{\theta JA}$ has been used to determine some of the maximum ratings.



a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2oz copper.



b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted on a 0.076 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

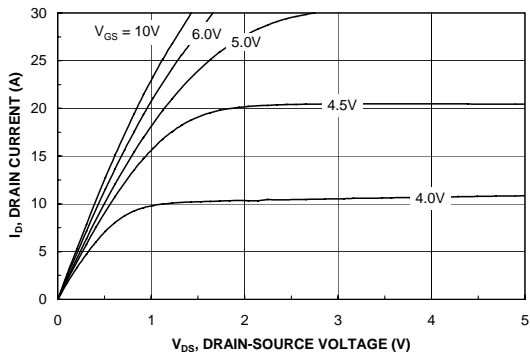


Figure 1. On-Region Characteristics.

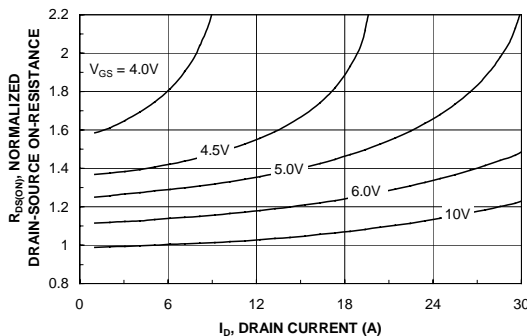


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

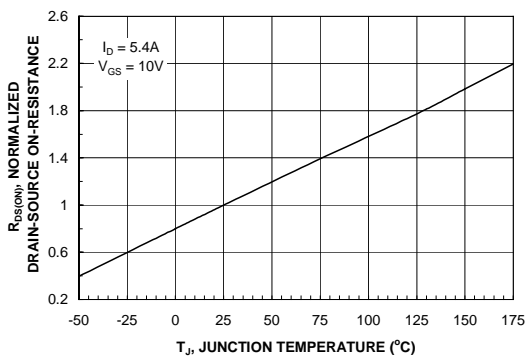


Figure 3. On-Resistance Variation with Temperature.

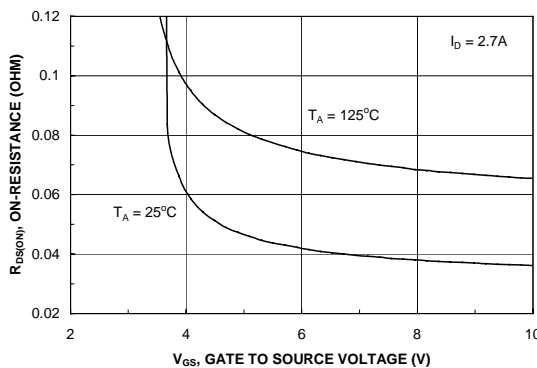


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

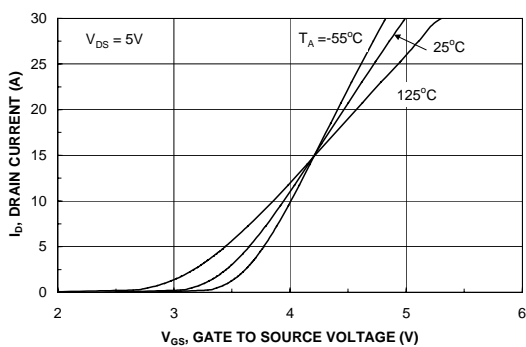


Figure 5. Transfer Characteristics.

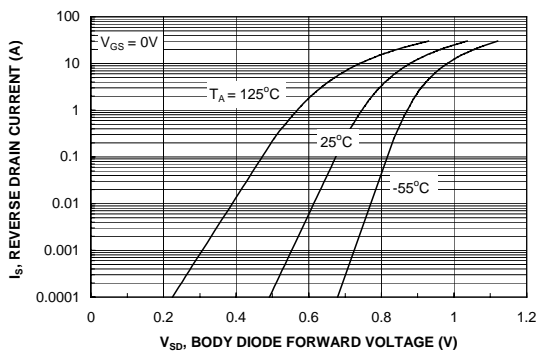


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

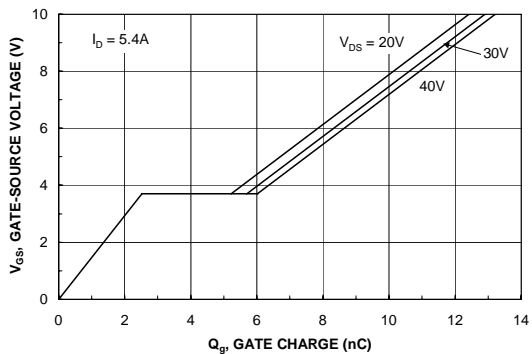


Figure 7. Gate Charge Characteristics.

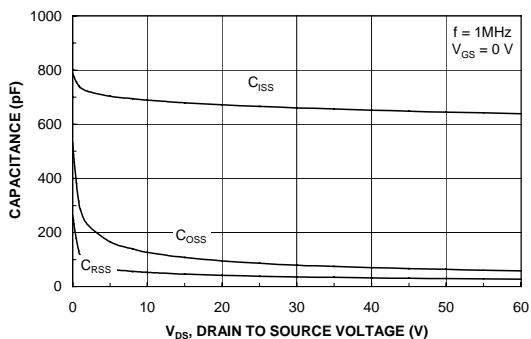


Figure 8. Capacitance Characteristics.

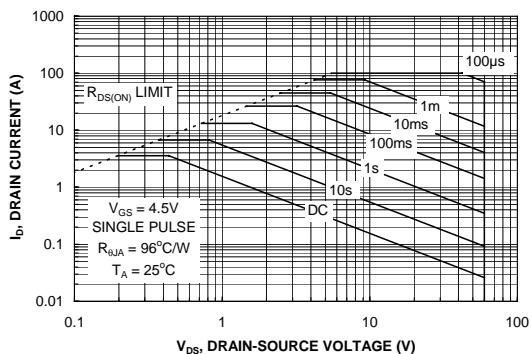


Figure 9. Maximum Safe Operating Area.

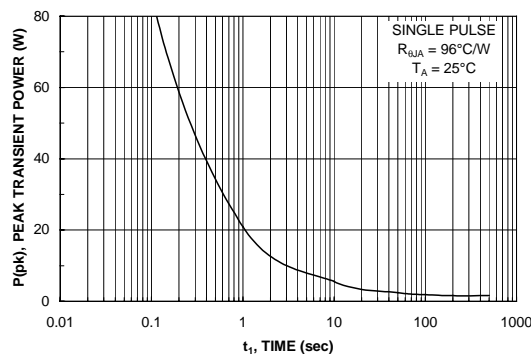


Figure 10. Single Pulse Maximum Power Dissipation.

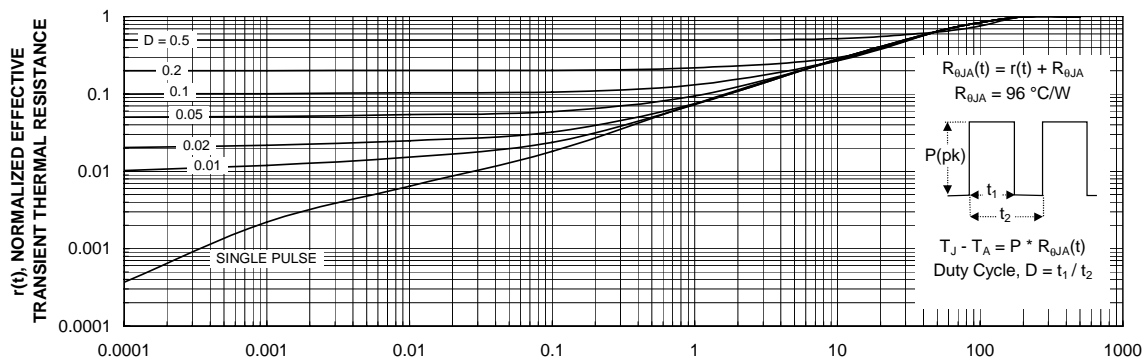
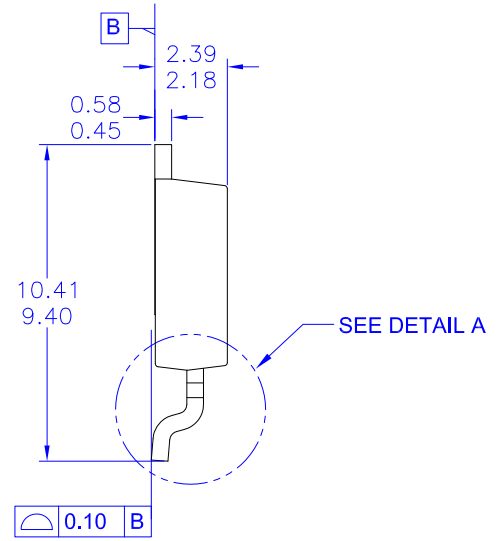
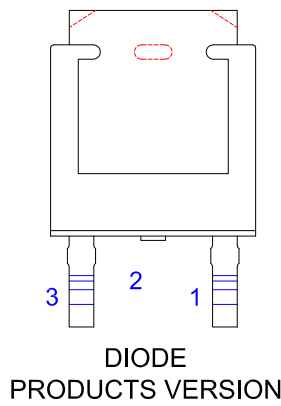
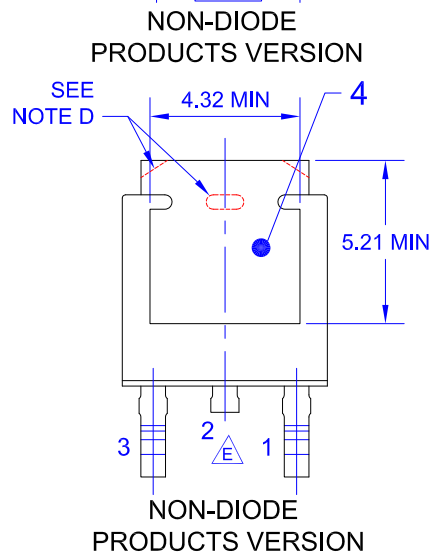
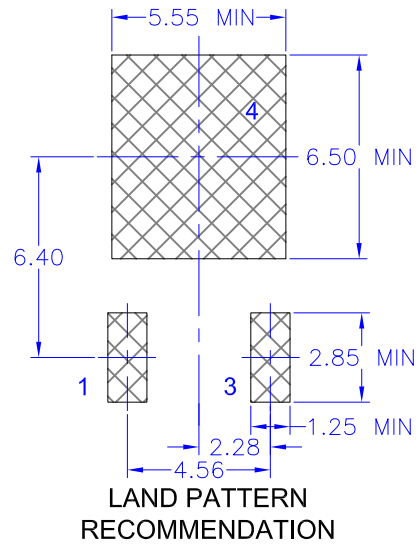
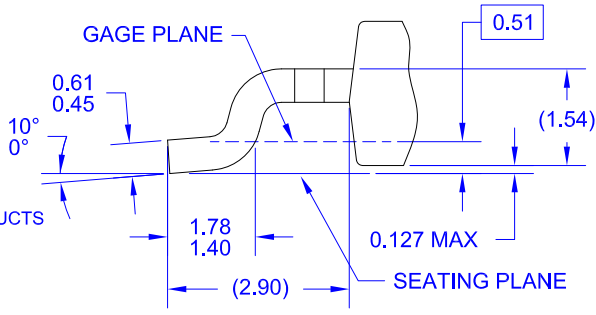


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



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 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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