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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

June 2014

FDMC510P

P-Channel PowerTrench® MOSFET
-20 V, -18 A, 8.0 mΩ

Features

- Max $r_{DS(on)}$ = 8.0 mΩ at V_{GS} = -4.5 V, I_D = -12 A

- Max $r_{DS(on)}$ = 9.8 mΩ at V_{GS} = -2.5 V, I_D = -10 A

- Max $r_{DS(on)}$ = 13 mΩ at V_{GS} = -1.8 V, I_D = -9.3 A

- Max $r_{DS(on)}$ = 17 mΩ at V_{GS} = -1.5 V, I_D = -8.3 A

- High performance trench technology for extremely low $r_{DS(on)}$

- High power and current handling capability in a widely used surface mount package

- 100% UIL Tested

- Termination is Lead-free and RoHS Compliant

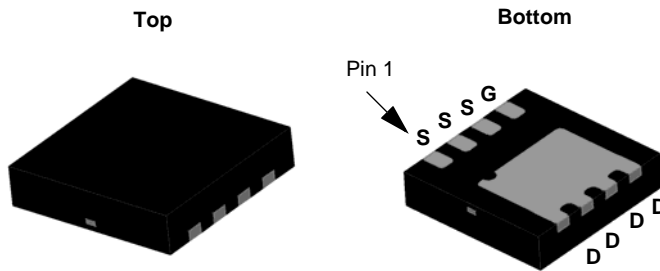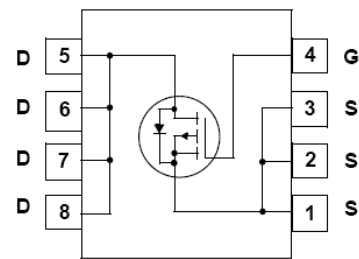- HBM ESD capability level >2 KV typical (Note 4)

General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for $r_{DS(ON)}$, switching performance and ruggedness.

Applications

- Battery Management

- Load Switch

MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-20	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Current -Continuous	T_C = 25 °C		-18	A
	-Continuous	T_A = 25 °C	(Note 1a)	-12	
	-Pulsed			-50	
E_{AS}	Single Pulse Avalanche Energy			37	mJ
P_D	Power Dissipation	T_C = 25 °C		41	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC510P	FDMC510P	MLP 3.3X3.3	13 "	12 mm	3000 units

www.fairchildsemi.com

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -12 A		6.4	8.0	mΩ
		V_{GS} = -2.5 V, I_D = -10 A		7.6	9.8	
		V_{GS} = -1.8 V, I_D = -9.3 A		9.2	13	
		V_{GS} = -1.5 V, I_D = -8.3 A		11	17	
		V_{GS} = -4.5 V, I_D = -12 A, T_J = 125 °C		8.5	12	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -12 A		75		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz		5910	7860	pF
C_{oss}	Output Capacitance			840	1120	pF
C_{rss}	Reverse Transfer Capacitance			738	1110	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -12 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		15	27	ns
t_r	Rise Time			34	55	ns
$t_{d(off)}$	Turn-Off Delay Time			338	540	ns
t_f	Fall Time			170	272	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -4.5 V, V_{DD} = -10 V, I_D = -12 A		83	116	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -2.5 V, V_{DD} = -10 V, I_D = -12 A		50	70	nC
Q_{gs}	Gate to Source Charge			6.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			20.4		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -12 A (Note 2)		-0.70	-1.3	V
		V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.53	-1.2	
t_{rr}	Reverse Recovery Time	I_F = -12 A, di/dt = 100 A/μs		35	57	ns
Q_{rr}	Reverse Recovery Charge			20	32	nC

Notes**:**
1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3: Starting T_J = 25°C; P-Ch: L = 3 mH, I_{AS} = -5 A, V_{DD} = -20 V, V_{GS} = -4.5 V.
4: No gate overvoltage rating is implied.

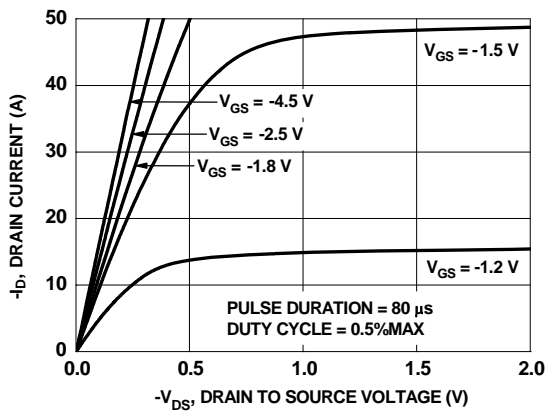## Typical Characteristics T_J = 25 °C unless otherwise noted

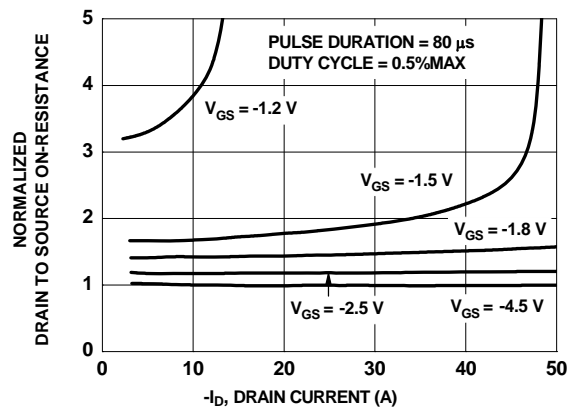**Figure 1. On Region Characteristics**

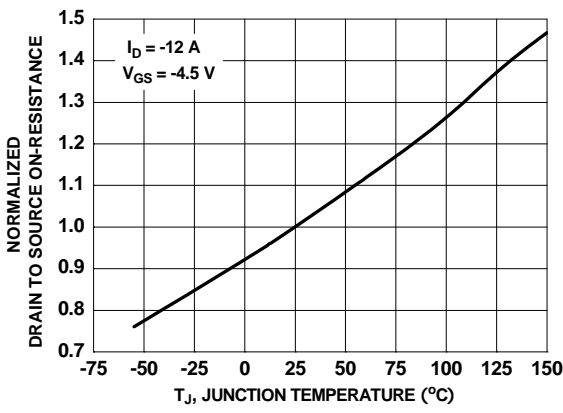**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**

Figure 3. Normalized On Resistance vs. Junction Temperature
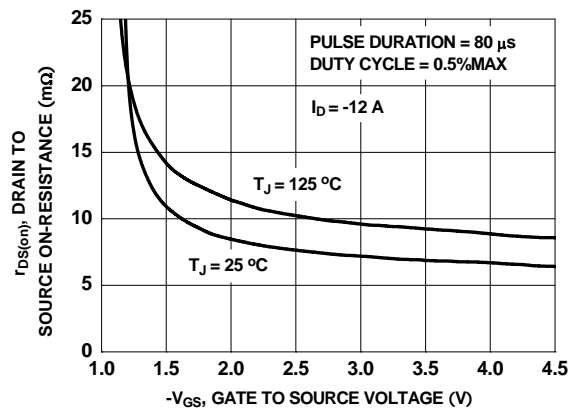
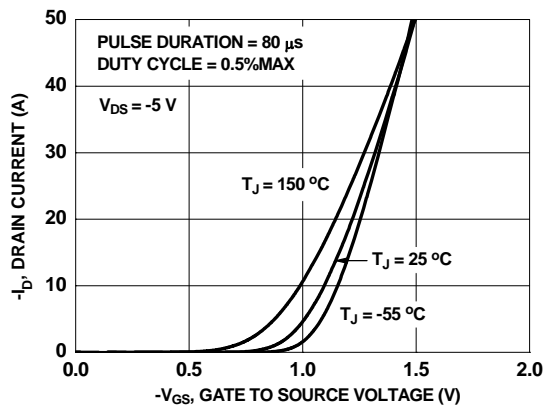**Figure 4. On-Resistance vs. Gate to Source Voltage**
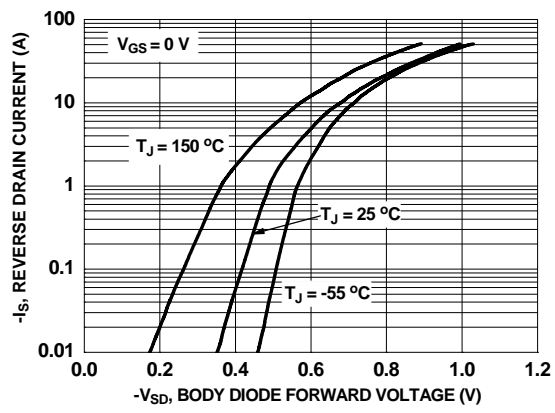
Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

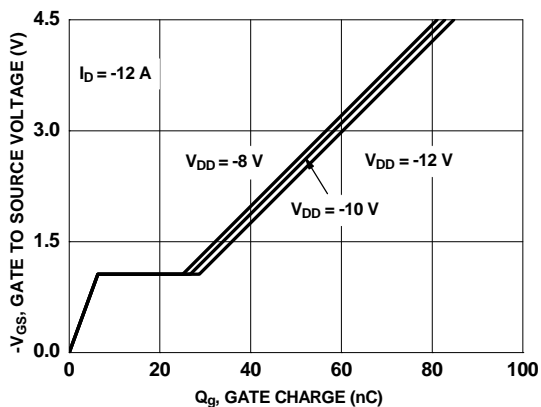## Typical Characteristics T_J = 25 °C unless otherwise noted

Figure 7. Gate Charge Characteristics
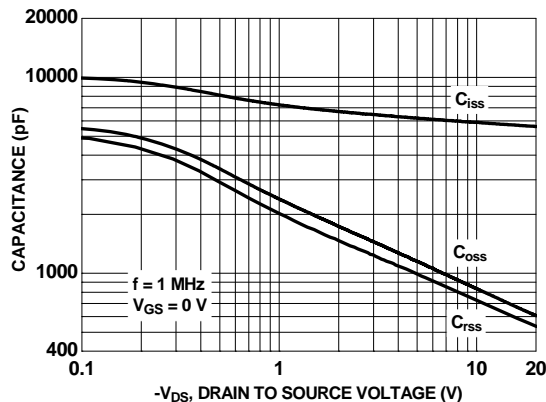
Figure 8. Capacitance vs. Drain to Source Voltage
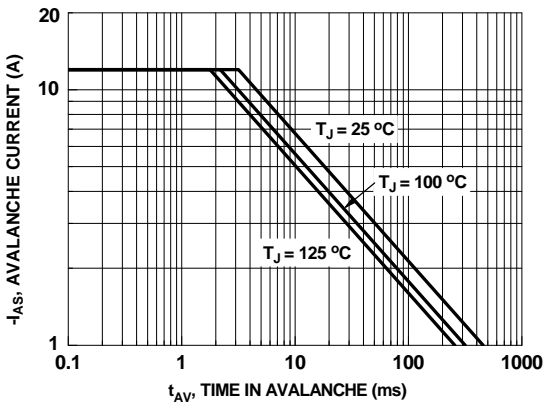
Figure 9. Unclamped Inductive Switching Capability
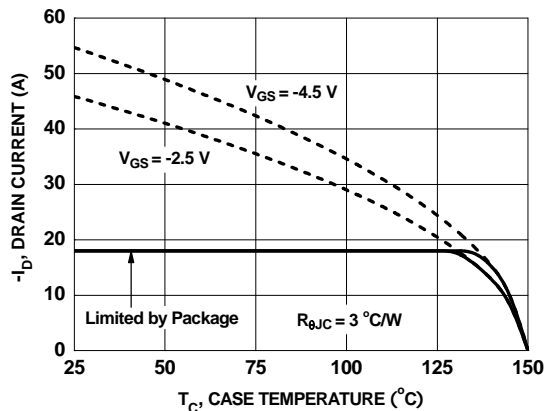
Figure 10. Maximum Continuous Drain Current vs. Case Temperature
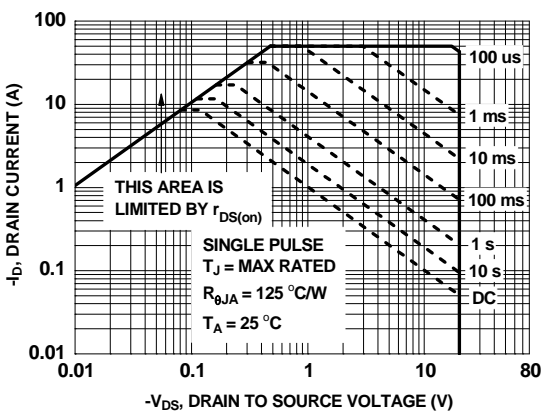
Figure 11. Forward Bias Safe Operating Area
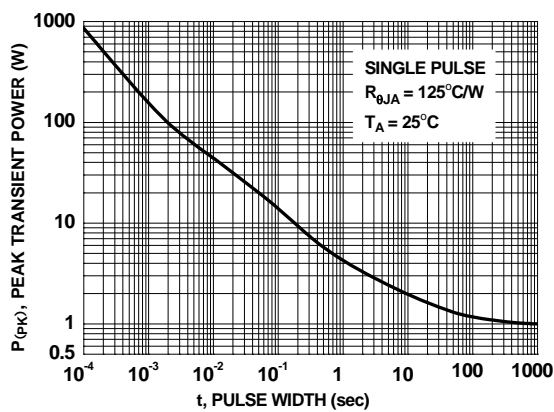
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted
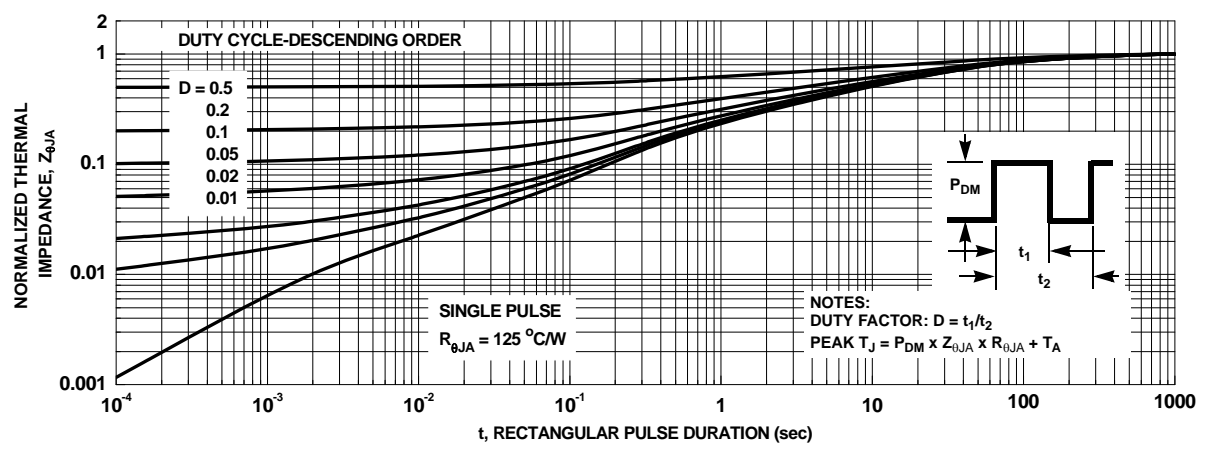
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TOP VIEW

2X ⟨ 0.05 │ C

3.30 | A │ B

3.30

⟨ 0.05 │ C
2X

PIN#1 IDENT

SIDE VIEW

// │ 0.10 │ C

0.75±0.05

0.15±0.05

⟨ 0.08 │ C

0.025±0.025
SEATING
PLANE

C

BOTTOM VIEW

3.30±0.05

2.27±0.05

PIN #1 IDENT

(0.79)

(0.50)4X

0.50±0.05(4X)

1   4

(0.35)

(1.15)

3.30±0.05

R0.15

2.00±0.05

0.30±0.05(3X)

8   5

0.35±0.05(8X)

0.65

1.95

⌖ │ 0.10 Ⓜ │ C │ A │ B
⌖ │ 0.05 Ⓜ │ C

RECOMMENDED LAND PATTERN

(3.40)

2.37

8   5

0.45(4X)

2.15

(1.70)

(0.40)

(0.65)

KEEP OUT
AREA

0.70(4X)

0.65   1   4

0.42(8X)

1.95
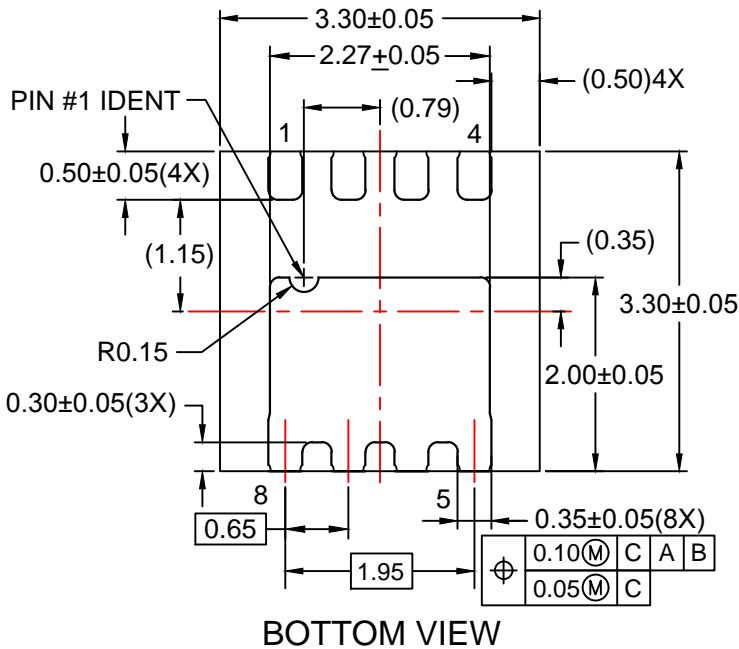
NOTES:

A. DOES NOT CONFORM TO JEDEC
   REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
   ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS
   EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

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PUBLICATION ORDERING INFORMATION