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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

June 2014

# FDMC7692S

## N-Channel PowerTrench® SyncFET™

**30 V, 18 A, 9.3 mΩ**

### Features

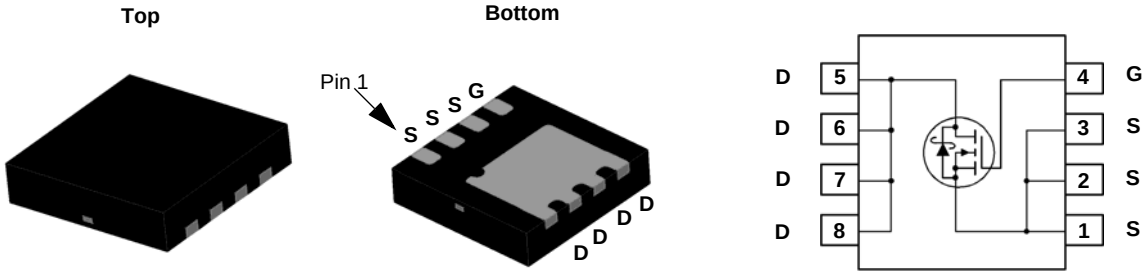
- Max $r_{DS(on)}$ = 9.3 mΩ at $V_{GS}$ = 10 V, $I_D$ = 12.5 A
- Max $r_{DS(on)}$ = 13.6 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 10.4 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

### General Description

This FDMC7692S is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery packs.

### Applications

- DC - DC Buck Converters
- Notebook DC - DC application




**MLP 3.3x3.3**

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | 18 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 12.5 | |
| | -Pulsed | | | 45 | |
| $E_{AS}$ | Sinlge Pulse Avalanche Energy | | (Note 3) | 21 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 27 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 4.7 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | °C/W |

### Package Marking and Ordering Information

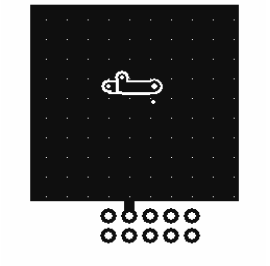
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMC7692S | FDMC7692S | MLP 3.3X3.3 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

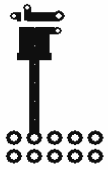
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 10 mA, referenced to 25 °C | | 16 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 500 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA | 1.2 | 2.0 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 10 mA, referenced to 25 °C | | -5 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 12.5 A | | 7.8 | 9.3 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 10.4 A | | 10.8 | 13.6 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 12.5 A, $T_J$ = 125 °C | | 9.6 | 13.0 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 12.5 A | | 62 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | | 1040 | 1385 | pF |
| $C_{oss}$ | Output Capacitance | | | 445 | 590 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 40 | 60 | pF |
| $R_g$ | Gate Resistance | | | 1.1 | 2.9 | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 12.5 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 9 | 17 | ns |
| $t_r$ | Rise Time | | | 3 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 19 | 34 | ns |
| $t_f$ | Fall Time | | | 3 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 15 V, $I_D$ = 12.5 A | | 16 | 23 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V; $V_{DD}$ = 15 V, $I_D$ = 12.5 A | | 8 | 10 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD}$ = 15 V, $I_D$ = 12.5 A | | 4 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 15 V, $I_D$ = 12.5 A | | 2 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 12.5 A (Note 2) | | 0.9 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 0.9 A (Note 2) | | 0.5 | 0.7 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 12.5 A, di/dt = 300 A/μs | | 21 | 33 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 16 | 29 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. $E_{AS}$ of 21 mJ is based on starting $T_J$ = 25 °C, L = 0.3 mH, $I_{AS}$ = 12.0 A, $V_{DD}$ = 27 V, $V_{GS}$ = 10 V. 100% test at L = 3 mH, $I_{AS}$ = 3.2 A .

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

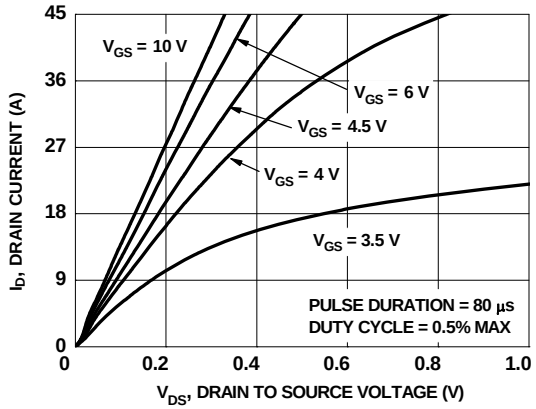



**Figure 1. On-Region Characteristics**

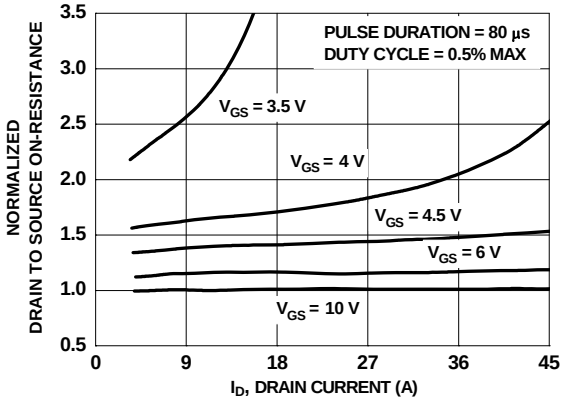



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

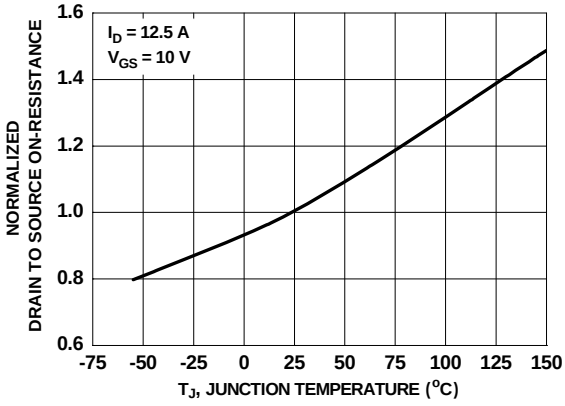



**Figure 3. Normalized On-Resistance vs Junction Temperature**

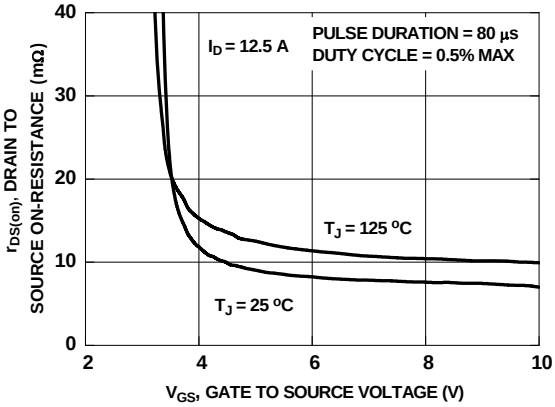



**Figure 4. On-Resistance vs Gate to Source Voltage**

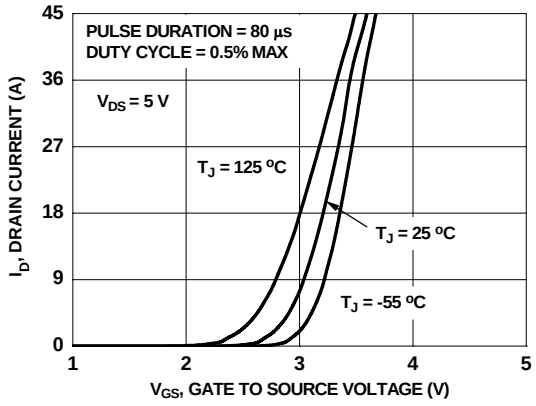



**Figure 5. Transfer Characteristics**

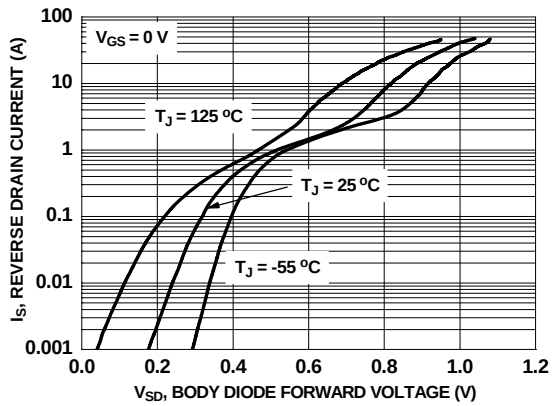



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

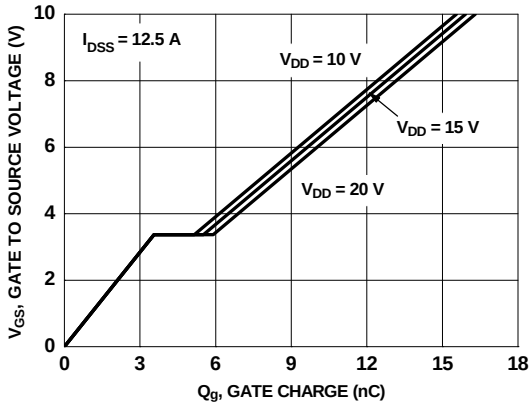



**Figure 7. Gate Charge Characteristics**

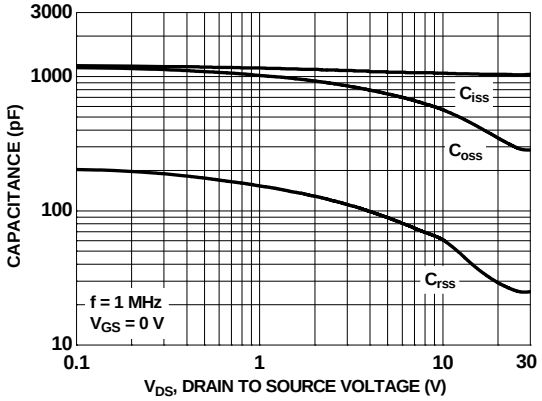



**Figure 8. Capacitance vs Drain to Source Voltage**

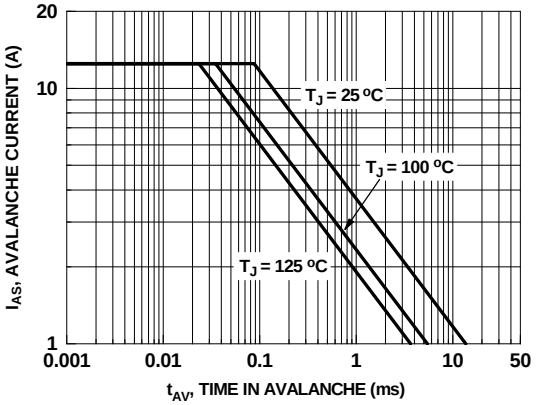



**Figure 9. Unclamped Inductive Switching Capability**

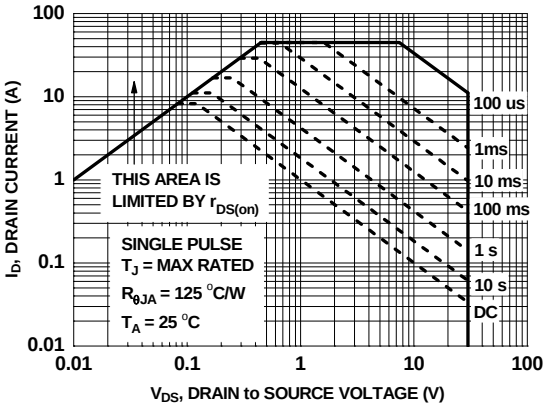



**Figure 10. Forward Bias Safe Operating Area**

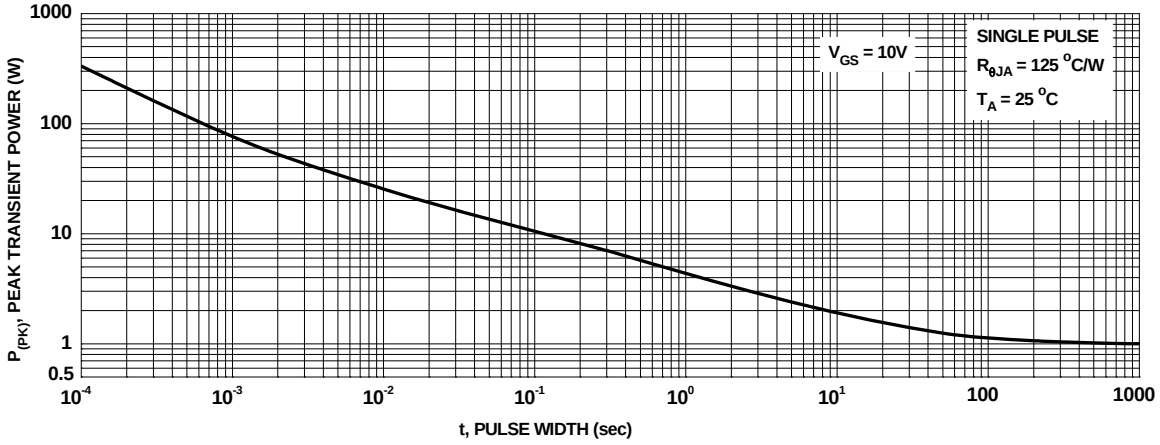



**Figure 11. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

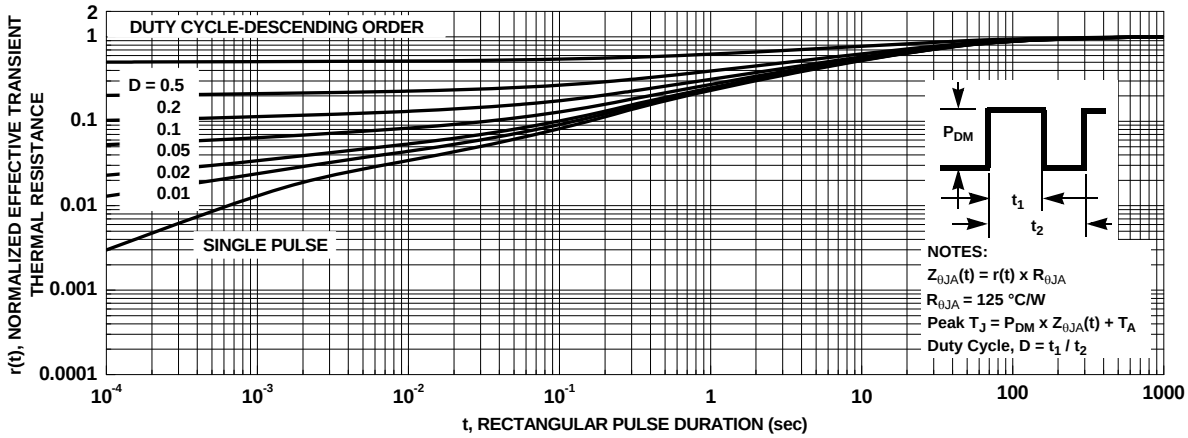



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 13 shows the reverse recovery characteristic of the FDMC7692S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

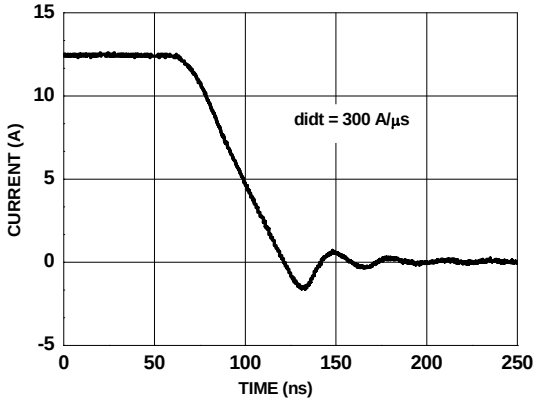



**Figure 13. SyncFET body diode reverse recovery characteristic**

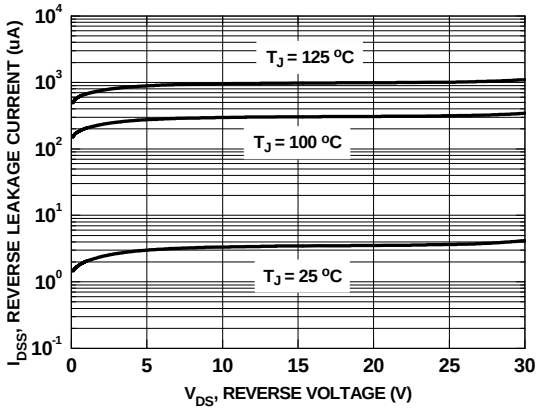
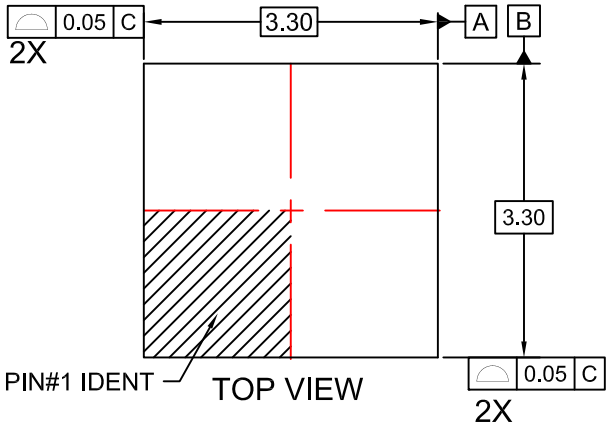
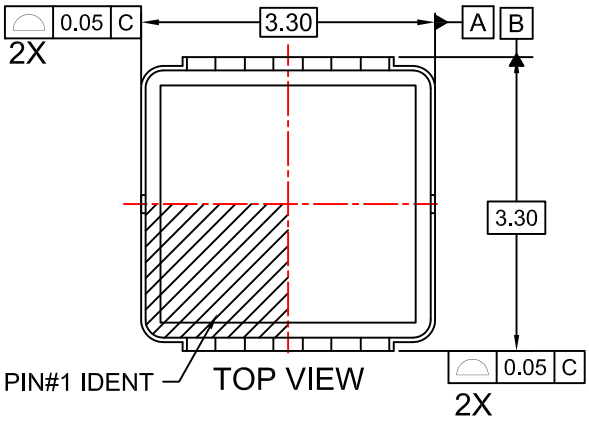
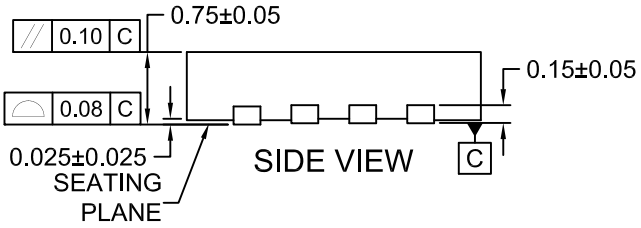
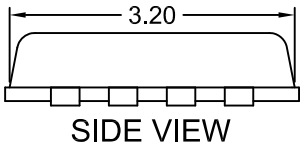


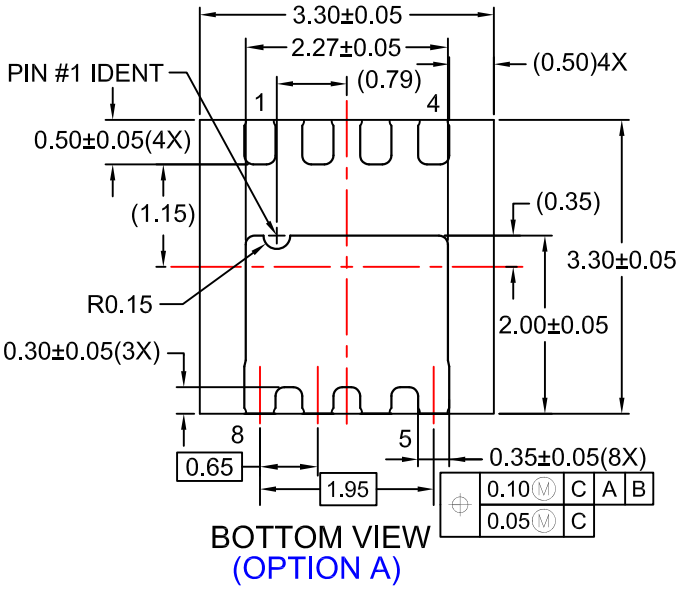

**Figure 14. SyncFET body diode reverse leakage versus drain-source voltage**

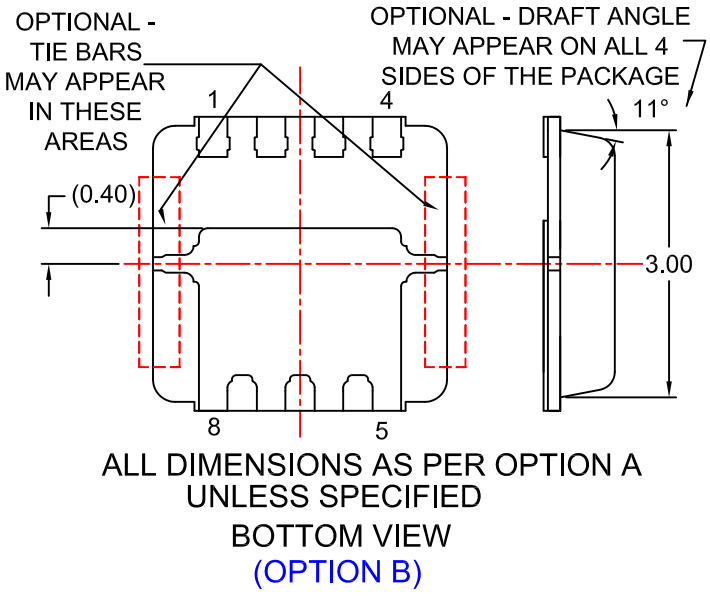

0.05 C
2X
3.30
A
B
3.30
PIN#1 IDENT
TOP VIEW
0.05 C
2X

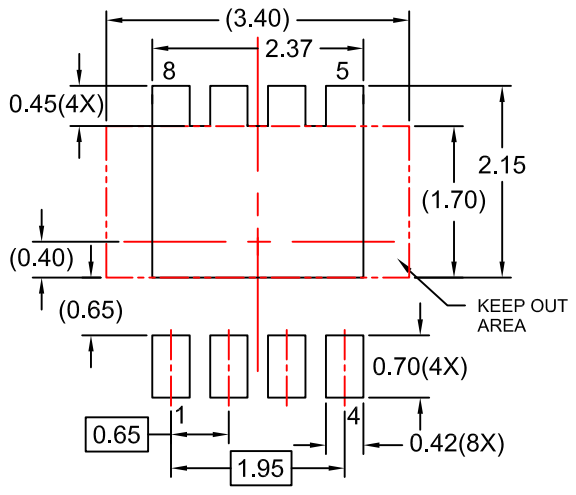

0.05 C
2X
3.30
A
B
3.30
PIN#1 IDENT
TOP VIEW
0.05 C
2X


0.10 C
0.75±0.05
0.08 C
0.15±0.05
0.025±0.025
SEATING
PLANE
SIDE VIEW
C

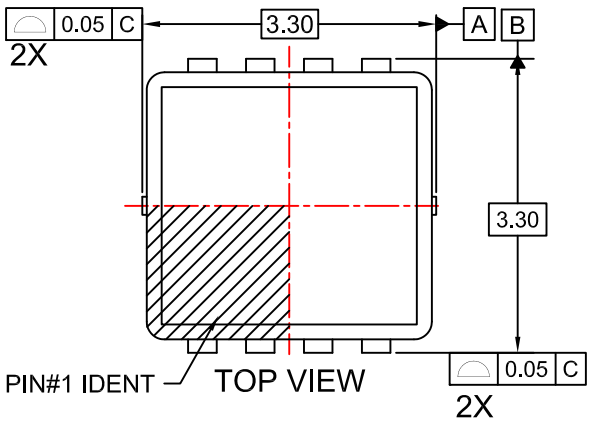

3.20
SIDE VIEW

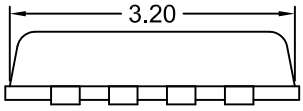

3.30±0.05
2.27±0.05
(0.79)
(0.50)4X
PIN #1 IDENT
1
4
0.50±0.05(4X)
(1.15)
(0.35)
3.30±0.05
R0.15
2.00±0.05
0.30±0.05(3X)
8
5
0.65
1.95
0.35±0.05(8X)
0.10 M C A B
0.05 M C
BOTTOM VIEW
(OPTION A)


OPTIONAL -
TIE BARS
MAY APPEAR
IN THESE
AREAS
OPTIONAL - DRAFT ANGLE
MAY APPEAR ON ALL 4
SIDES OF THE PACKAGE
1
4
11°
(0.40)
3.00
8
5
ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED
BOTTOM VIEW
(OPTION B)

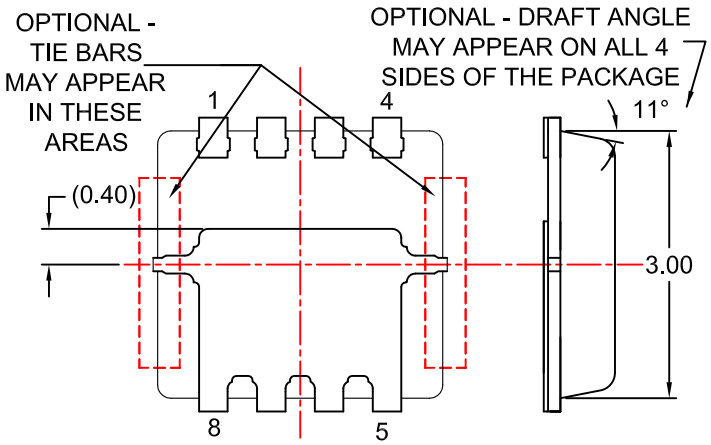

(3.40)
2.37
8
5
0.45(4X)
2.15
(1.70)
(0.40)
(0.65)
KEEP OUT
AREA
0.70(4X)
0.65
1
4
0.42(8X)
1.95
RECOMMENDED LAND PATTERN

FAIRCHILD.




SIDE VIEW



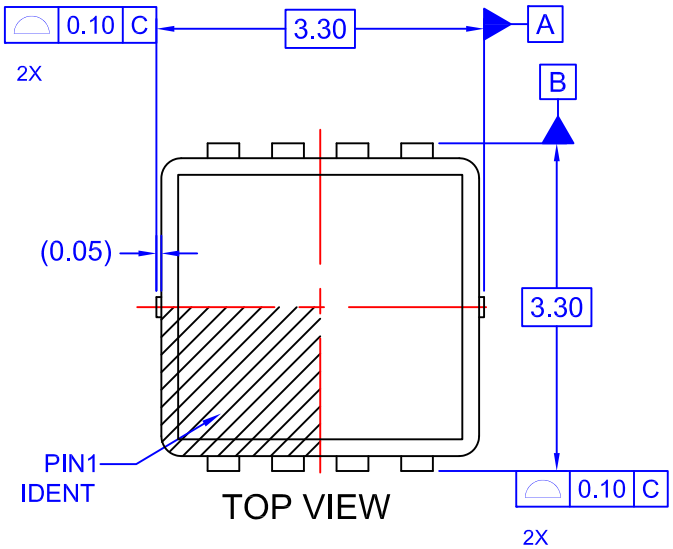

ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

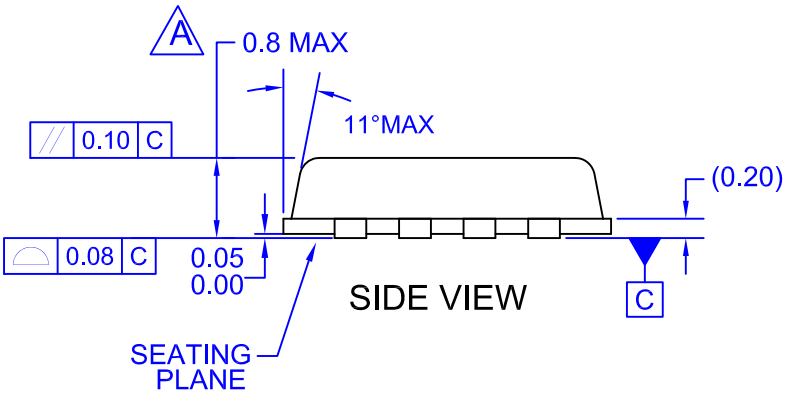
NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
F. DRAWING FILENAME: MKT-MLP08Wrev3.
G. OPTION A - SAWN MLP, OPTIONS B & C - PUNCH MLP.

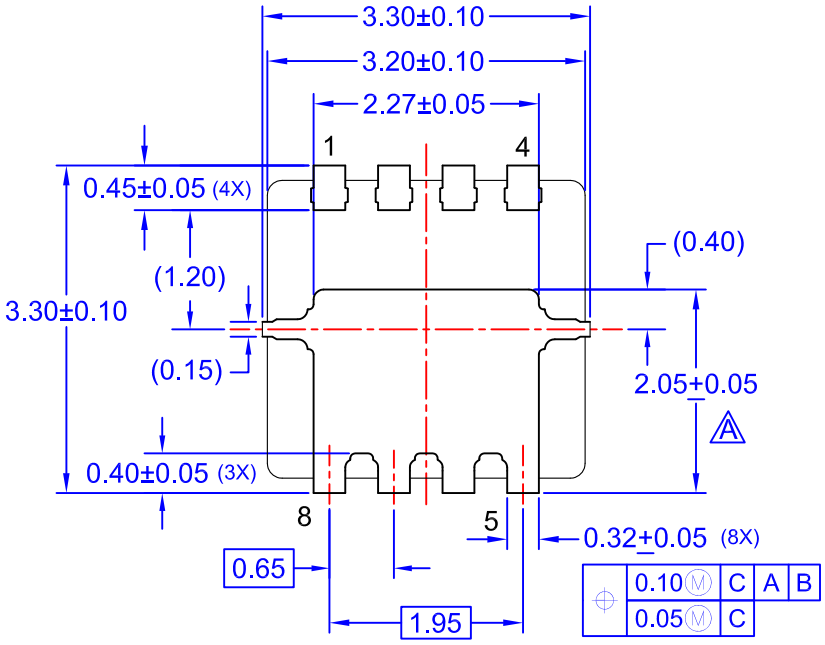
FAIRCHILD.



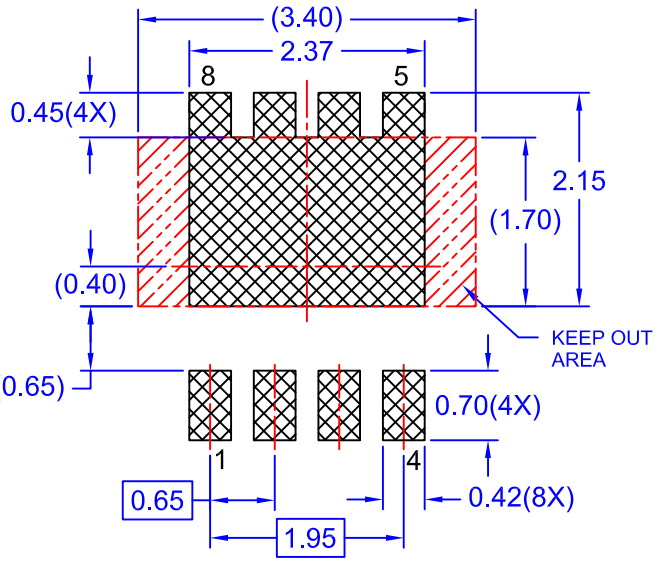

TOP VIEW




SIDE VIEW




BOTTOM VIEW

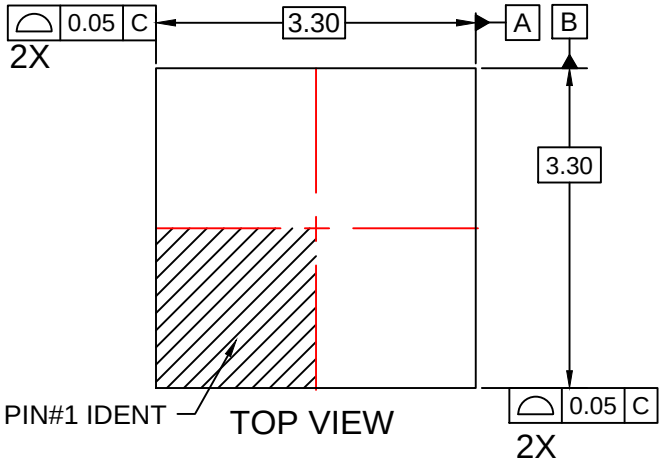


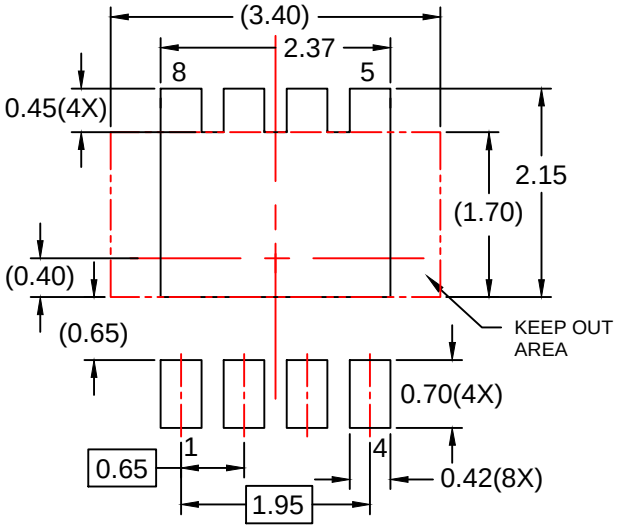

RECOMMENDED LAND PATTERN

NOTES:

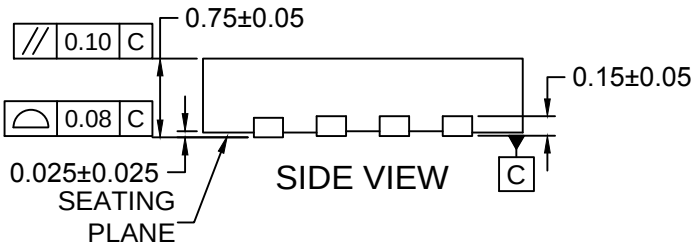
A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
H. DRAWING FILENAME: MKT-MLP08Trev4.
I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

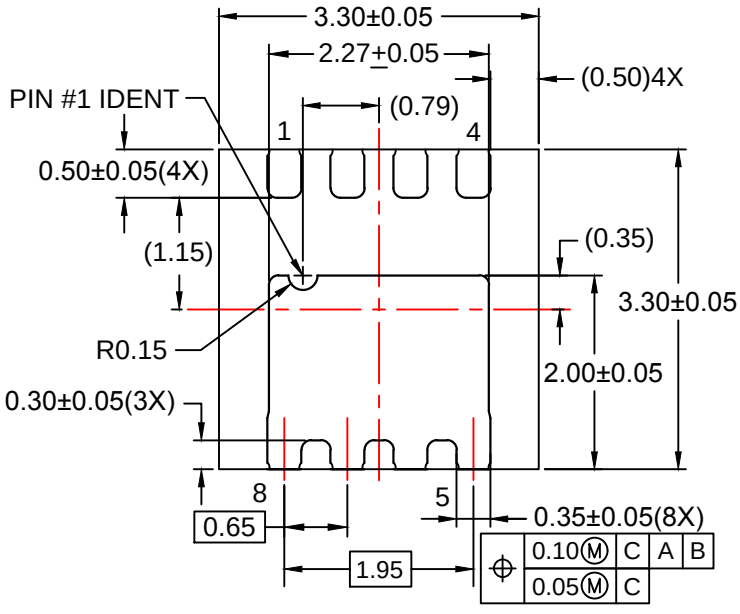
FAIRCHILD™




RECOMMENDED LAND PATTERN




BOTTOM VIEW

## NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

FAIRCHILD.

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