

# MOSFET - Dual N-Channel, Asymmetric, POWER TRENCH<sup>®</sup> Power Clip 30 V



ON Semiconductor<sup>®</sup>

[www.onsemi.com](http://www.onsemi.com)

## FDPC5030SG

### General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET<sup>™</sup> (Q2) have been designed to provide optimal power efficiency.

### Features

Q1: N-Channel

- Max  $R_{DS(on)}$  = 5.0 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 17 A
- Max  $R_{DS(on)}$  = 6.5 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 14 A

Q2: N-Channel

- Max  $R_{DS(on)}$  = 2.4 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 25 A
- Max  $R_{DS(on)}$  = 3.0 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses.
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing.
- RoHS Compliant

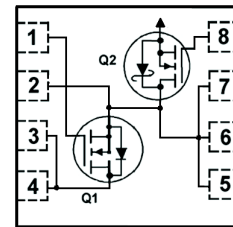
### Applications

- Computing
- Communications
- General Purpose Point of Load

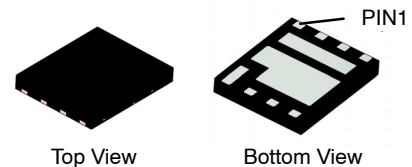
Table 1. PIN DESCRIPTION

Pin	Name	Description
1	HSG	High Side Gate
2	GR	Gate Return
3, 4, 10	V+(HSD)	High Side Drain
5, 6, 7	SW	Switching Node, Low Side Drain
8	LSG	Low Side Gate
9	GND (LSS)	Low Side Source

### ELECTRICAL CONNECTION

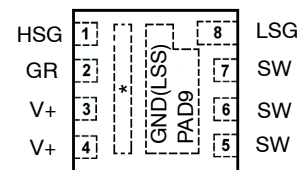


N-Channel MOSFET



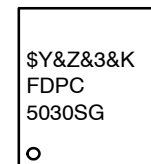
Power Clip 56  
(PQFN8 5x6)  
CASE 483AR

### PIN ASSIGNMENT



\*PAD10 V+(HSD)

### MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Numeric Date Code
- &K = Lot Code
- FDPC5030SG = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDPC5030SG

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit
$V_{DS}$	Drain to Source Voltage	30	30	V
$Bvdsst$	$Bvdsst$ (Transient) < 100 ns	36	36	V
$V_{GS}$	Gate to Source Voltage	+/-20	+/-12	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ ) (Note 5)	56	84	A
	– Continuous ( $T_C = 100^\circ\text{C}$ ) (Note 5)	35	53	
	– Continuous ( $T_A = 25^\circ\text{C}$ )	17 (Note 1a)	25 (Note 1b)	
	– Pulsed ( $T_A = 25^\circ\text{C}$ ) (Note 4)	227	503	
$E_{AS}$	Single Pulsed Avalanche Energy (Note 3)	54	96	mJ
$P_D$	Power Dissipation for Single Operation ( $T_C = 25^\circ\text{C}$ ) ( $T_A = 25^\circ\text{C}$ ) ( $T_A = 25^\circ\text{C}$ )	23 2.1 (Note 1a) 1.0 (Note 1c)	25 2.3 (Note 1b) 1.1 (Note 1d)	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.6	4.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 1a)	55 (Note 1b)	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 1c)	120 (Note 1d)	$^\circ\text{C}/\text{W}$

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Top Marking	Package	Reel Size	Tape Width	Quantity
FDPC5030SG	FDPC5030SG	Power Clip 56	13"	12 mm	3,000 Units

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
--------	-----------	-----------------	------	-----	-----	-----	------

### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	Q1 Q2	30 30	– –	– –	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 10 \text{ mA}$ , referenced to $25^\circ\text{C}$	Q1 Q2	– –	15 16	– –	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2	– –	– –	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2	– –	– –	$\pm 100$ $\pm 100$	nA nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	Q1 Q2	1.0 1.0	1.7 1.6	3.0 3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 1 \mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = 10 \text{ mA}$ , referenced to $25^\circ\text{C}$	Q1 Q2	– –	–5 –3	– –	$\text{mV}/^\circ\text{C}$

# FDPC5030SG

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>							
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A, T <sub>J</sub> = 125°C	Q1	–	4.1	5.0	mΩ
		Q2	–	5.4	6.5		
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 22 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125°C	Q1	–	1.9	2.4	
			Q2	–	2.4	3.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 17 A	Q1	–	93	–	S
		V <sub>DS</sub> = 5 V, I <sub>D</sub> = 25 A	Q2	–	139	–	

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	Q1: V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz Q2: V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Q1	–	1224	1715	pF
			Q2	–	2730	3825	
C <sub>oss</sub>	Output Capacitance		Q1	–	397	560	pF
			Q2	–	801	1125	
C <sub>rss</sub>	Reverse Transfer Capacitance		Q1	–	42	60	pF
			Q2	–	72	100	
R <sub>g</sub>	Gate Resistance		Q1	0.1	0.5	1.5	Ω
			Q2	0.1	1.1	2.2	

## SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A, R <sub>GEN</sub> = 6 Ω Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25 A, R <sub>GEN</sub> = 6 Ω	Q1	–	8	16	ns
			Q2	–	10	19	
t <sub>r</sub>	Rise Time		Q1	–	2	10	ns
			Q2	–	4	10	
t <sub>d(off)</sub>	Turn-Off Delay Time		Q1	–	18	33	ns
			Q2	–	30	48	
t <sub>f</sub>	Fall Time		Q1	–	2	10	ns
			Q2	–	3	10	
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25 A	Q1	–	17	24	nC
			Q2	–	39	55	
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25 A	Q1	–	8	11	nC
			Q2	–	18	26	
Q <sub>gs</sub>	Gate to Source Gate Charge	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25 A	Q1	–	3.1	–	nC
			Q2	–	6.1	–	
Q <sub>gd</sub>	Gate to Drain “Miller” Charge	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25 A	Q1	–	2.0	–	nC
			Q2	–	4.3	–	

## SOURCE-DRAIN DIODE CHARACTERISTICS

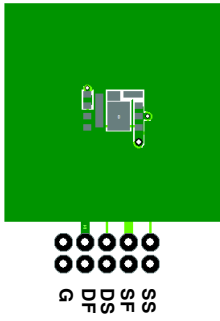
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 17 A (Note 2) V <sub>GS</sub> = 0 V, I <sub>S</sub> = 25 A (Note 2)	Q1	–	0.8	1.2	V
			Q2	–	0.8	1.2	
t <sub>rr</sub>	Reverse Recovery Time	Q1 I <sub>F</sub> = 17 A, di/dt = 100 A/μs Q2 I <sub>F</sub> = 25 A, di/dt = 230 A/μs	Q1	–	23	37	ns
			Q2	–	27	44	
Q <sub>rr</sub>	Reverse Recovery Charge		Q1	–	8	16	nC
			Q2	–	31	50	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

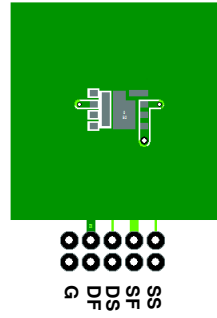
### NOTES:

1. R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R<sub>θCA</sub> is determined by the user's board design.

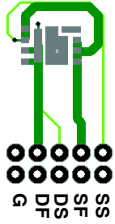
# FDPC5030SG



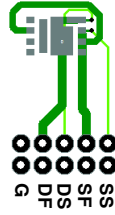
a) 60°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 55°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



c) 130°C/W when mounted on a minimum pad of 2 oz copper.



d) 120°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
3. Q1:  $E_{AS}$  of 54 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 3$  mH,  $I_{AS} = 6$  A,  $V_{DD} = 30$  V.  $V_{GS} = 10$  V, 100% tested at  $L = 0.1$  mH,  $I_{AS} = 20$  A.  
Q2:  $E_{AS}$  of 96 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 3$  mH,  $I_{AS} = 8$  A,  $V_{DD} = 30$  V.  $V_{GS} = 10$  V, 100% tested at  $L = 0.1$  mH,  $I_{AS} = 27$  A.
4. Pulsed  $I_d$  refer to Figure NO TAG and Figure NO TAG SOA graphs for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS (Q1 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

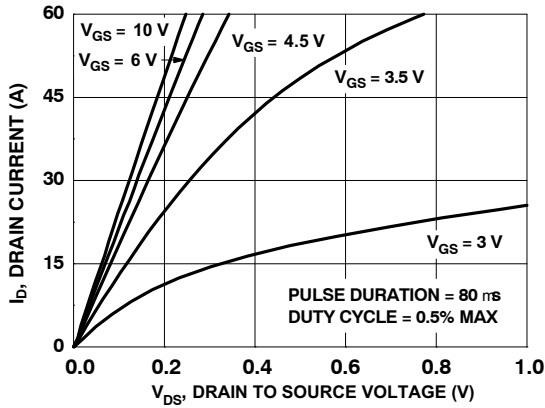


Figure 1. On Region Characteristics

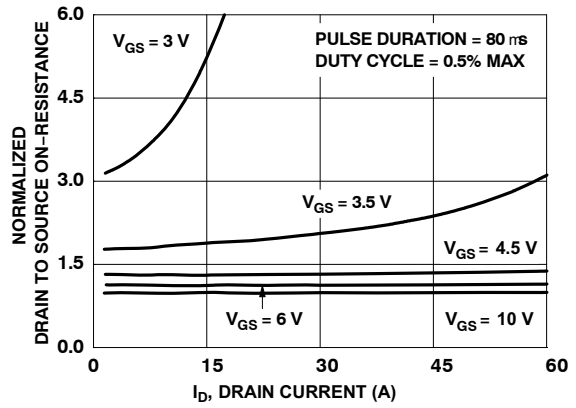


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

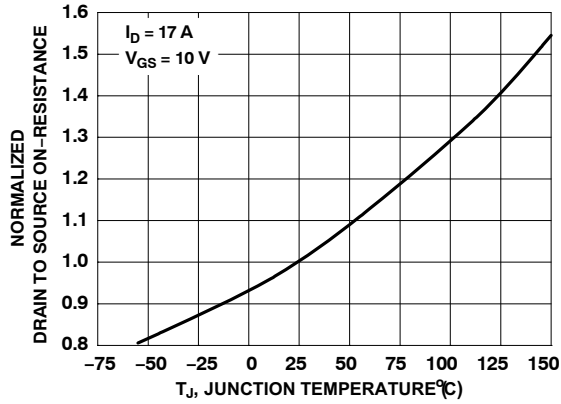


Figure 3. Normalized On Resistance vs. Junction Temperature

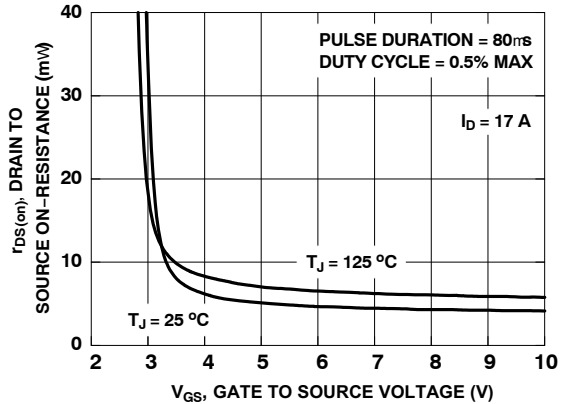


Figure 4. Normalized On Resistance vs. Gate to Source Voltage

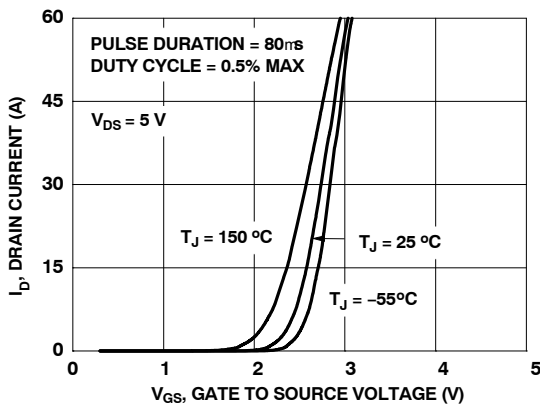


Figure 5. Transfer Characteristics

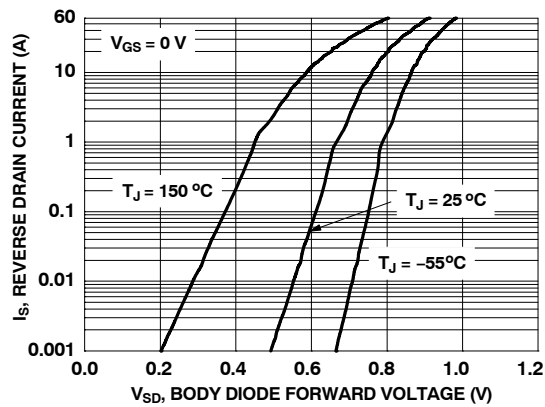


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDPC5030SG

## TYPICAL CHARACTERISTICS (Q1 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

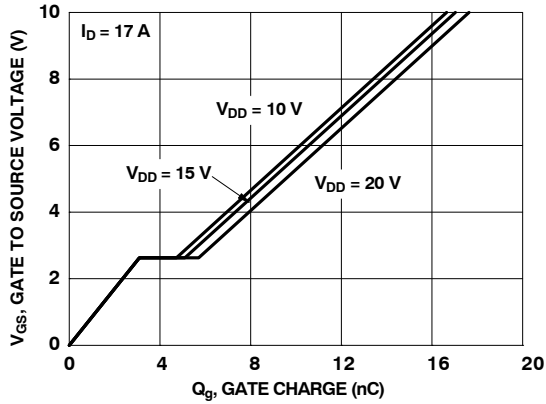


Figure 7. Gate Charge Characteristics

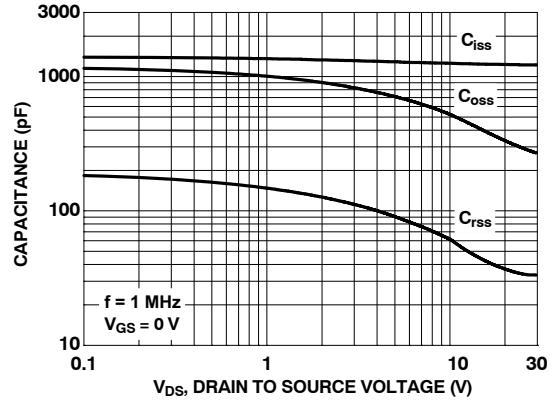


Figure 8. Capacitance vs. Drain to Source Voltage

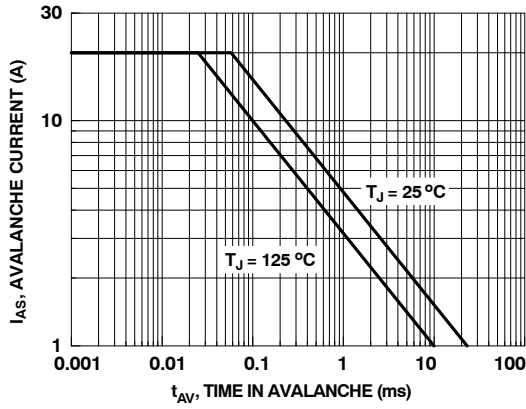


Figure 9. Unclamped Inductive Switching Capability

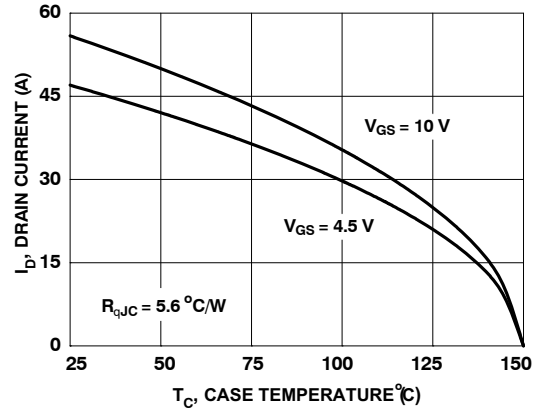


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

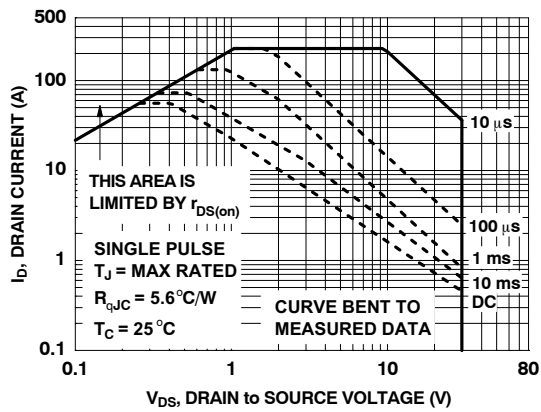


Figure 11. Forward Bias Safe Operating Area

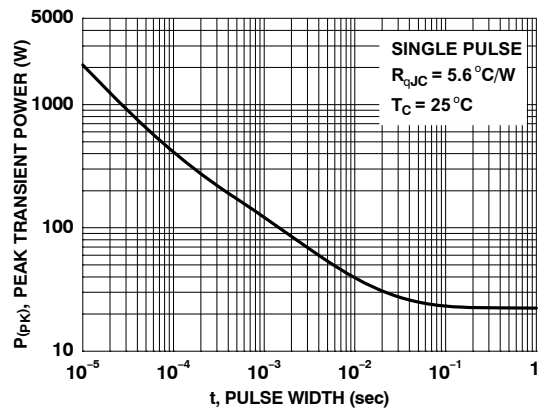


Figure 12. Single Pulse Maximum Power Dissipation

# FDPC5030SG

## TYPICAL CHARACTERISTICS (Q1 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

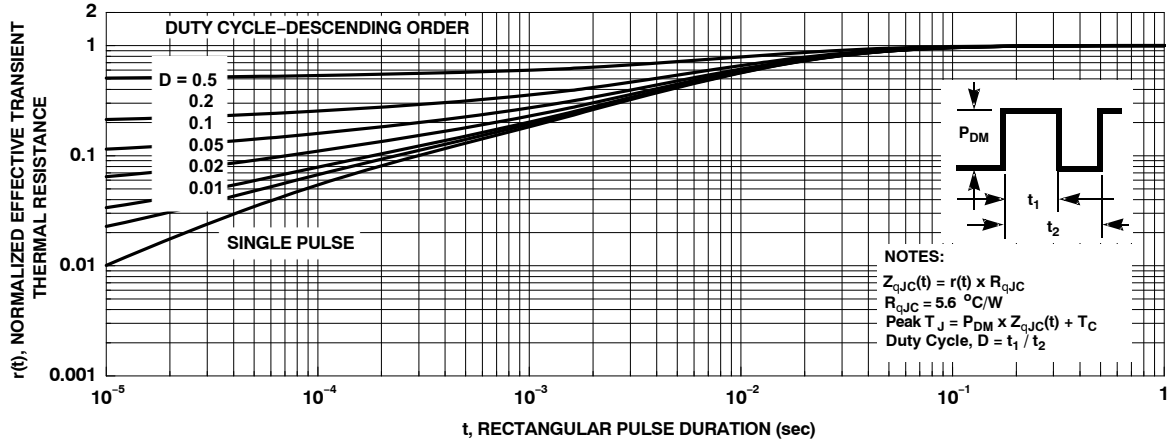


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

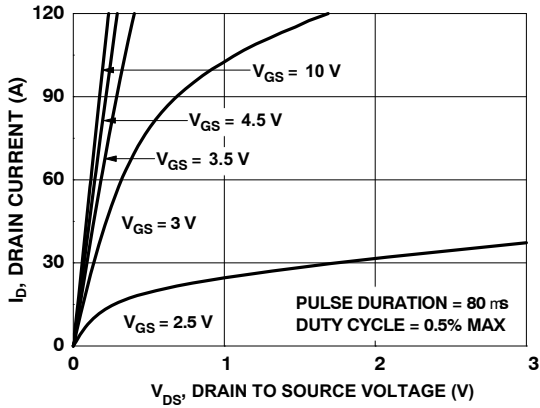


Figure 14. On-Region Characteristics

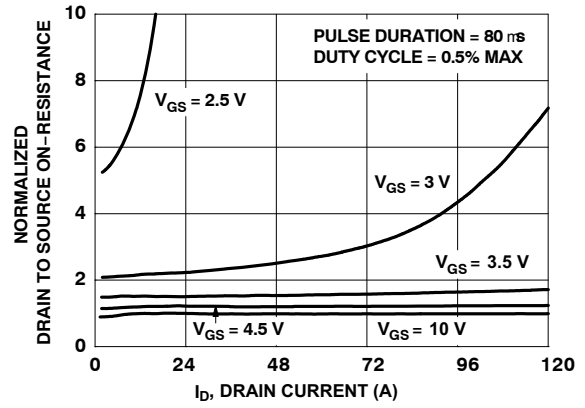


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

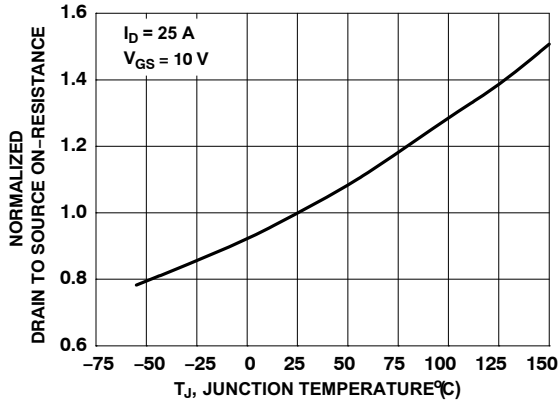


Figure 16. Normalized On-Resistance vs. Junction Temperature

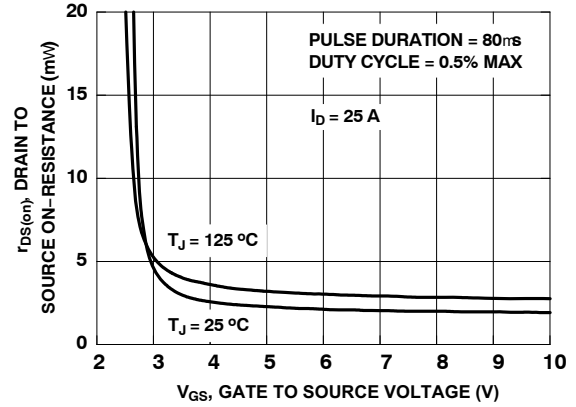


Figure 17. On-Resistance vs. Gate to Source Voltage

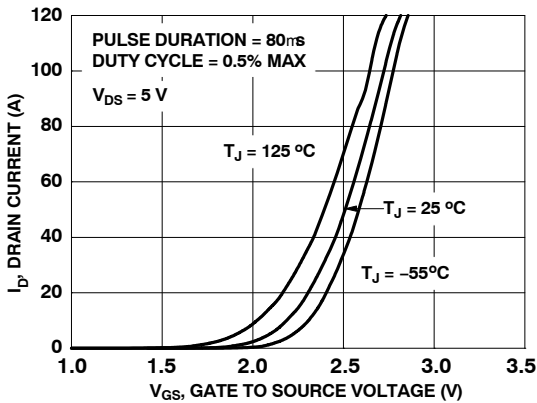


Figure 18. Transfer Characteristics

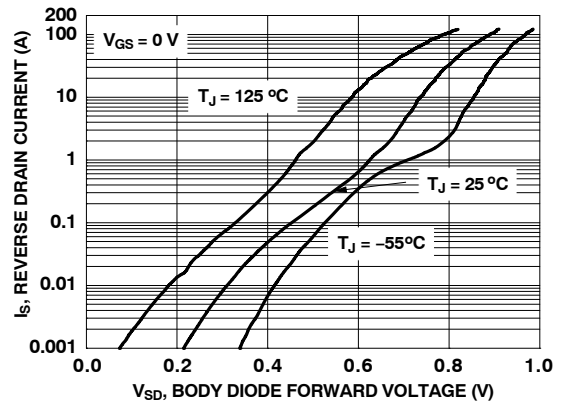


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current



# FDPC5030SG

## TYPICAL CHARACTERISTICS (Q2 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

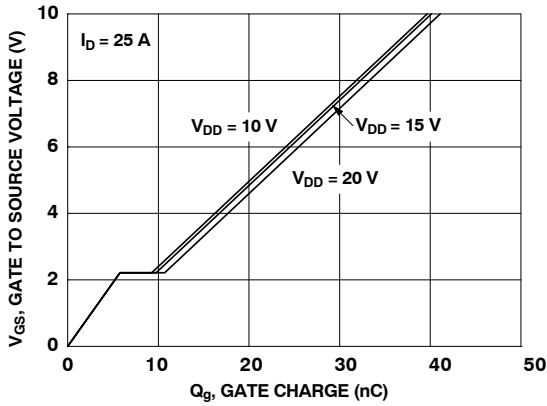


Figure 20. Gate Charge Characteristics

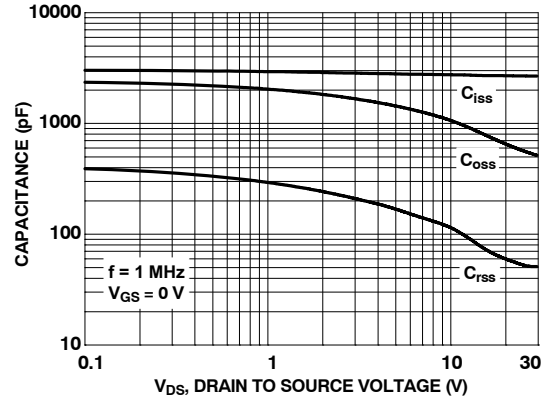


Figure 21. Capacitance vs. Drain to Source Voltage

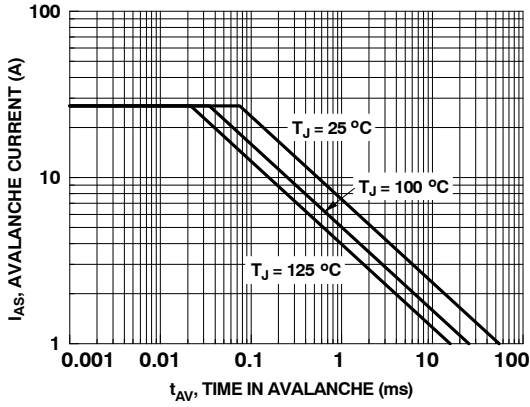


Figure 22. Unclamped Inductive Switching Capability

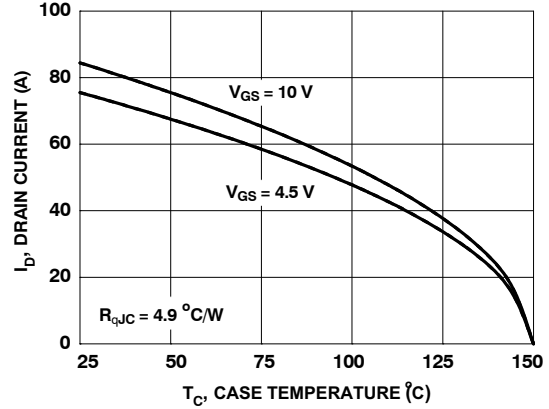


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

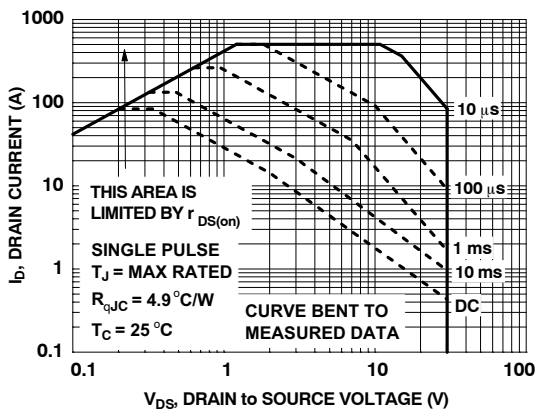


Figure 24. Forward Bias Safe Operating Area

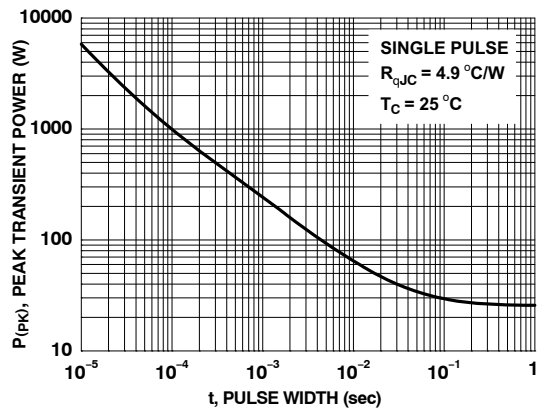


Figure 25. Single Pulse Maximum Power Dissipation

# FDPC5030SG

## TYPICAL CHARACTERISTICS (Q2 N-Channel)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

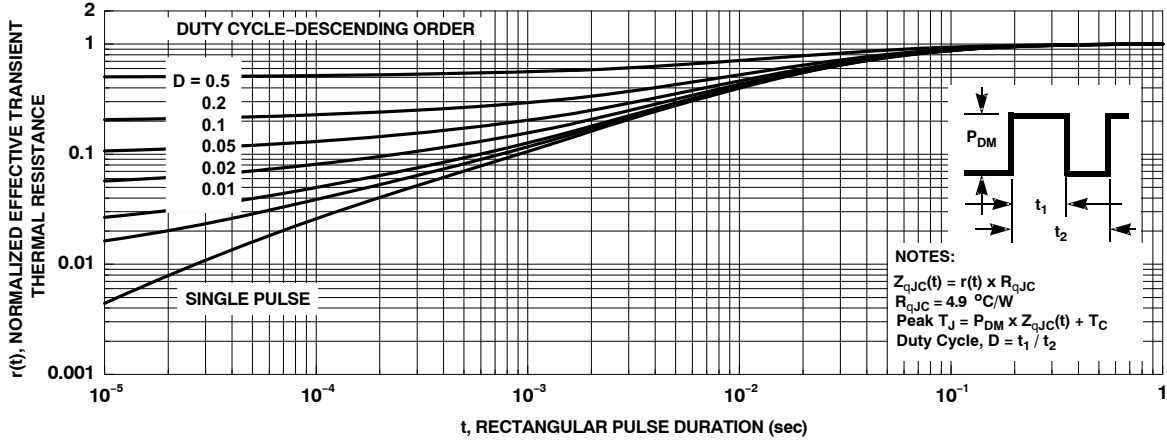


Figure 26. Junction-to-Case Transient Thermal Response Curve

# FDPC5030SG

## TYPICAL CHARACTERISTICS (continued)

### SyncFET Schottky Body Diode Characteristics

ON's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5030SG.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

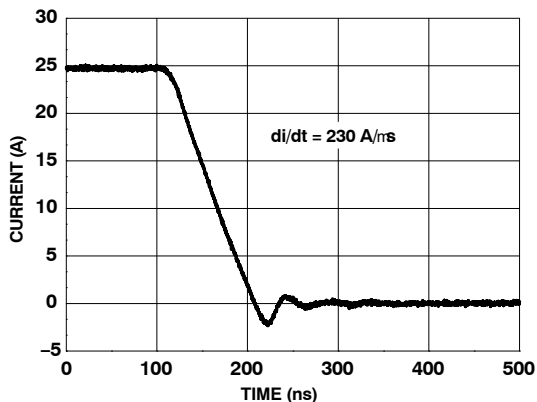


Figure 27. FDPC5030SG SyncFET™ Body Diode Reverse Recovery Characteristics

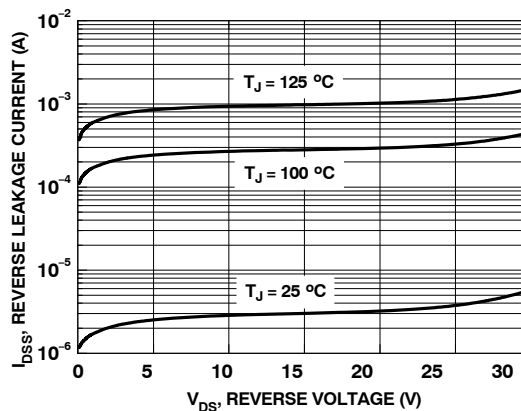
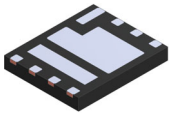


Figure 28. SyncFET™ Body Diode Reverse Leakage vs. Drain-Source Voltage

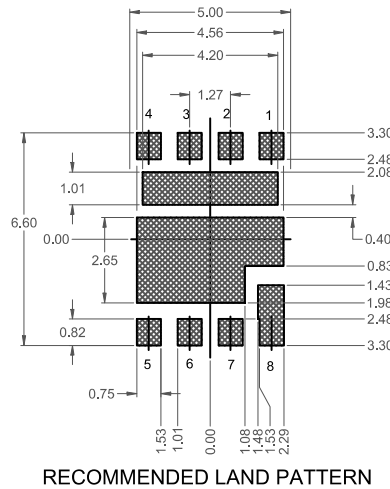
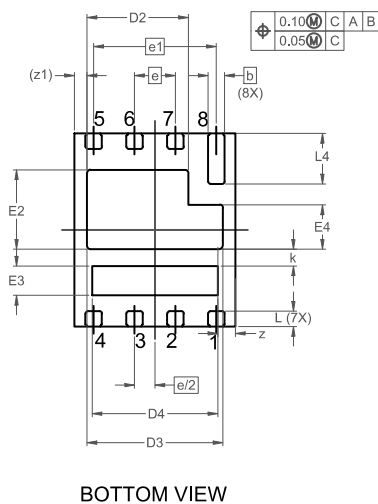
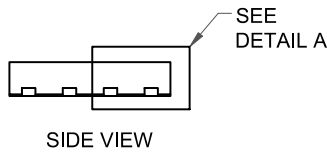
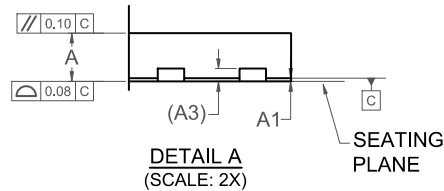
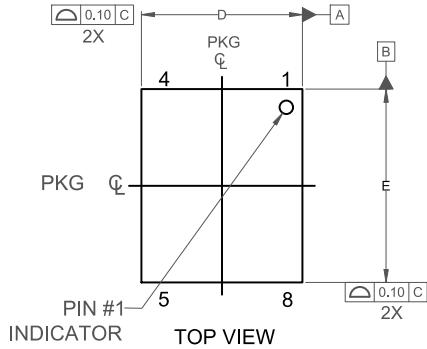
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## PQFN8 5x6, 1.27P CASE 483AR ISSUE A

DATE 21 MAY 2021



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.42	0.52	0.62
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

<b>DOCUMENT NUMBER:</b>	<b>98AON13666G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PQFN8 5x6, 1.27P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)