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October 2006

FAIRCHILD SEMICONDUCTOR®

FDS6994S

Dual Notebook Power Supply N-Channel PowerTrench® SyncFet™

General Description

The FDS6994S is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6994S contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

Features

- **Q2**: Optimized to minimize conduction losses
  Includes SyncFET Schottky body diode

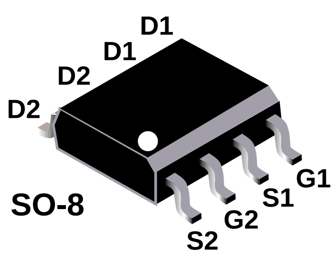
  8.2A, 30V $R_{DS(on)}$ = 15 mΩ @ V_{GS} = 10V

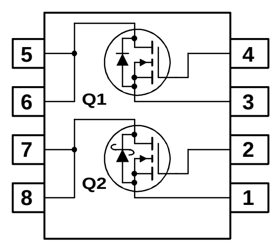
  $R_{DS(on)}$ = 17.5 mΩ @ V_{GS} = 4.5V

- **Q1**: Optimized for low switching losses
  Low gate charge (85.5 nC typical)

  6.9A, 30V $R_{DS(on)}$ = 21 mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ = 26 mΩ @ V_{GS} = 4.5V





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±16	±16	V
I_D	Drain Current - Continuous	(Note 1a)	8.2	6.9	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6994S	FDS6994S	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA V_{GS} = 0 V, I_D = 250 uA	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 μA, Referenced to 25°C	Q2 Q1		23 24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q2 Q1			500 1	μA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±16 V, V_{DS} = 0 V	All			±100	nA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA V_{DS} = V_{GS}, I_D = 250 μA	Q2 Q1	1 1	1.5 1.9	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 uA, Referenced to 25°C	Q2 Q1		–2 –5		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8.2A V_{GS} = 10 V, I_D = 8.2 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7.6 A	Q2		10 15 11	15 24 17.5	mΩ
		V_{GS} = 10 V, I_D = 6.9 A V_{GS} = 10 V, I_D = 6.9 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 6.2 A	Q1		16 24 19	21 33.5 26	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 8.2 A V_{DS} = 10 V, I_D = 6.9 A	Q2 Q1	42 41			S

Dynamic Characteristics

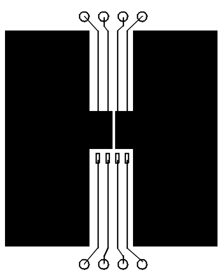
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	Q2 Q1		2815 800		pF
C_{oss}	Output Capacitance		Q2 Q1		540 205		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		210 90		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	Q2 Q1		2.8 2.6	4.9 4.6	Ω

Electrical Characteristics (continued) $T_A = 25°C$ unless otherwise noted

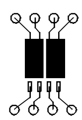
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10V$, $R_{GEN} = 6\ \Omega$	Q2 Q1		11 11	20 20	ns
t_r	Turn-On Rise Time		Q2 Q1		8 7	16 14	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		50 27	80 43	ns
t_f	Turn-Off Fall Time		Q2 Q1		17 4	31 8	ns
Q_g	Total Gate Charge	Q2: $V_{DS} = 15$ V, $I_D = 7.9$ A, $V_{GS} = 5$ V	Q2 Q1		25 8	35 12	nC
Q_{gs}	Gate-Source Charge	Q1: $V_{DS} = 15$ V, $I_D = 6.5$ A, $V_{GS} = 5$ V	Q2 Q1		6 3		nC
Q_{gd}	Gate-Drain Charge		Q2 Q1		7 3		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			2.3 1.3	A
t_{RR}	Reverse Recovery Time	$I_F = 8.2$ A, $d_{iF}/d_t = 300$ A/µs (Note 3)	Q2		25		ns
Q_{RR}	Reverse Recovery Charge				19		nC
t_{RR}	Reverse Recovery Time	$I_F = 6.9$ A, $d_{iF}/d_t = 100$ A/µs (Note 3)	Q2		23		ns
Q_{RR}	Reverse Recovery Charge				10		nC
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 2.3$ A (Note 2) $V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)	Q2 Q1		0.4 0.53	7 1.2	V

Notes:

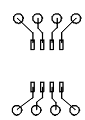
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. See "SyncFET Schottky body diode characteristics" below.

Typical Characteristics for Q2

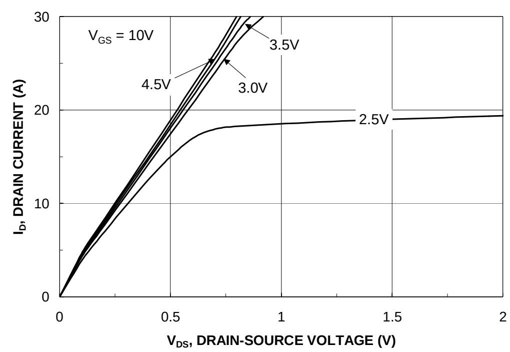


Figure 1. On-Region Characteristics.

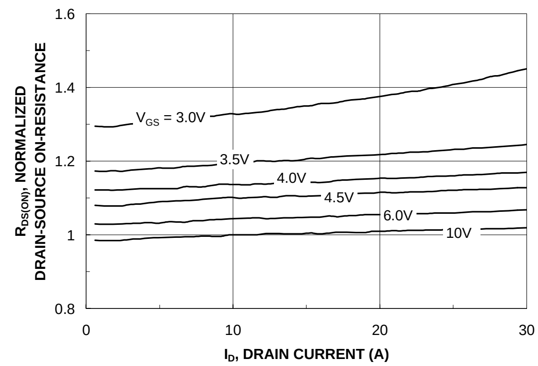


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

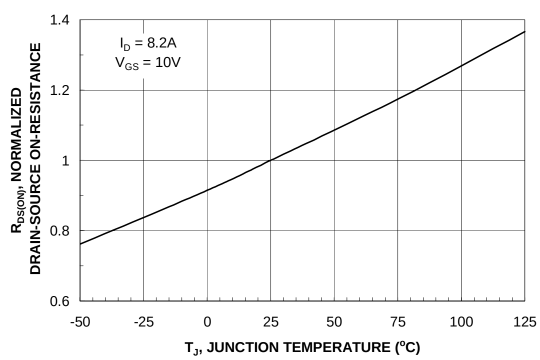


Figure 3. On-Resistance Variation with Temperature.

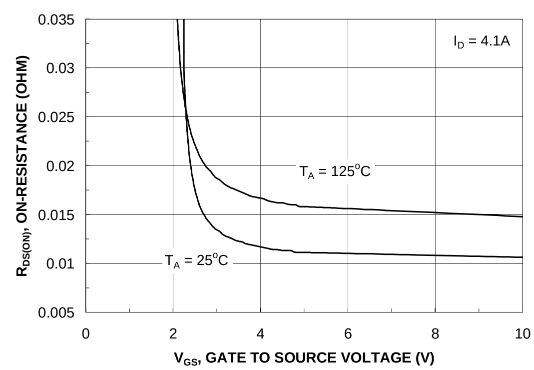


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

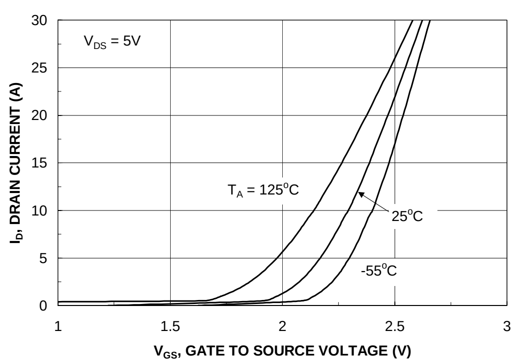


Figure 5. Transfer Characteristics.

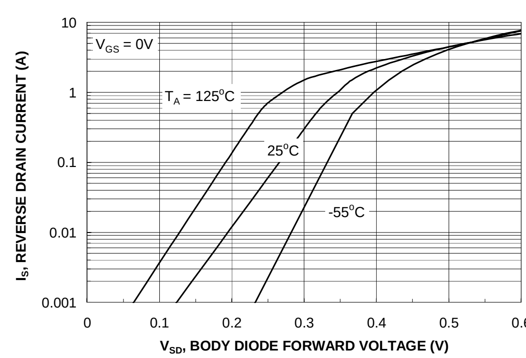


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics for Q2

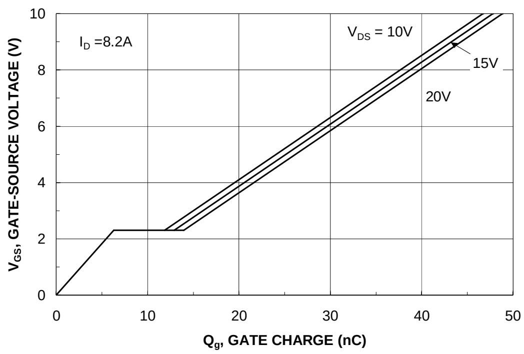


Figure 7. Gate Charge Characteristics.

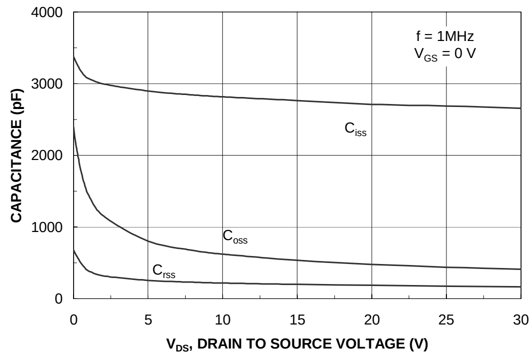


Figure 8. Capacitance Characteristics.

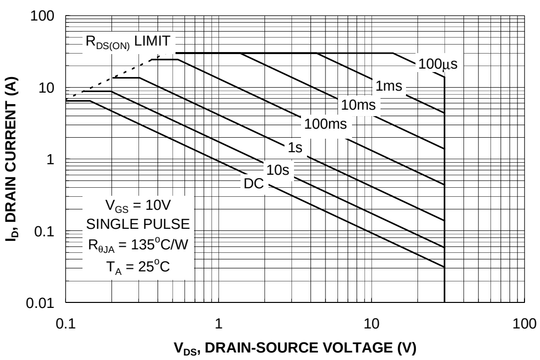


Figure 9. Maximum Safe Operating Area.

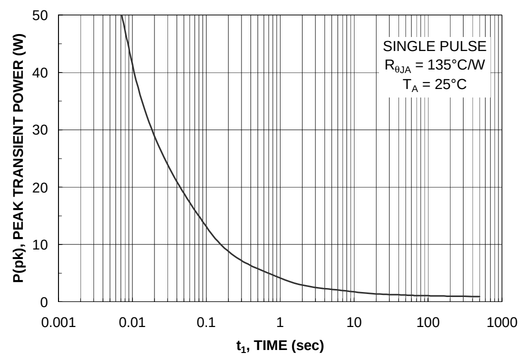


Figure 10. Single Pulse Maximum Power Dissipation.

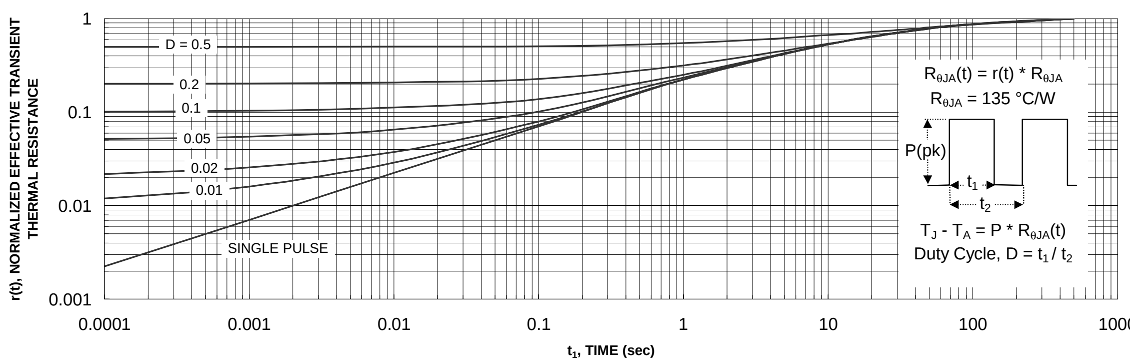


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics for Q1

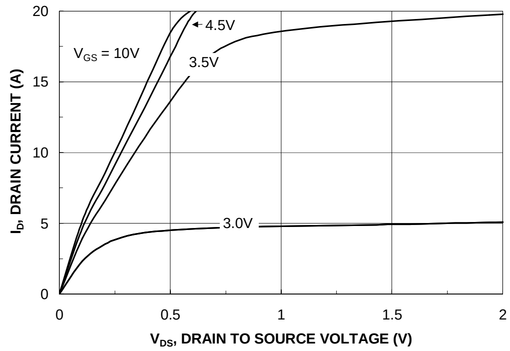


Figure 11. On-Region Characteristics.

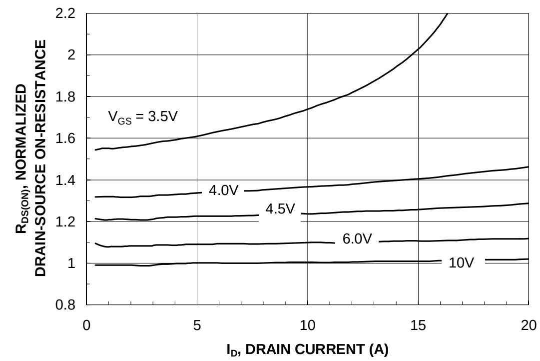


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

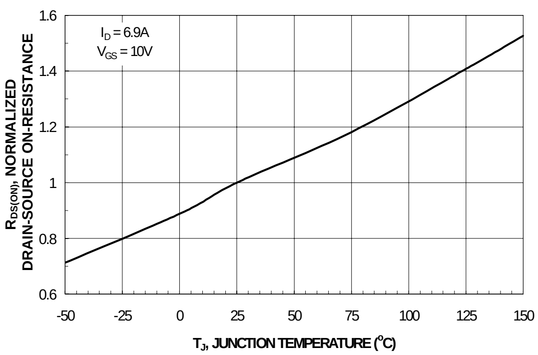


Figure 13. On-Resistance Variation with Temperature.

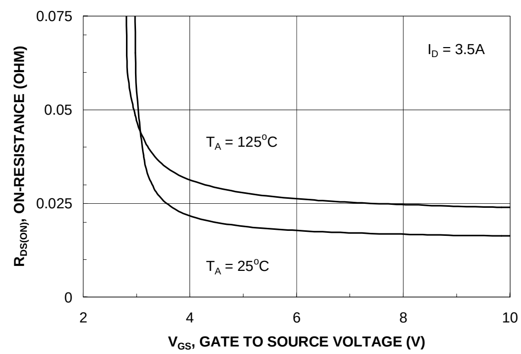


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

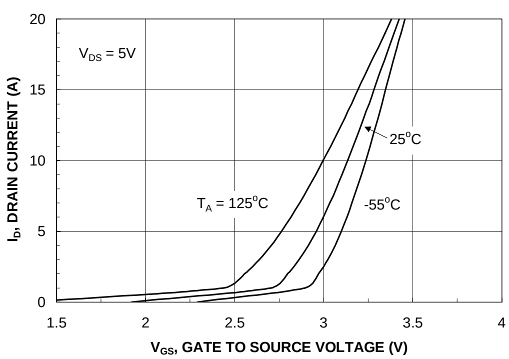


Figure 15. Transfer Characteristics.

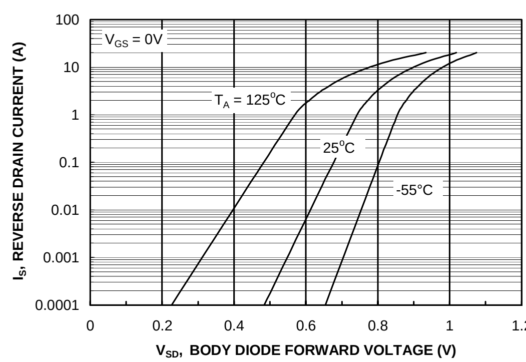


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

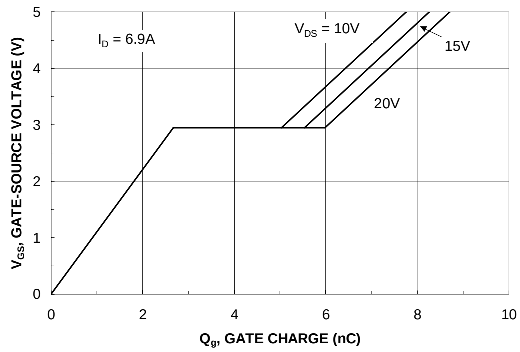


Figure 17. Gate Charge Characteristics.

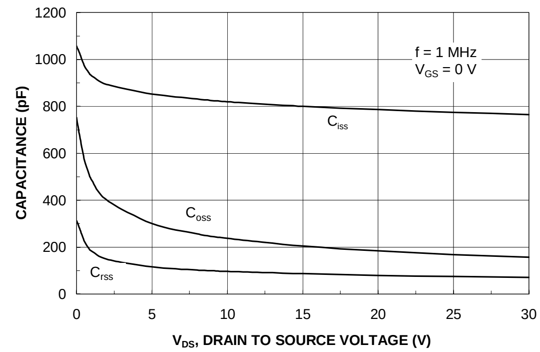


Figure 18. Capacitance Characteristics.

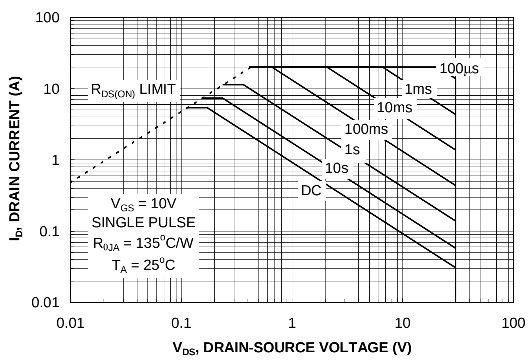


Figure 19. Maximum Safe Operating Area.

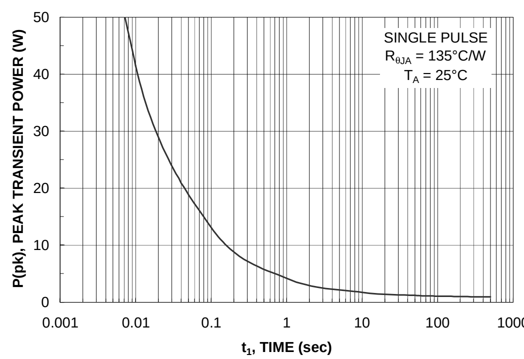


Figure 20. Single Pulse Maximum Power Dissipation.

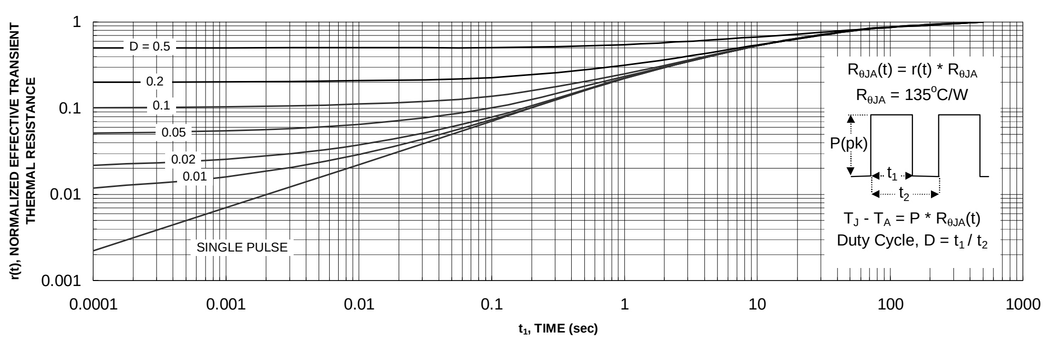


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued) This section copied from FDS6984S datasheet

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDS6994S.

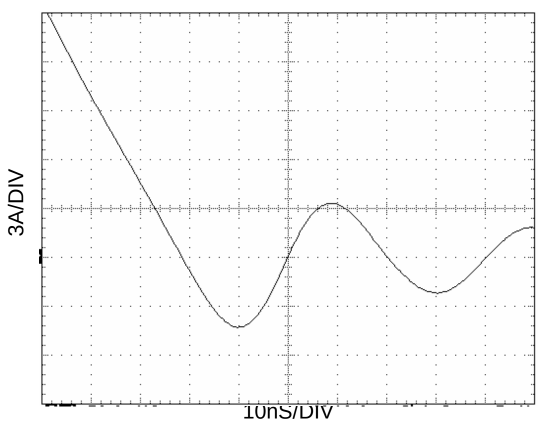


Figure 22. FDS6994S SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690A).

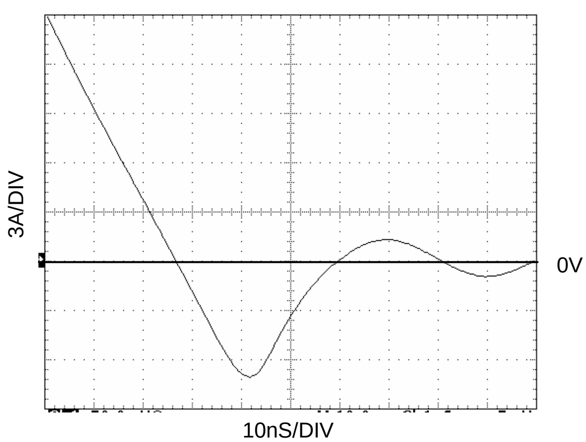


Figure 23. Non-SyncFET (FDS6690A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

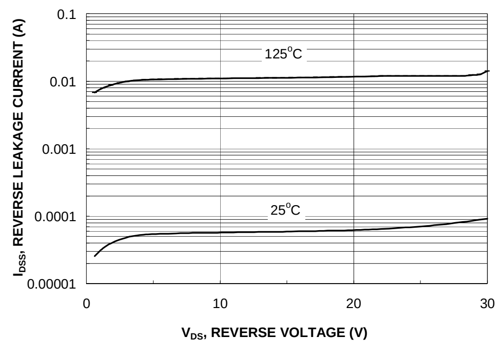


Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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