Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR TM

February 2012

FDT3612

100V N-Channel PowerTrench® MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

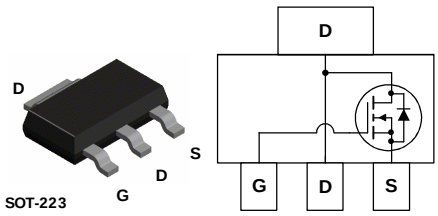
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

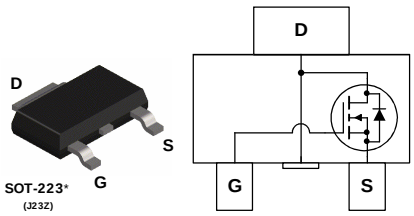
Applications

- DC/DC converter
- Motor driving

Features

- 3.7 A, 100 V. $R_{DS(ON)}$ = 120 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 130 mΩ @ V_{GS} = 6 V
- Fast switching speed
- Low gate charge (14nC typ)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	3.7	A
	– Pulsed		20	
P_D	Maximum Power Dissipation	(Note 1a)	3.0	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
3612	FDT3612	13”	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, V_{DD} = 50 V, I_D= 3.7 A			90	mJ
I_{AR}	Drain-Source Avalanche Current				3.7	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		106		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			10	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 3.7 A V_{GS} = 6 V, I_D = 3.5 A V_{GS} = 10 V, I_D = 3.7A, T_J = 125°C		88 94 170	120 130 245	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.7 A		11		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz		632		pF
C_{oss}	Output Capacitance			40		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 50 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8.5	17	ns
t_r	Turn–On Rise Time			2	4	ns
$t_{d(off)}$	Turn–Off Delay Time			23	37	ns
t_f	Turn–Off Fall Time			4.5	9	ns
Q_g	Total Gate Charge	V_{DS} = 50 V, I_D = 3.7 A, V_{GS} = 10 V		14	20	nC
Q_{gs}	Gate–Source Charge			2.4		nC
Q_{gd}	Gate–Drain Charge			3.8		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.75	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 42°C/W when mounted on a 1in^2 pad of 2 oz copper

b) 95°C/W when mounted on a .0066 in^2 pad of 2 oz copper

c) 110°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

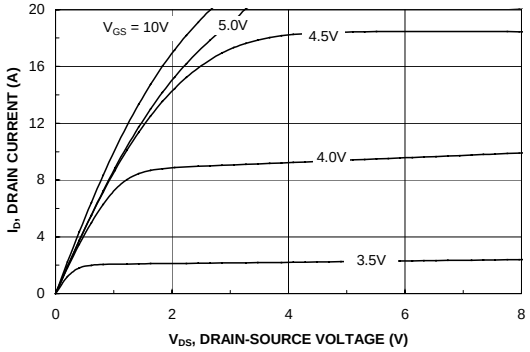


Figure 1. On-Region Characteristics.

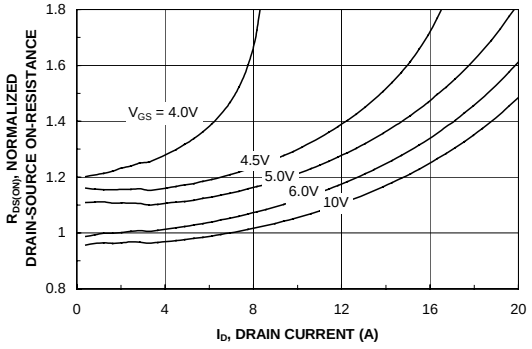


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

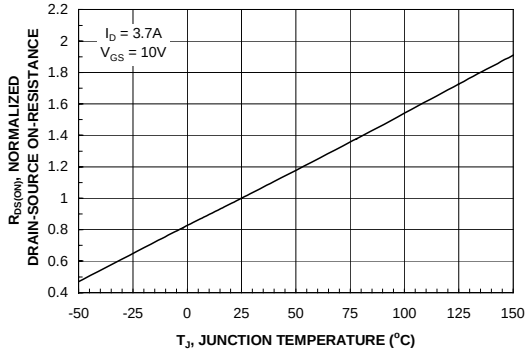


Figure 3. On-Resistance Variation with Temperature.

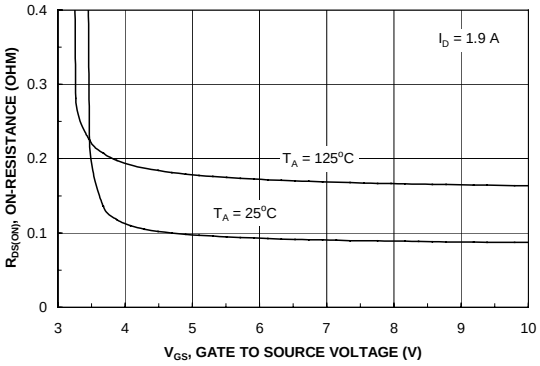


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

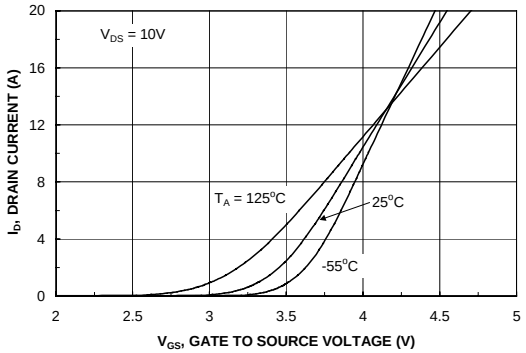


Figure 5. Transfer Characteristics.

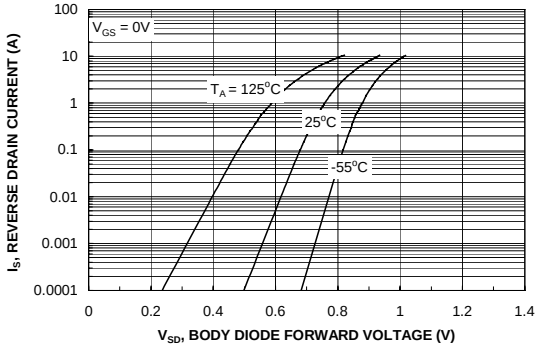


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

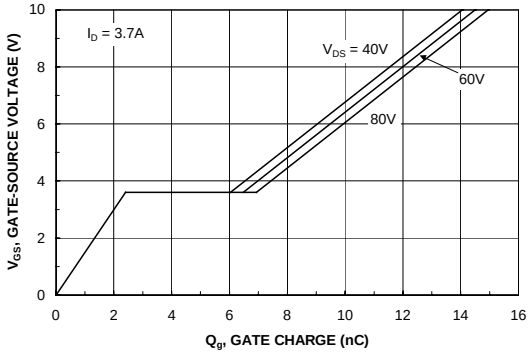


Figure 7. Gate Charge Characteristics.

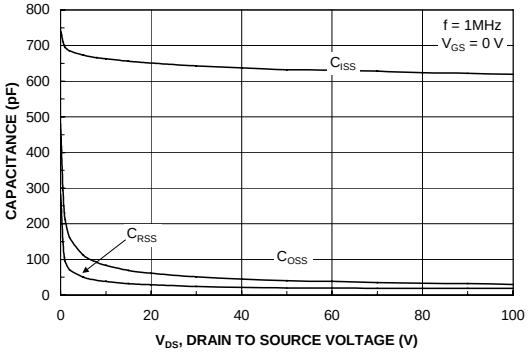


Figure 8. Capacitance Characteristics.

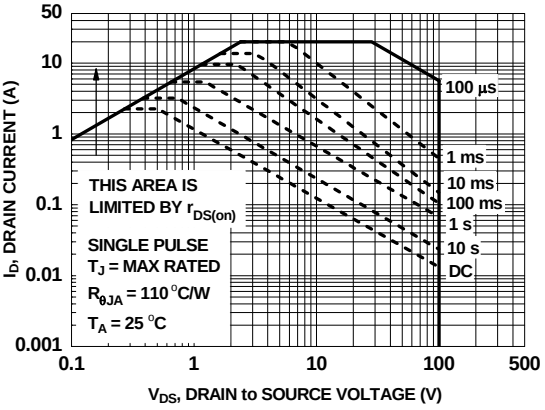


Figure 9. Maximum Safe Operating Area.

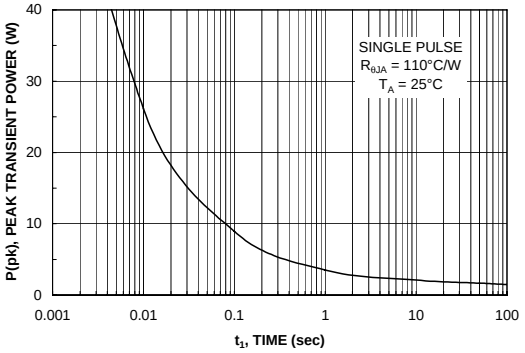


Figure 10. Single Pulse Maximum Power Dissipation.

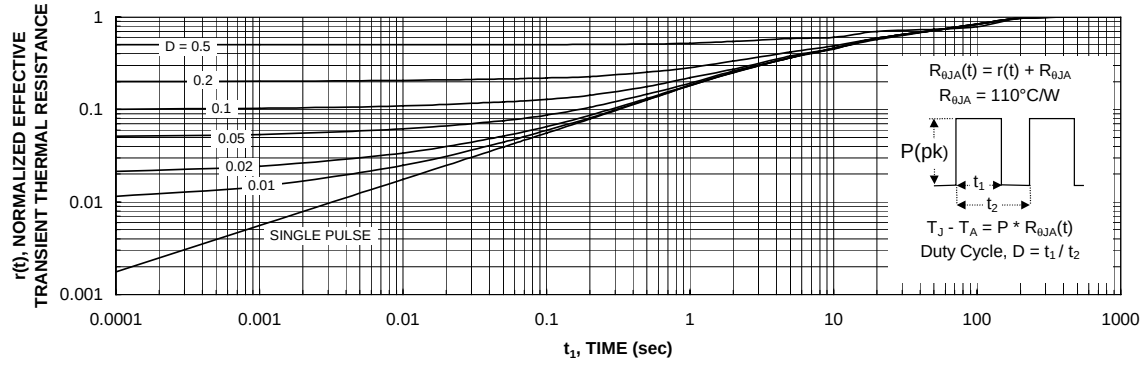
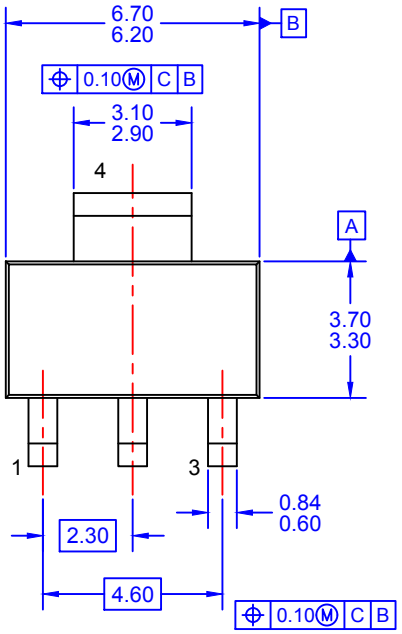
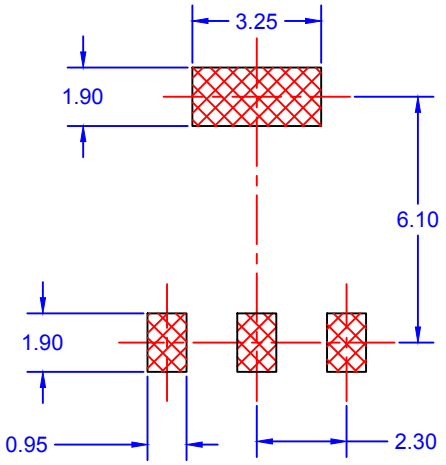


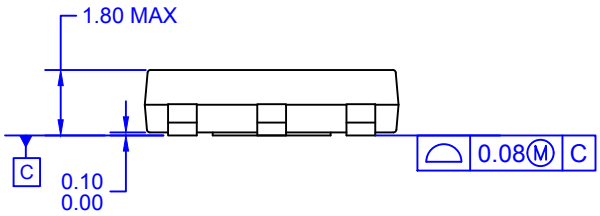
Figure 11. Transient Thermal Response Curve.

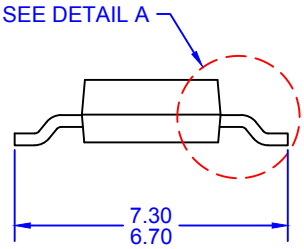
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.



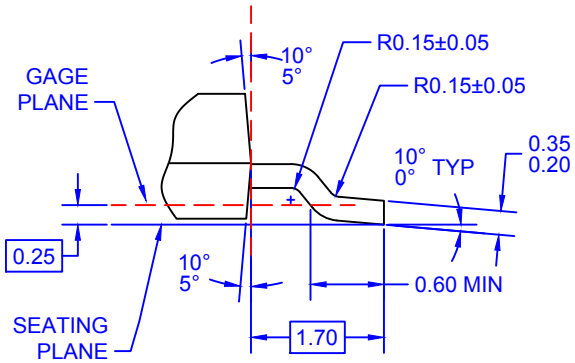


LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) LANDPATTERN NAME: SOT230P700X180-4BN
F) DRAWING FILENAME: MKT-MA04AREV3



DETAIL A
SCALE: 2:1

FAIRCHILD

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative