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FAIRCHILD SEMICONDUCTOR®

February 2008

FMS6403
Triple Video Drivers with Selectable HD/PS/SD Bypass Filters for RGB and YPbPr Signals

Features

- Three Video Anti-aliasing or Reconstruction Filters
- 2:1 MUX Inputs for YPbPr and RGB Inputs
- Supports D1, D2, D3, and D4 Video D-connector (EIAJ CP-4120)
- Selectable 8MHz/15MHz/30MHz 6th-order Filters, Plus Bypass
- Works with SD (480i), Progressive (480p), and HD (1080i/ 720p)
- AC-coupled Inputs Include DC Restore / Bias Circuitry
- All Outputs Can Drive AC- or DC-Coupled 75Ω Loads and Provide Either 0dB or 6dB of Gain
- 0.40% Differential Gain, 0.25° Differential Phase
- TSSOP-20 Packaging

Applications

- Progressive Scan
- Cable Set-top Boxes
- Home Theaters
- Satellite Set-top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6403 offers comprehensive filtering for TV, set-top box, or DVD applications. This part consists of a triple, sixth-order filter with selectable 30MHz, 15MHz, or 8MHz cutoff frequency. The filters may also be bypassed so that the bandwidth is limited only by the output amplifiers.

A 2:1 multiplexer is provided on each filter channel. The triple filters are intended for YPbPr and RGB signals. The DC clamp levels are set according to the RGB_SEL control input. YPbPr sync tips are clamped to 250mV, 1.125V, and 1.125V, respectively; while RGB sync tips are all clamped to 250mV. Sync clamp timing can be derived from the Y/G inputs or from the external SYNC_IN pin. The 8MHz and 15MHz filter settings support bi-level sync, while the 30MHz filter setting and bypass mode support tri-level sync.

All channels nominally accept AC-coupled $1V_{PP}$ signals. Selectable 0dB or 6dB gain allows the outputs to drive $1V_{PP}$ or $2V_{PP}$ signals into AC- or DC-coupled terminated loads with a $1V_{PP}$ input. Input signals cannot exceed $1.5V_{PP}$ and outputs cannot exceed $2.5V_{PP}$.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSM6403MTC	0 to 70°C	20-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units in Tubes
FSM6403MTC20X	0 to 70°C	20-Lead, Thin Shrink Small Outline Package (TSSOP)	2500 Unit Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Functional Block Diagram

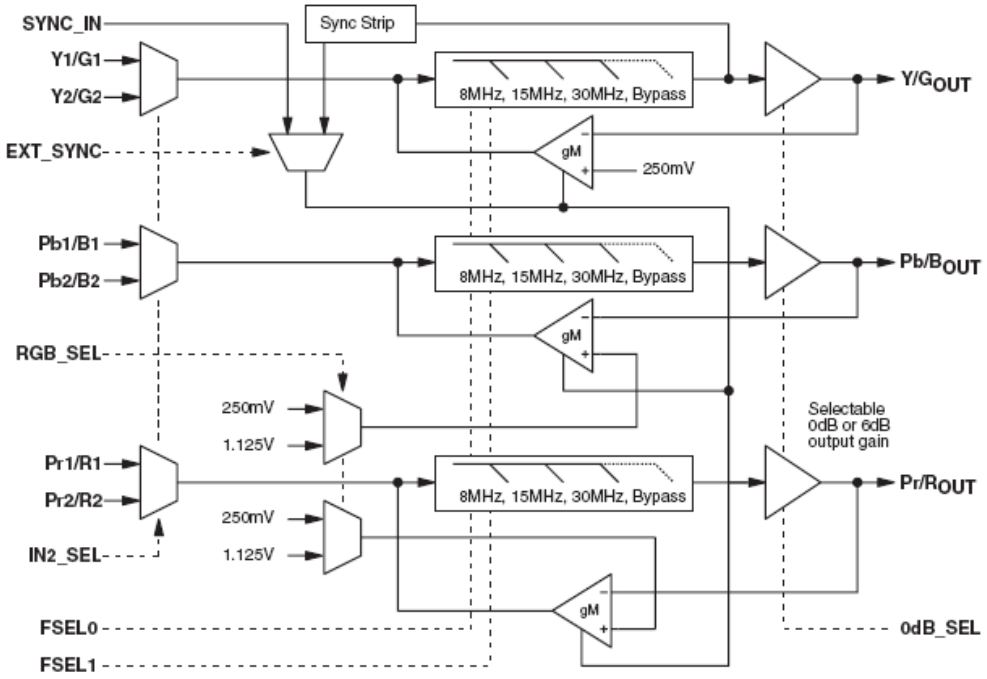

Figure 1. Block Diagram

Typical Application

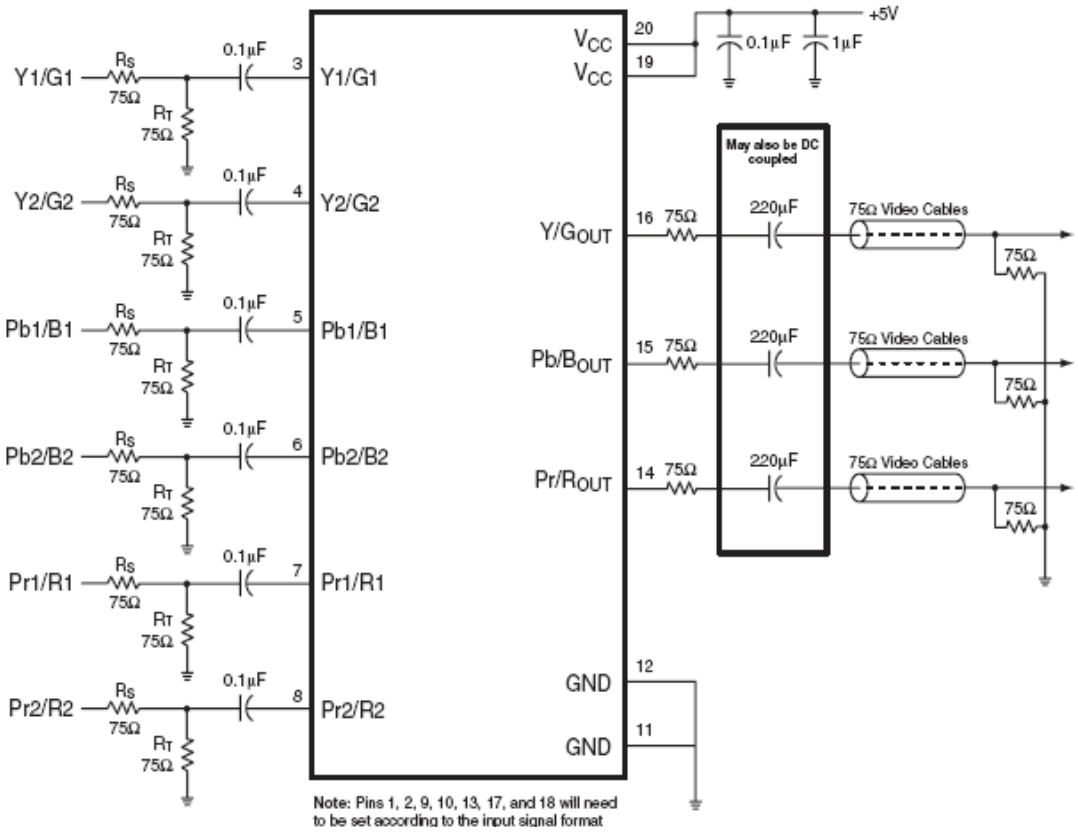

Figure 2. Typical Application Circuit

Pin Configuration

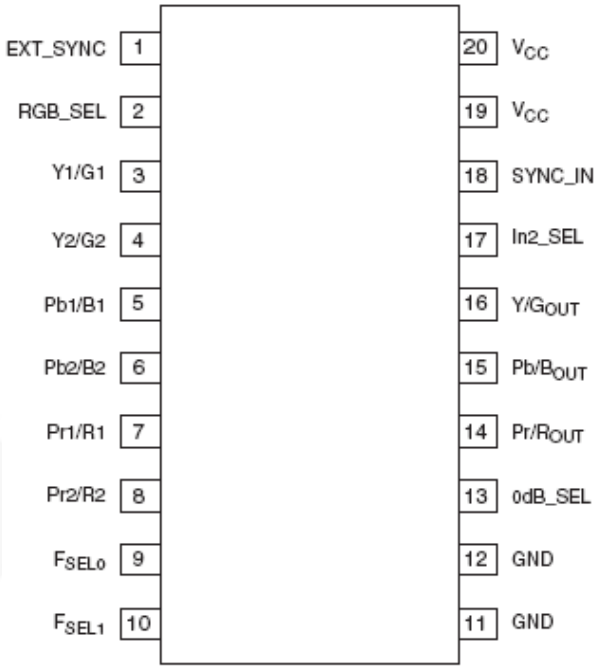

Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Type	Description
1	EXT_SYNC	Input	Selects the external SYNC_IN signal when set to logic 1; do not float.
2	RGB_SEL	Input	Selects RGB clamp levels when set to logic 1. YPbPr clamps levels when set to logic 0; do not float.
3	Y1/G1	Input	Y or G input 1 - may be connected to a signal that includes sync.
4	Y2/G2	Input	Y or G input 2 - may be connected to a signal that includes sync.
5	Pb1/B1	Input	Pb or B input 1.
6	Pb2/B2	Input	Pb or B input 2.
7	Pr1/R1	Input	Pr or R input 1.
8	Pr2/R2	Input	Pr or R input 2.
9	F_{SEL0}	Input	Selects filter corner frequency or bypass, see Table 2. Do not float.
10	F_{SEL1}	Input	Selects filter corner frequency or bypass, see Table 2. Do not float.
11	GND	Input	Must be tied to ground, do not float.
12	GND	Input	Must be tired to ground, do not float.
13	0dB_SEL	Input	Selects output gain of 0dB when set to logic 1; 6dB when set to logic 0. Do not float.
14	Pr/R_{OUT}	Output	Pr or R output.
15	Pb/B_{OUT}	Output	Pb or B output.
16	Y/G_{OUT}	Output	Y or G output.
17	In2_SEL	Input	Selects MUX input 2 when set to logic 1; MUX input 1 when set to logic 0. Do not float.
18	SYNC_IN	Input	External sync inputs signal, square wave crossing V_{IL} and V_{IN} input thresholds. Do not float.
19	V_{CC}	Input	+5V supply. Do not float.
20	V_{CC}	Input	+5V supply. Do not float.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	+6.6	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
I_{OUT}	Output Current, Any One Channel, Do Not Exceed		60	mA

Note:
1. Functional operation under any of these conditions is not implied.

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature, Soldering 10 seconds			+300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard Multi-layer Test Boards, Still Air		74		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	0		70	°C
V_{CC}	V_{CC} Range	4.75	5.00	5.25	V
R_{SOURCE}	Input Source Resistance			150	Ω

DC Electrical Specifications

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V; all inputs AC coupled with 0.1µF; all outputs AC coupled into 150Ω; referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(2)	V_{CC}, no load		90	130	mA
V_I	Input Voltage Maximum			1.5		V_{PP}
V_{IL}	Digital Input Low(2)	F_{SELO}, F_{SEL1}, RGB_SEL, 0dB_SEL, EXT_SYNC, IN2_SEL, SYNC_IN	0		0.8	V
V_{IH}	Digital Input High(2)	F_{SELO}, F_{SEL1}, RGB_SEL, 0dB_SEL, EXT_SYNC, IN2_SEL, SYNC_IN	2.4		V_{CC}	V
V_{CLAMP1}	Output Clamp Voltage	R,G,B,Y		250		mV
V_{CLAMP2}	Output Clamp Voltage	Pb and Pr		1.125		V
PSRR	Power Supply Rejection Ratio	DC, All Channels		-40		dB

Note:
2. 100% tested at 25°C.

Standard-Definition Electrical Specifications

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=0, F_{SEL1}=0, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{SD}	SD Gain, 0dB_SEL=0(3)	All Channels, SD Mode	5.6	6.0	6.4	dB
	SD Gain, 0dB_SEL=1(3)		-0.4	0	0.4	
f_{1dBSD}	-1dB Bandwidth for SD	All Channels	5.5	7.6		MHz
f_{CSD}	-3dB Bandwidth for SD	All Channels		8.5		MHz
f_{SBSD}	Attenuation: SD (Stop-band Rejection)(3)	All Channels at f=27MHz	40	56		dB
dG	Differential Gain	All Channels		0.40		%
dϕ	Differential Phase	All Channels		0.25		°
THD	Output Distortion, All Channels	V_{OUT}=1.8V_{PP} at 1MHz		0.4		%
X_{TALK}	Crosstalk, Channel-to-channel	At 1.0MHz		-68		dB
IN_{MUXISO}	INMUX Isolation	At 1.0MHz		-70		dB
SNR	Signal-to-Noise Ratio	All Channels, NTC-7 Weighting, 4.2MHz Lowpass, 100Khz Highpass		74		dB
t_{pdSD}	Propagation Delay for SD	Delay from Input to Output at 4.5MHz		80		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Minimum Pulse Width			4		µs

Note:
3. 100% tested at 25°C.

Progressive Scan (PS) Electrical Specifications

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=1, F_{SEL1}=0, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{PS}	PS Gain, 0dB_SEL=0[4]	All Channels PS Mode	5.6	6.0	6.4	dB
	PS Gain, 0dB_SEL=1[4]	All Channels PS Mode	-0.4	0	0.4	dB
f_{1dBPS}	-1dB Bandwidth for PS[4]	All Channels	10	15		MHz
f_{CPS}	-3dB Bandwidth for PS	All Channels		17		MHz
f_{SBPS}	Attenuation, PS (Stop-band Reject)[4]	All Channels at f=54MHz	40	48		dB
t_{pdPS}	Propagation Delay for PS	Delay from Input to Output at 10MHz		45		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Minimum Pulse Width			2		µs

Note:
4. 100% tested at 25°C.

High-Definition Electrical Specifications

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=0, F_{SEL1}=1, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{HD}	HD Gain, 0dB_SEL=0[5]	All Channels HD Mode	5.6	6.0	6.4	dB
	HD Gain, 0dB_SEL=1[5]	All Channels HD Mode	-0.4	0	0.4	dB
f_{1dBHD}	-1dB Bandwidth for HD[5]	All Channels	20	29		MHz
f_{CHD}	-3dB Bandwidth for HD	All Channels		33		MHz
f_{SBHD}	Attenuation, HD (Stop-band Reject)[5]	All Channels at f=74.25MHz	30	40		dB
t_{pdHD}	Propagation Delay for HD	Delay from Input to Output at 20MHz		26		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Minimum Pulse Width			1.5		µs

Note:
5. 100% tested at 25°C.

Unfiltered 1080p Bypass (Wide Bandwidth) Electrical Specifications

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=1, F_{SEL1}=1, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{WB}	Gain, 0dB_SEL=0[6]	All Channels Bypass Mode	5.6	6.0	6.4	dB
	Gain, 0dB_SEL=1[6]	All Channels Bypass Mode	-0.4	0	0.4	dB
f_{1dBWB}	-1dB Bandwidth	All Channels		63		MHz
f_{CWB}	-3dB Bandwidth	All Channels		91		MHz
t_{pdWB}	Propagation Delay	Delay from Input to Output at 20MHz		10		ns

Note:
6. 100% tested at 25°C.

Typical Performance Characteristics

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=0, F_{SEL1}=0, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

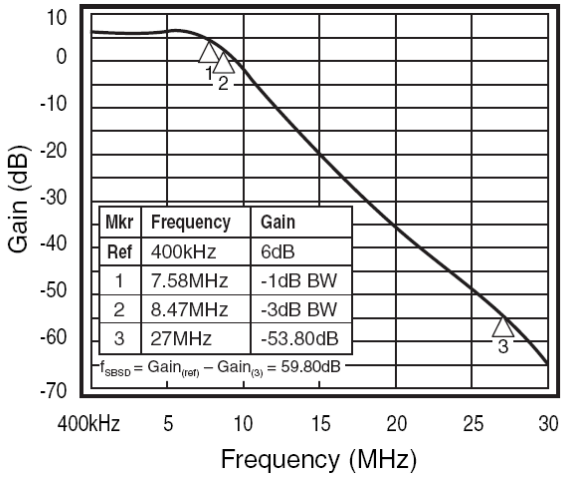

Figure 4. SD Frequency Response

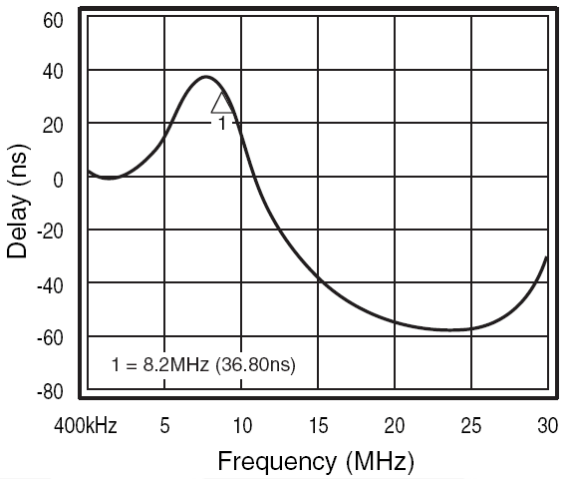

Figure 5. SD Group Delay vs. Frequency

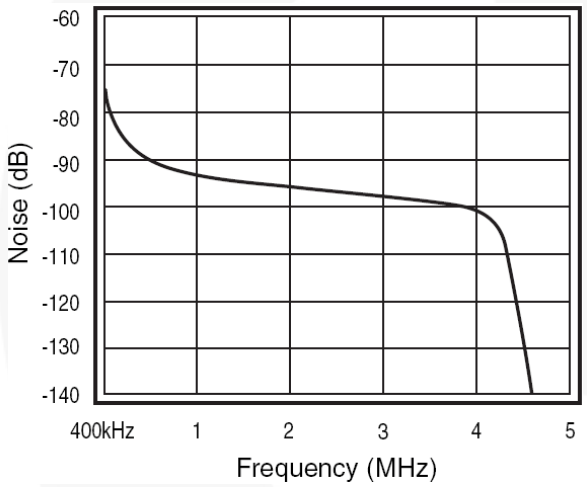

Figure 6. SD Noise vs. Frequency

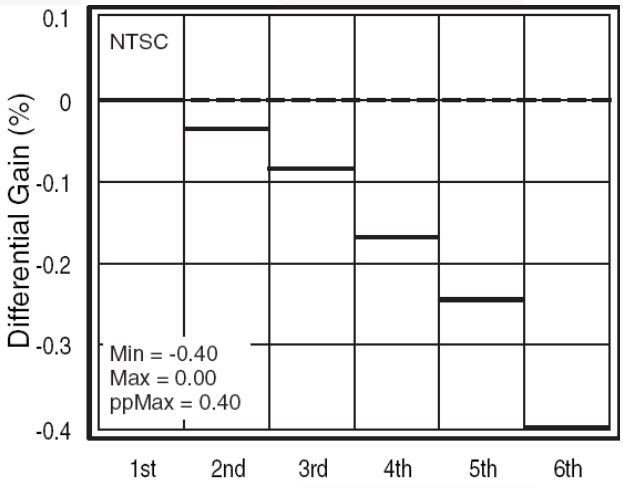

Figure 7. SD Differential Gain

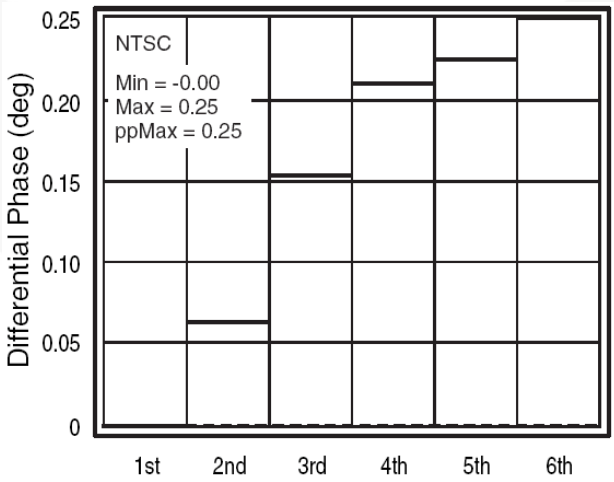

Figure 8. SD Differential Phase

Progressive Scan (PS) Typical Performance Characteristics

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=1, F_{SEL1}=0, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

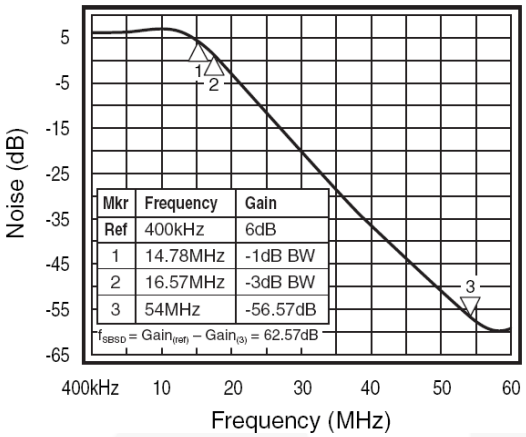

Figure 9. PS Frequency Response

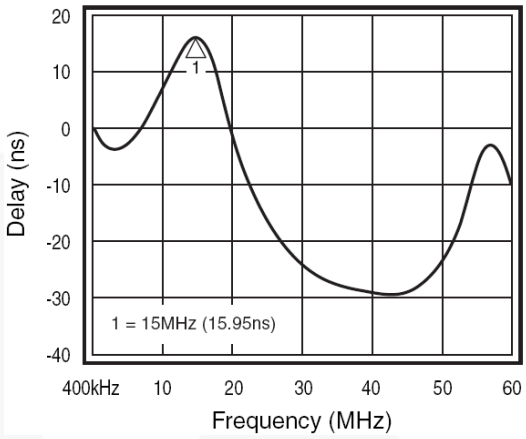

Figure 10. PS Group Delay vs. Frequency

High-Definition Typical Performance Characteristics

T_A=25°C, V_I=1V_{PP}, V_{CC} = 5.0V, F_{SEL0}=0, F_{SEL1}=1, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

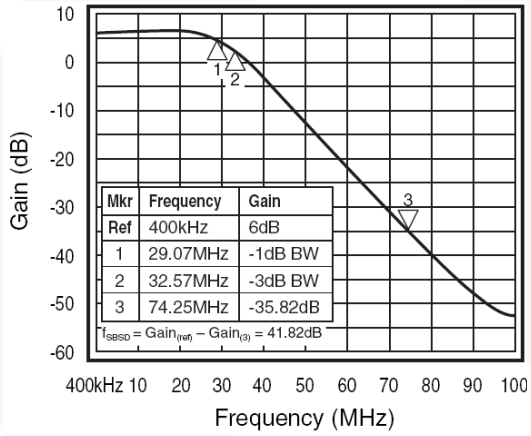

Figure 11. HD Frequency Response

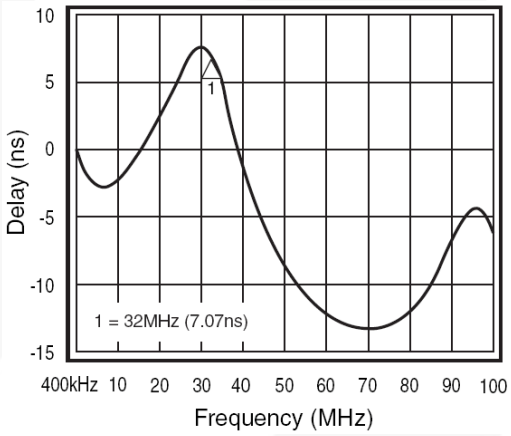

Figure 12. HD Group Delay vs. Frequency

Unfiltered 1080p Bypass (WB) Typical Performance Characteristics

T_A=25°C, V_I=1V_{PP}, V_{CC}=5.0V, F_{SEL0}=1, F_{SEL1}=1, 0dB_SEL=0 (gain=6dB), R_{SOURCE}=37.5Ω; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz: unless otherwise noted.

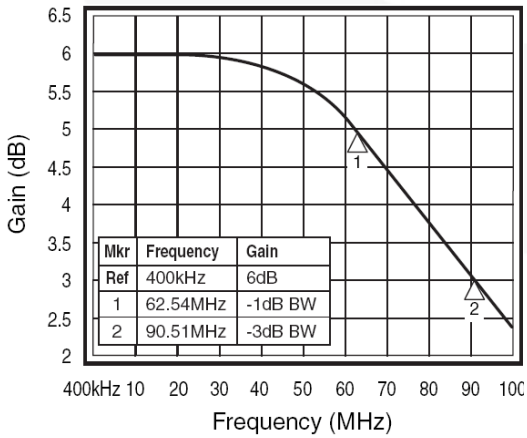

Figure 13. Bypass Mode Frequency Response

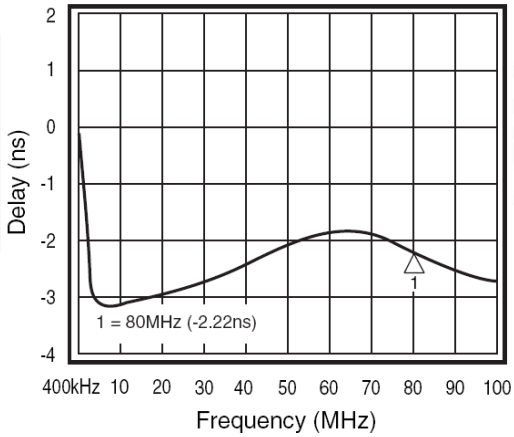

Figure 14. Bypass Mode Group Delay vs. Frequency

Functional Description

Introduction

The FMS6403 is a next-generation filter solution from Fairchild Semiconductor addressing the expanding filtering needs for televisions, set-top boxes, and DVD players, including progressive scan capability. The product provides selectable filtering with cutoff frequencies of 30MHz, 15MHz, and 8MHz for all three channels. In addition, the filters can be bypassed for wider bandwidth applications. The FMS6403 allows consumer devices to support a variety of resolution standards with the same hardware.

Multiplexers on the channel inputs are controlled by the IN2_SEL pin. The RGB_SEL pin can be used to set the sync tip clamp voltages for YPbPr or RGB applications. All three channels are set for 250mV sync tips to reduce DC-coupled power dissipation for RGB inputs. The lower output bias voltage is not suitable for the PbPr outputs; so for YPbPr inputs, these signals are clamped to 1.125V, while Y is still clamped to 250mV. Sync tip clamping voltages are set by forcing the desired DC bias level during the active sync period. For systems without sync on Y/G, an external sync input is provided. If sync exists on one input Y/G signal, but not on the other Y/G input signal, the IN2_SEL and EXT_SYNC control inputs may be wired together on the PCB to switch the sync source with the input source. Both standard-definition (bi-level) and high-definition (tri-level) sync are supported at the Y/G inputs and SYNC_IN depending on the FSEL[1:0] inputs. *See the Sync Processing section for further details.*

Standard-definition (480i) and progressive (480p) signals are clamped by forcing the signal to the desired voltage during the sync pulse. For signals with sync, the sync tip itself is forced to the clamp voltage (typically 250mV). When high-definition (HD) sync is present (tri-level sync) the sync tip duration is too short to allow this approach. To accurately clamp HD signals, the sync pulse starts a timer and the actual clamping is done at the blanking level right after the sync pulse. The sync tip is typically placed at 250mV if its amplitude is 300mV.

All three outputs are driven by amplifiers with selectable gains of 0dB or +6dB. The gain is set with the 0dB_SEL pin. These amplifiers can drive two terminated video loads (75Ω) to $2V_{PP}$ with a $1V_{PP}$ input when set to 6dB gain. The input range is limited to $1.5V_{PP}$ and the output range is limited to $2.5V_{PP}$.

All control inputs must be driven high or low. Do not leave them floating.

External SYNC Mode

The FMS6403 can properly recover sync timing from video signals that include sync. If the Y-input video signals do not include sync, the FMS6403 can be used in sxternal SYNC mode. In external sync mode, (EXT_SYNC pin is high), a pulsed input must be applied to the SYNC_IN pin. If there is no video signal present, therefore no sync signal present, there must be an input applied to the SYNC_IN pin. When there is no video signal on the video inputs, SYNC_IN can be a sync pulse every 60µs to mimic the slowest sync in a regular video signal. The following two sections discuss the sync processing and timing required in more detail.

SD and Progressive Scan Video Sync Processing

The FMS6403 must control the DC offset of AC-coupled input signals since the average DC level of video varies with image content. If the input offset is allowed to wander, the common-mode input range of the amplifiers can be exceeded, leading to signal distortion. DC offset adjustment is referred to as “clamping” or, in some cases, biasing, and must be done at the correct time during each video line. The optimum time is during the sync pulse, since it is the lowest input voltage. This approach works well for 480i and 480p signals since the sync tip duration is long enough to allow the DC-offset errors to be compensated from line to line. The DC-offset of the sync tip is adjusted as illustrated in Figure 15 by forcing a current on the input during the sync pulse. The sync tip is clamped to approximately 250mV. Signals like Pb and Pr with a symmetric voltage range (±350mV) are clamped to approximately 1.125V. Note that the following diagrams illustrate DC restore functionality and indicate output voltage levels for both 0dB and 6dB gain ($1V_{PP}$ and $2V_{PP}$ video signals at the output pin).

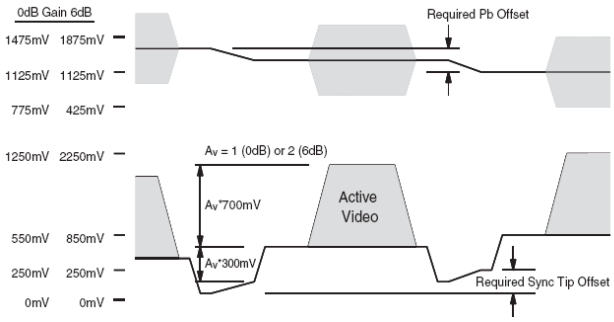

Figure 15. Bi-level Sync Tip Clamping and Bias

In some cases, the sync voltage may be compressed to less than the nominal 300mV value. The FMS6403 can successfully recover SD and progressive scan sync greater than 100mV (compressed to 33% of nominal).

The FMS6403 can properly recover sync timing from luma and green, which include sync. If none of the video signals includes sync, the EXT_SYNC control input can be set high and an external sync signal must be input on the SYNC_IN pin. *Refer to the External Sync section for more details.* The timing required for this operating mode is shown in Figure 16. SYNC timings, T1 and T2, are defined in the SD Electrical Specifications section.

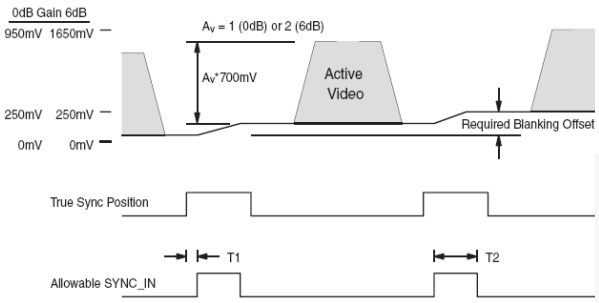

Figure 16. Bi-level External Sync Clamping and Bias

HD and Bypass Mode Video Sync Processing

When the input signal is a high-definition signal, the tri-level sync pulse is too short to allow proper clamp operation. Rather than clamp during the sync pulse, the sync pulse is located and the signal is clamped to the blanking level. This is done such that the sync tip is set to approximately 250mV for signals with 300mV sync tip amplitude. The EXT_SYNC control input selects the sync stripper output or the SYNC_IN pin for use by the clamp circuit.

Note:

7. The SYNC_IN timing for HD signals is different from the timing for SD or PS signals.

For HD signals, the SYNC_IN signal must be high when the clamp must be active. This is during the time immediately after the sync pulse while the signal is at the blanking level. This operation is shown in Figure 17. Note that the following diagrams illustrate DC restore functionality and indicate output voltage levels for both 0dB and 6dB gain ($1V_{PP}$ and $2V_{PP}$ video signals at the FMS6403 output pin). SYNC timings, T1 and T2, are defined in the HD Electrical Specifications table section.

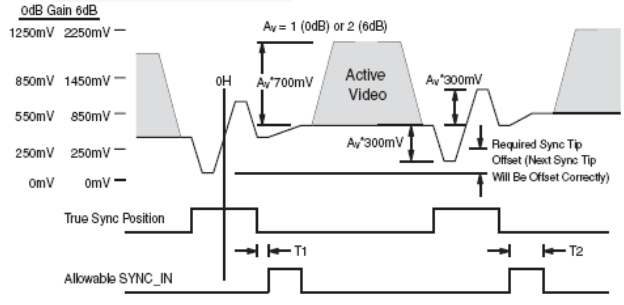

Figure 17. Tri-level Blanking Clamp

Note:

8. Tri-level sync may only be compressed 5%. If HD sync is compressed more than 5%, it may not be properly located.

Sync Timing

Normally, the FMS6403 responds to bi-level sync and clamps the sync tip during period 'B' in Figure 19. When the filters are switched to high-definition mode (30MHz) or bypass mode, the sync processing responds to tri-level sync and clamps to the blanking level during period 'C' in Figure 19.

Note:

9. The diagram indicates SYNC timings at the output pin.

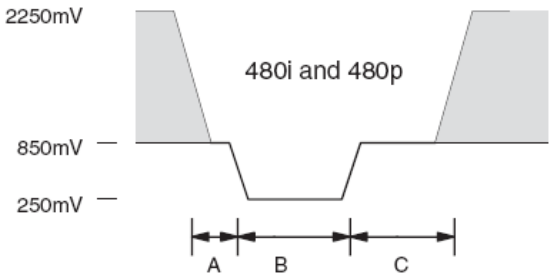

Figure 18. Sync Timing Bi-level

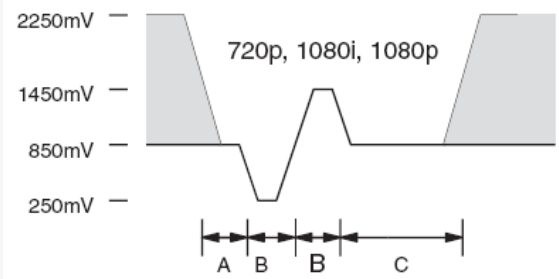

Figure 19. Sync Timing Tri-level

The tri-level sync pulse is located such that the broad pulses in the vertical interval do not trigger the clamp. To improve the system settling at turn-on, the broad pulses are clamped to just above ground. Once the broad pulses (and tri-level sync tips) are above ground, the normal clamping process takes over and clamps to the blanking level during period 'C' in Figure 19.

FMS6403 is supports the video standards and associated sync timings shown in Table 1, (additional standards, such as 483p59.94, also work correctly).

Table 1. Sync Timings

Format	Refresh	Sample Rate	Period (T)	A	B	C	H-Rate
480i	30Hz	13.5MHz	74ns	20T=1.5µs	64T=4.7µs	61T=4.5µs	15.75kHz
480p	60Hz	27 MHz	37ns	20T=750ns	64T=2.35µs	61T=2.25µs	31.5kHz
720p	60Hz	74.25 MHz	13.4ns	70T=938ns	40T=536ns	220T=2.95ns	45kHz
1080i	30Hz	74.25 MHz	13.4ns	20T=589ns	44T=589ns	148T=1.98ns	33.75kHz
1080p	60Hz	148.5 MHz	6.7ns	20T=596ns	44T=296ns	148T=996ns	67.5kHz

Note:
10. Timing values are approximate for 30Hz/60Hz refresh rates.

Table 2. Filter Settings

FSEL1, Pin 10	FSEL0, Pin 9	Filter -3db Frequency	Video Format	Sync Format
0	0	8MHz	SD, 480i	Bi-level, 4.7µs pulse width
0	1	15MHz	PS, 480p	Bi-level, 2.35µs pulse width
1	0	32MHz	HD, 1080i, 720p	Tri-level, 589ns pulse width
1	1	Filter Bypass	Unfiltered 1080p	Tri-level, 290ns pulse width

Table 3. Gain Settings Tables

0dB_SEL, Pin 13	Gain (dB)	V_{IN} (11)	V_{OUT} (11)
0	6	$1V_{PP}$	$2V_{PP}$
1	0	$1V_{PP}$	$1V_{PP}$

Note:
11. Video level does not include damp voltage, which offsets the input above ground.

Table 4. Sync Settings

EXT_SYNC, Pin 1	Sync Source
0	Y/G Input, Pin 3/4
1	SYNC_IN Input, Pin 2

Table 5. Clamp Settings

RGB_SEL, Pin 2	Input	Output	Clamp Voltage
0	Y1, Pin 3	Y, Pin 16	250mV
	Pb1, Pin 5	Pb, Pin 15	1.125V
	Pr1, Pin 7	Pr, Pin 14	1.125V
1	G1, Pin 3	G, Pin 16	250mV
	B1, Pin 5	B, Pin 15	250mV
	R1, Pin 7	R, Pin 14	250mV

Applications Information

Input Circuitry

The DC restore circuit requires a source impedance ($R_{SOURCE} = R_S \parallel R_T$) of less than or equal to 150Ω for correct operation. Driving the FMS6403 with a high-impedance source (e.g. a DAC loaded with 330Ω) does not yield optimum results. *Refer Figure 2 for details.*

Output Drive

The FMS6403 is specified to operate with output currents typically less than 60mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to approximately 100mA and should withstand brief-duration, short-circuit conditions; however, this capability is not guaranteed.

The maximum specified input voltage of $1.5V_{PP}$ can be sustained for all inputs. When the input is clamped to 1.125V, this does not result in a meaningful output signal. With a gain of 6dB, the output should be 1.125V ±1.5V, which is not possible since the output cannot drive below ground. This condition will not damage the part; however, the output will be clipped. For signals clamped to 250mV, this does not occur.

Signals at mid-scale during SYNC (Pb and Pr) must be clamped to 1.125V. Signals that are at their lowest during SYNC (Y, R, G, B) must be clamped to 250mV for proper operation. Clamping a Pr signal to 250mV results in clipping the bottom of the signal.

The 220µF capacitor coupled with the 150Ω termination, as shown in the Figure 2, forms a high-pass filter that blocks the DC while passing the video frequencies and avoiding tilt. Any value lower than 220µF creates problems, such as video tilt. Higher values, such as 470µF - 1000µF, are the most optimal output coupling capacitor. By AC coupling, the average DC level is zero and the output voltages of all channels is centered ~zero.

Sync Recovery

The FMS6403 typically recovers bi-level sync with amplitude greater than 100mV (33% compressed relative to the nominal 300mV amplitude). The FMS6403 looks for the lowest signal voltage and clamps this to approximately 250mV at the output.

Tri-level sync may not be compressed more than 5% (15mV) for correct operation. Tri-level sync is located by finding the edges of the tri-level pulse and running a timer to operate the clamp during the back porch interval.

The selection of the 8MHz or 15MHz filters enables bi-level sync recovery. Selection of the 30MHz filter or bypass mode enables tri-level sync recovery. Bi-level and tri-level sync recovery are not interchangeable. *See the Sync Processing section for more information.*

Power Dissipation

The output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6403's power dissipation and internal temperature rise:

$$T_J = T_A + Pd\ \Theta_{JA} \quad (1)$$

where:

$P_D = P_{CH1} + P_{CH2} + P_{CH3}$

and:

$PCHx = V_S \bullet I_{CH} - (V_O^2/R_L)$

where:

$V_O = 2V_{IN} + 0.280V$

$I_{CH} = (I_{CC} / 3) + (V_O/R_L)$

V_{IN} = RMS value of input signal

$I_{CC} = 90mA$

$V_S = 5V$

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations Section for more information.* The FMS6403 is specified to operate with output currents typically less than 60mA, more than sufficient for a single (150Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers an evaluation board, FMS6403DEMO, to guide layout and aid device testing and characterization. The FMS6403DEMO is a four-layer board with a full power and ground planes. For optimum results, follow the steps below as a basis for high-frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors.
- Place the 10µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Layout channel connections to reduce mutual trace inductance.
- Minimize all trace lengths to reduce series inductances. If routing across a board, place devise such that longer traces are at the inputs rather than the outputs.

If using multiple, low-impedance DC-coupled outputs; special layout techniques can help dissipate heat. For dual-layer boards, place a 0.5-inch to 1-inch (1.27cm to 2.54cm) square ground plane directly under the device and on the bottom side of the board. Use multiple vias to connect the ground planes. For multi-layer boards, additional planes (connected with vias) can be used for additional thermal improvements.

Worst-case additional die power due to DC loading can be estimated at ($V_{CC}^2/4R_{load}$) per output channel. This assumes a constant DC output voltage of V_{CC}^2. For 5V V_{CC} with a dual DC video load, add 25/(4•75) = 83mW, per channel.

Physical Dimensions

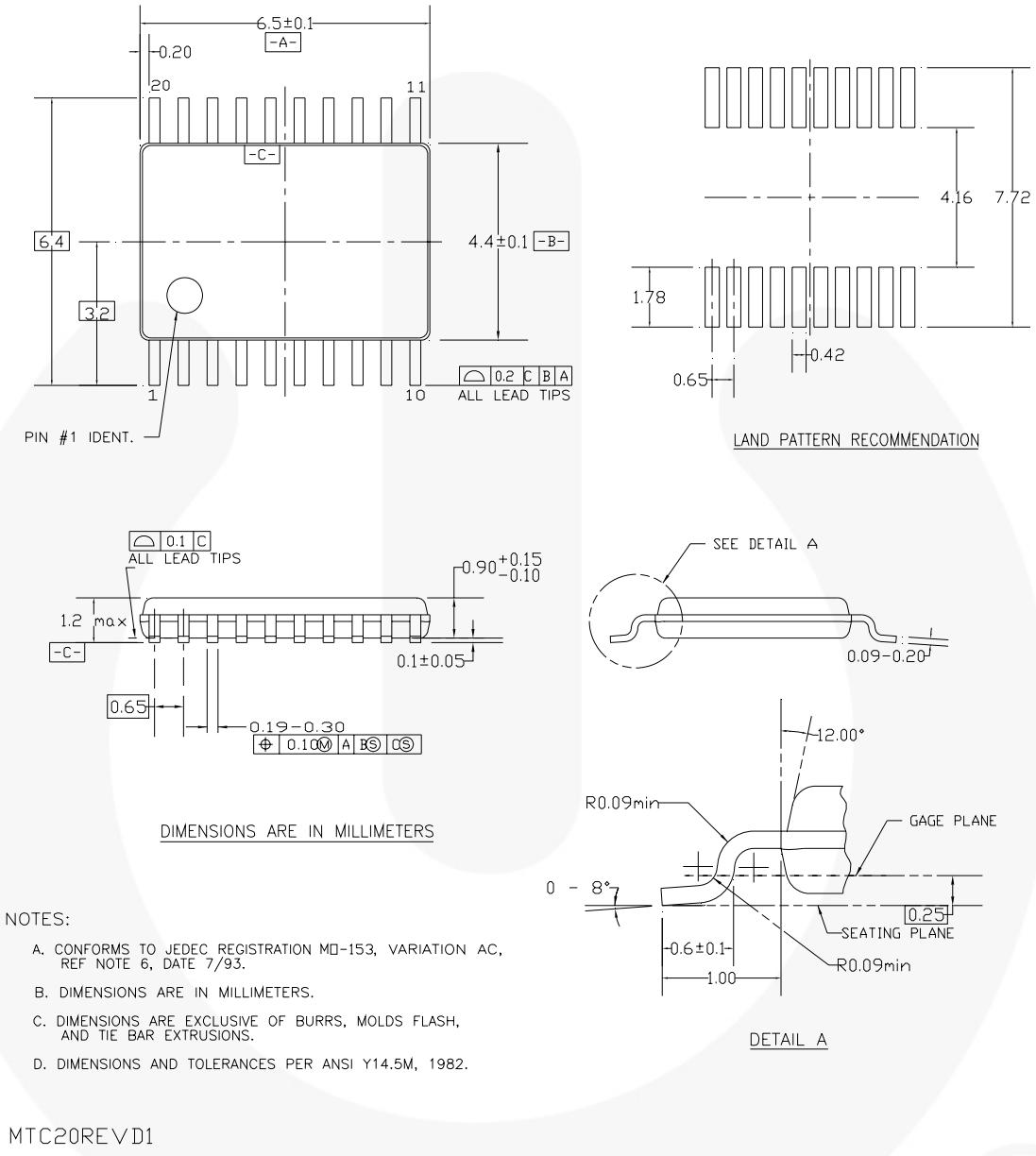

Figure 20. 20-lead Thin Shrink Small Outline Package (TSSOP)

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