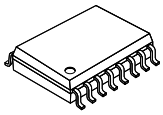
2.5 A Output Current, IGBT Drive Optocoupler with Desaturation Detection and Isolated Fault Sensing

FOD8316



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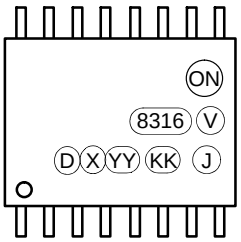
MARKING DIAGRAM



8316 = Device Number, e.g., '8316' for FOD8316
V = DIN EN/IEC60747−5−5 Option (Only Appears on Component Ordered with this Option)
D = Plant Code, e.g., 'D'
X = Last Digit Year Code, e.g., 'E' for 2014
YY = Two Digit Work Week Ranging from '01' to '53'
KK = Lot Traceability Code
J = Package Assembly Code, e.g., 'J'

ORDERING INFORMATION

See detailed ordering and shipping information on page 26 of this data sheet.

Description

The FOD8316 is an advanced 2.5 A output current IGBT drive optocoupler capable of driving most 1200 V /150 A IGBTs. It is ideally suited for fast−switching driving of power IGBTs and MOSFETs used in motor−control inverter applications and high−performance power systems. The FOD8316 offers critical protection features necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs.

The device utilizes **onsemi**'s proprietary OPTOPLANAR® coplanar packaging technology, and optimized IC design to achieve high noise immunity, characterized by high common−mode rejection and power supply rejection specifications.

The FOD8316 consists of an integrated gate drive optocoupler featuring low $R_{DS(ON)}$ CMOS transistors to drive the IGBT from rail−to−rail and an integrated high−speed isolated feedback for fault sensing. The device is housed in a compact 16−pin small−outline plastic package which meets the 8 mm creepage and clearance requirements.

Features

- High Noise Immunity Characterized by Common Mode Rejection − 35 kV/μs Minimum, V_{CM} = 1500 V_{PEAK}
- 2.5 A Peak Output Current Driving Capability for Most 1200 V / 150 A IGBTs
- Optically Isolated Fault Sensing Feedback
- "Soft" IGBT Turn−off
- Built−in IGBT Protection
  - Desaturation Detection
  - Under−Voltage Lockout (UVLO) Protection
- Wide Supply Voltage Range: 15 V to 30 V
  - P−Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to the Supply Rail (Rail−to−Rail Output)
- 3.3 V / 5 V, CMOS/TTL Compatible Inputs
- High Speed
  - 250 ns Maximum Propagation Delay Over Full Operating Temperature Range
- Extended Industrial Temperate Range, −40°C to 100°C
- Safety and Regulatory Approvals
  - UL1577, 4,243 V_{RMS} for 1 Minute
  - DIN EN/IEC 60747−5−5:
    1,414 V_{PEAK} Working Insulation Voltage Rating
    8,000 V_{PEAK} Transient Isolation Voltage Rating
- $R_{DS(ON)}$ of 1 Ω (Typical) Offers Lower Power Dissipation

Features (continued)

- User−Configurable: Inverting, Non−inverting, Auto−reset, Auto−shutdown
- 8 mm Creepage and Clearance Distances

Applications

- Industrial Inverter
- Induction Heating
- Isolated IGBT Drive

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TRUTH TABLE

V_{IN+}	V_{IN-}	UVLO ($V_{DD2} - V_E$)	DESAT Detected?	$\overline{FAULT}$	V_O
X	X	Active	X	X	LOW
X	X	X	Yes	LOW	LOW
LOW	X	X	X	X	LOW
X	HIGH	X	X	X	LOW
HIGH	LOW	Not Active	No	HIGH	HIGH

PIN CONFIGURATION

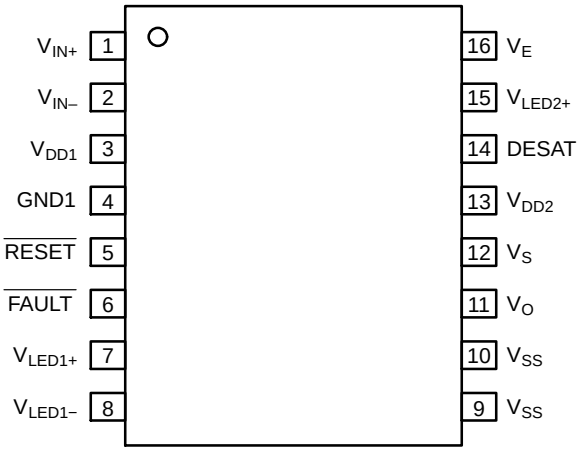

Figure 1. Pin Configuration

PIN DEFINITIONS

Pin No.	Name	Description
1	V_{IN+}	Non−inverting Gate Drive Control Input
2	V_{IN-}	Inverting Gate−Drive Control Input
3	V_{DD1}	Positive Input Supply Voltage (3 V to 5.5 V)
4	GND1	Input Ground
5	$\overline{RESET}$	FAULT Reset Input
6	$\overline{FAULT}$	Fault Output (Open Drain)
7	V_{LED1+}	LED 1 Anode (Do not connect. Leave floating.)
8	V_{LED1-}	LED 1 Cathode (Must be connected to ground.)
9	V_{SS}	Output Supply Voltage (Negative)
10	V_{SS}	Output Supply Voltage (Negative)
11	V_O	Gate−Drive Output Voltage
12	V_S	Pull−up PMOS Transistor Source
13	V_{DD2}	Positive Output Supply Voltage
14	DESAT	Desaturation Voltage Input
15	V_{LED2+}	LED 2 Anode (Do not connect. Leave floating.)
16	V_E	Output Supply Voltage / IGBT Emitter

BLOCK DIAGRAM

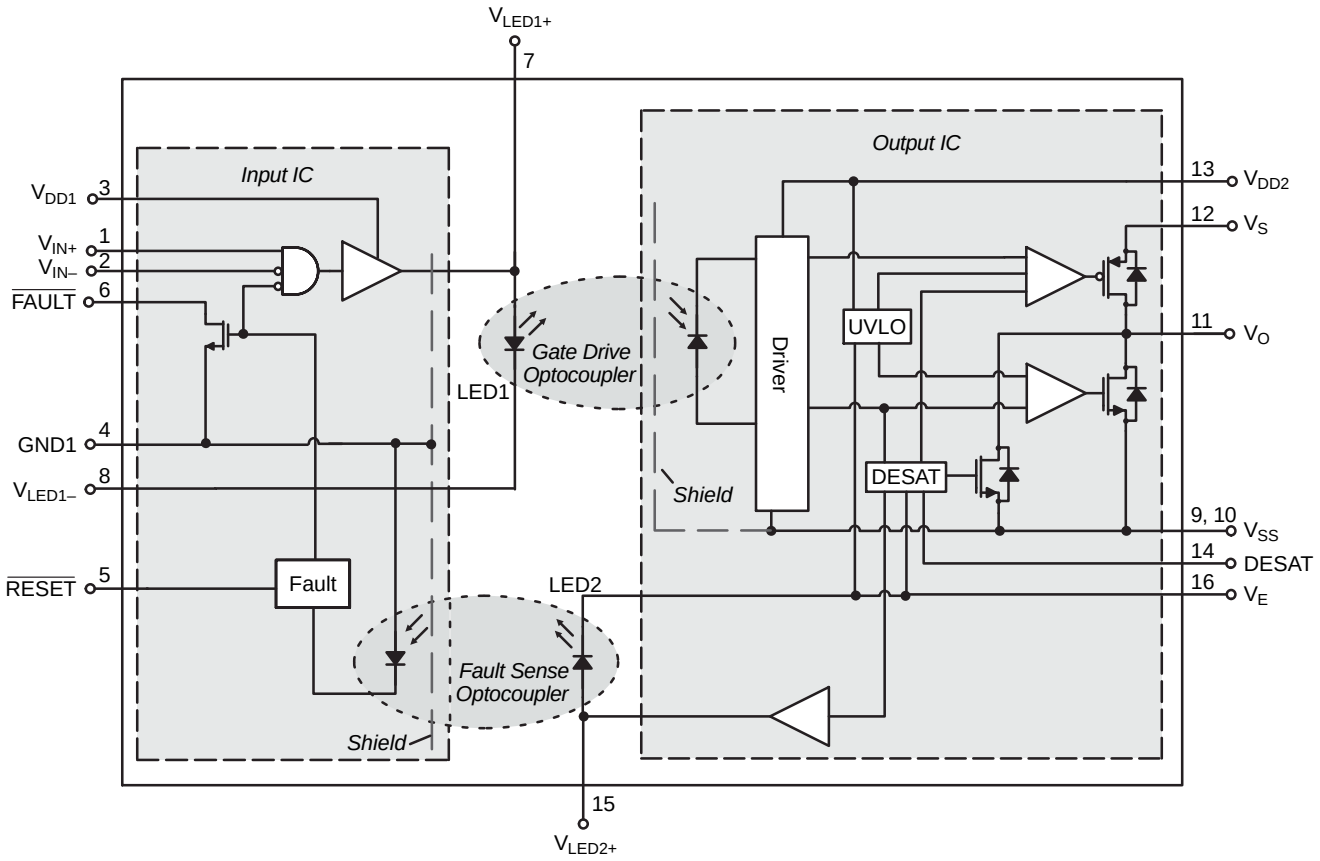

Figure 2. Block Diagram

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747−5−5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage < 150 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 300 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 450 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 600 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 1000 V_{RMS}	−	I−III	−	
	Climatic Classification	−	40/100/21	−	
	Pollution Degree (DIN VDE 0110/1.89)	−	2	−	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	175	−	−	
V_{PR}	Input−to−Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2651	−	−	V_{peak}
	Input−to−Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2262	−	−	V_{peak}
VI_{ORM}	Maximum Working Insulation Voltage	1414	−	−	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8000	−	−	V_{peak}
	External Creepage	8.0	−	−	mm
	External Clearance	8.0	−	−	mm
	Insulation Thickness	0.5	−	−	mm
T_{Case}	Safety Limit Values − Maximum Values in Failure; Case Temperature	150	−	−	°C
$P_{S,INPUT}$	Safety Limit Values − Maximum Values in Failure; Input Power	100	−	−	mW
$P_{S,OUTPUT}$	Safety Limit Values − Maximum Values in Failure; Output Power	600	−	−	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	−	−	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Wave Solder Temperature (No Solder Immersion) *Refer to Reflow Temperature Profile on Page 25.*	260 for 10 seconds	°C
$I_{\overline{FAULT}}$	Fault Output Current	15	mA
$I_{O(PEAK)}$	Peak Output Current (Note 1)	3	A
$V_E - V_{SS}$	Negative Output Supply Voltage (Note 2)	0 to 15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage	−0.5 to 35 − ($V_E - V_{SS}$)	V
$V_{O(peak)}$	Gate Drive Output Voltage	−0.5 to 35	V
$V_{DD2} - V_{SS}$	Output Supply Voltage	−0.5 to 35	V
V_{DD1}	Positive Input Supply Voltage	−0.5 to 6	V
V_{IN+}, V_{IN-} and $V_{\overline{RESET}}$	Input Voltages	−0.5 to V_{DD1}	V
V_{FAULT}	Fault Pin Voltage	−0.5 to V_{DD1}	V
V_S	Source of Pull−up PMOS Transistor Voltage	V_{SS} + 6.5 to V_{DD2}	V
V_{DESAT}	DESAT Voltage	V_E to V_E + 25	V
PD_I	Input Power Dissipation (Note 3, 5)	100	mW
PD_O	Output Power Dissipation (Note 4, 5)	600	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.
2. This negative output supply voltage is optional. It's only needed when negative gate drive is implemented. Refer to "Dual Supply Operation − Negative Bias at Vss" on page 23.
3. No derating required across temperature range.
4. Derate linearly above 64°C, free air temperature at a rate of 10.2 mW/°C
5. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+100	°C
V_{DD1}	Input Supply Voltage (Note 6)	3	5.5	V
$V_{DD2} - V_{SS}$	Total Output Supply Voltage	15	30	V
$V_E - V_{SS}$	Negative Output Supply Voltage	0	15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage (Note 6)	15	30 − ($V_E - V_{SS}$)	V
V_S	Source of Pull−up PMOS Transistor Voltage	V_{SS} + 7.5	V_{DD2}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. During power up or down, it is important to ensure that V_{IN+} remains low until both the input and output supply voltages reaches the proper recommended operating voltages to avoid any momentary instability at the output state. See also the discussion in the "Time to Good Power" section on page 23.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50 %, t = 1.0 minute, $I_{I-O} \leq 10$ μA, 50 Hz (Note 7, 8, 9)	4,243	−	−	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 7)	−	10^{11}	−	Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, Freq = 1.0 MHz (Note 7)	−	1	−	pF

7. Device is considered a two terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
8. 4,243 VRMS for 1−minute duration is equivalent to 5,091 VRMS for 1−second duration.
9. The input−output isolation voltage is a dielectric voltage rating as per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating refer to your equipment−level safety specification or DIN EN/IEC 60747−5−5 Safety and Insulation Ratings Table.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD1} = 5 V, $V_{DD2} - V_{SS}$ = 30 V, $V_E - V_{SS}$ = 0 V, and T_A = 25°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
V_{IN+L}, V_{IN-L}, $V_{\overline{RESETL}}$	Logic Low Input Voltages		−	−	0.8	V	
V_{IN+H}, V_{IN-H}, $V_{\overline{RESETH}}$	Logic High Input Voltages		2.0	−	−	V	
I_{IN+L}, I_{IN-L}, $I_{\overline{RESETL}}$	Logic Low Input Currents	V_{IN} = 0.4 V	−0.5	−0.001	−	mA	
$I_{\overline{FAULTL}}$	$\overline{FAULT}$ Logic Low Output Current	V_{FAULT} = 0.4 V	5.0	12.0	−	mA	3, 34
$I_{\overline{FAULTH}}$	$\overline{FAULT}$ Logic High Output Current	$V_{FAULT} = V_{DD1}$	−40	0.002	−	μA	34
I_{OH}	High Level Output Current	$V_O = V_{DD2} - 3$ V	−1	−2.5	−	A	4, 9, 35
		$V_O = V_{DD2} - 6$ V (Note 10)	−2.5	−	−	A	
I_{OL}	Low Level Output Current	$V_O = V_{SS} + 3$ V	1	3	−	A	5, 36
		$V_O = V_{SS} + 6$ V (Note 11)	2.5	−	−	A	
I_{OLF}	Low Level Output Current During Fault Condition	$V_O - V_{SS}$ = 14 V	70	125	170	mA	6, 40
V_{OH}	High Level Output Voltage	I_O = −100 mA (Note 12, 13, 14)	V_S − 1.0 V	V_S − 0.5 V	−	V	7, 9, 37
V_{OL}	Low Level Output Voltage	I_O = 100 mA	−	0.1	0.5	V	8, 10, 37
I_{DD1H}	High Level Supply Current	$V_{IN+} = V_{DD1}$ = 5.5 V, V_{IN-} = 0 V	−	14	17	mA	11, 38
I_{DD1L}	Low Level Supply Current	$V_{IN+} = V_{IN-}$ = 0 V, V_{DD1} = 5.5 V	−	2	3	mA	
I_{DD2H}	High Level Output Supply Current	V_O = Open (Note 14)	−	1.7	3	mA	12, 13, 39
I_{DD2L}	Low Level Output Supply Current	V_O = Open	−	1.8	2.8	mA	
I_{SH}	High Level Source Current	I_O = 0 mA	−	0.65	1.5	mA	39
I_{SL}	Low Level Source Current	I_O = 0 mA	−	0.6	1.4	mA	39
I_{EL}	V_E Low Level Supply Current		−0.8	−0.5	−	mA	15, 39
I_{EH}	V_E High Level Supply Current		−0.5	−0.25	−	mA	
I_{CHG}	Blanking Capacitor Charge Current	V_{DESAT} = 2 V (Note 14, 15)	−0.13	−0.25	−0.33	mA	14, 40
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7 V	10	36	−	mA	40
V_{UVLO+}	Under Voltage Lockout Threshold (Note 14)	V_O > 5 V @ 25°C	10.8	11.7	12.7	V	17, 31, 41
V_{UVLO-}		V_O < 5 V @ 25°C	9.8	10.7	11.7	V	
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis	@ 25°C	0.4	1.0	−	V	
V_{DESAT}	DESAT Threshold (Note 14)	$V_{DD2} - V_E > V_{ULVO-}$, V_O < 5 V	6.0	6.5	7.2	V	18, 40

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.
11. Maximum pulse width = 4.99 ms, maximum duty cycle = 99.8%.
12. V_{OH} is measured with the DC load current in this testing (Maximum pulse width = 1 ms, maximum duty cycle = 20%).When driving capacitive loads, V_{OH} will approach V_{DD} as I_{OH} approaches zero units.
13. Positive output supply voltage ($V_{DD2} - V_E$) should be at least 15 V to ensure adequate margin in excess of the maximum under−voltage lockout threshold, V_{UVLO+}, of 13.5 V.
14. When $V_{DD2} - V_E > V_{UVLO}$ and output state V_O is allowed to go high, the DESAT detection feature is active and provides the primary source of IGBT protection. UVLO is needed to ensure DESAT detection is functional.
15. The blanking time, t_{BLANK}, is adjustable by an external capacitor (C_{BLANK}), where $t_{BLANK} = C_{BLANK} \times (V_{DESAT} / I_{CHG})$.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions, typical value is measured at V_{DD1} = 5 V, $V_{DD2} - V_{SS}$ = 30 V, $V_E - V_{SS}$ = 0 V, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay Time to Logic Low Output (Note 17)	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50% (Note 16)	–	140	250	ns	19, 20, 21, 22, 23, 24, 42, 50
t_{PLH}	Propagation Delay Time to Logic High Output (Note 18)		–	160	250	ns	
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$ (Note 19)		–	20	100	ns	
PDD Skew	Propagation Delay Difference between Any Two Parts or Channels, ($t_{PHL} - t_{PLH}$) (Note 20)		−150	–	150	ns	
t_R	Output Rise Time (10% to 90%)		–	25	–	ns	42, 50
t_F	Output Fall Time (90% to 10%)		–	25	–	ns	
$t_{DESAT(90\%)}$	DESAT Sense to 90% V_O Delay (Note 21)	Rg = 10 Ω, Cg = 10 nF, $V_{DD2} - V_{SS}$ = 30 V	–	450	700	ns	25, 43
$t_{DESAT(10\%)}$	DESAT Sense to 10% V_O Delay (Note 21)		–	2.7	4	μs	26, 28, 29, 43
$t_{DESAT(\overline{FAULT})}$	DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay (Note 22)		–	1.4	5	μs	27, 43, 51
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay (Note 23)		–	250	–	ns	43
$t_{\overline{RESET}(\overline{FAULT})}$	$\overline{RESET}$ to High Level $\overline{FAULT}$ Signal Delay (Note 24)		3	6	20	μs	30, 44, 51
$t_{DESAT(MUTE)}$	DESAT Input Mute		10	22	35	μs	
$PW_{\overline{RESET}}$	$\overline{RESET}$ Signal Pulse Width		1.2	–	–	μs	
$t_{UVLO\ ON}$	UVLO Turn On Delay (Note 25)	V_{DD2} = 20 V in 1.0 ms Ramp	–	4	–	μs	31, 45
$t_{UVLO\ OFF}$	UVLO Turn Off Delay (Note 26)		–	3	–	μs	
t_{GP}	Time to Good Power (Note 27)	V_{DD2} = 0 to 30 V in 10 μs Ramp	–	2.5	–	μs	32, 33, 45
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 25 V, V_{SS} = Ground, V_{CM} = 1500 Vpk (Note 28)	35	50	–	kV/μs	47, 48
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 25 V, V_{SS} = Ground, V_{CM} = 1500 Vpk (Note 29)	35	50	–	kV/μs	46, 49

16. This load condition approximates the gate load of a 1200 V / 150 A IGBT.
17. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse (V_{IN+}, V_{IN-}) to the 50% level of the falling edge of the V_O signal. Refer to Figure 50.
18. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse (V_{IN+}, V_{IN-}) to the 50% level of the rising edge of the V_O signal. Refer to Figure 50.
19. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
20. The difference between t_{PHL} and t_{PLH} between any two FOD8316 parts under same operating conditions with equal loads.
21. This is the amount of time the DESAT threshold must be exceeded before V_O begins to go LOW. This is supply voltage dependent. See Figure 51.
22. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes LOW. See Figure 51.
23. The length of time the DESAT threshold must be exceeded before V_O begins to go LOW, and the FAULT output begins to go LOW. See Figure 51.
24. The length of time from when RESET is asserted LOW, until FAULT output goes HIGH. See Figure 51.

25. The UVLO turn−on delay, $t_{UVLO\ ON}$, is measured from V_{UVLO+} threshold voltage of the output supply voltage (V_{DD2}) to the 5 V level of the rising edge of the V_O signal.
26. The UVLO turn−off delay, $t_{UVLO\ OFF}$, is measured from V_{UVLO-} threshold voltage of the output supply voltage (V_{DD2}) to the 5 V level of the falling edge of the V_O signal.
27. The time to good power, t_{GP}, is measured from 13.5 V level of the rising edge of the output supply voltage (V_{DD2}) to the 5 V level of the rising edge of the V_O signal.
28. Common−mode transient immunity at output HIGH state is the maximum tolerable negative dVCM/dt on the trailing edge of the common−mode pulse, V_{CM}, to assure the output will remain in HIGH state (i.e., V_O > 15 V or FAULT > 2 V).
29. Common−mode transient immunity at output LOW state is the maximum positive tolerable dVCM/dt on the leading edge of the common−mode pulse, V_{CM}, to assure the output will remain in LOW state (i.e., V_O < 1.0 V or FAULT < 0.8 V).

TYPICAL PERFORMANCE CHARACTERISTICS

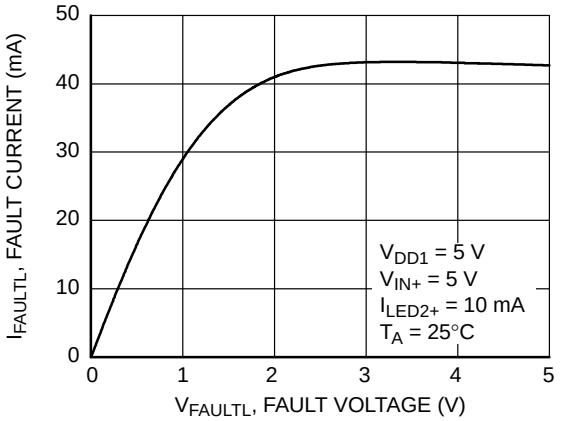

Figure 3. FAULT Logic Low Output Current ($I_{\overline{FAULTL}}$) vs. FAULT Logic Low Output Voltage ($V_{\overline{FAULTL}}$)

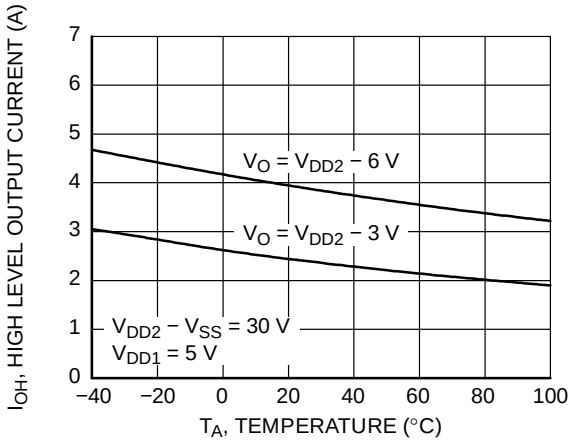

Figure 4. High Level Output Current (I_{OH}) vs. Temperature

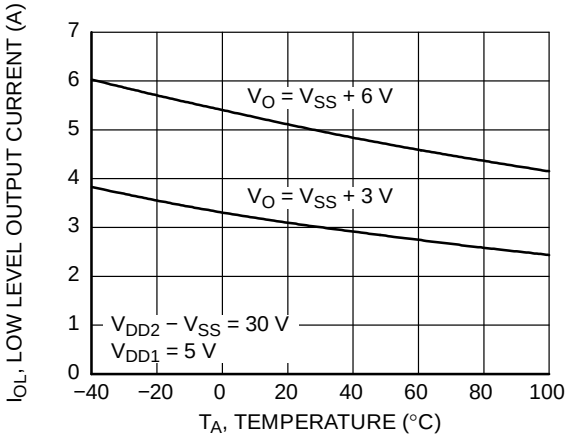

Figure 5. Low Level Output Current (I_{OL}) vs. Temperature

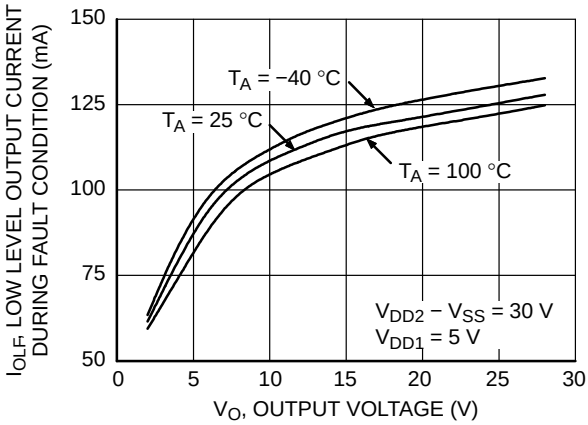

Figure 6. Low Level Output Current During Fault Condition (I_{OLF}) vs. Output Voltage (V_{OL})

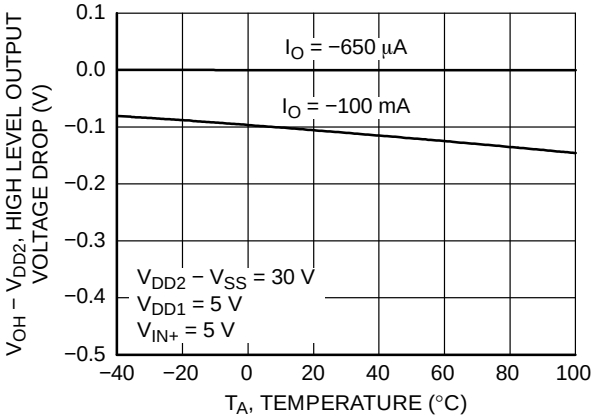

Figure 7. High Level Output Voltage Drop (V_{OH} − V_{DD}) vs. Temperature

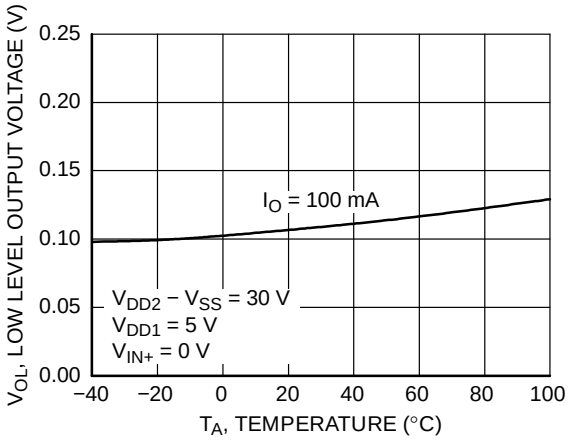

Figure 8. Low Level Output Voltage (V_{OL}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

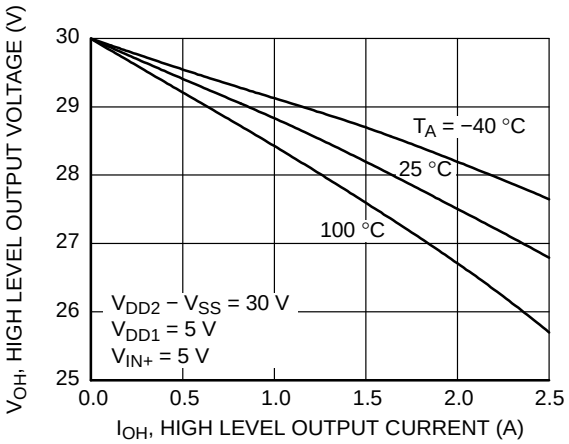

Figure 9. High Level Output Voltage (V_{OH}) vs. High Level Output Current (I_{OH})

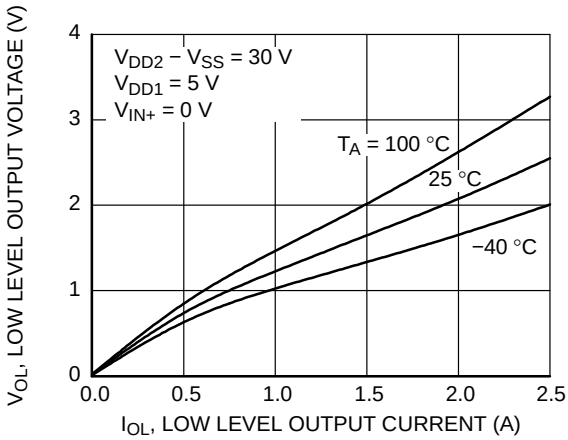

Figure 10. Low Level Output Voltage (V_{OL}) vs. Low Level Output Current (I_{OL})

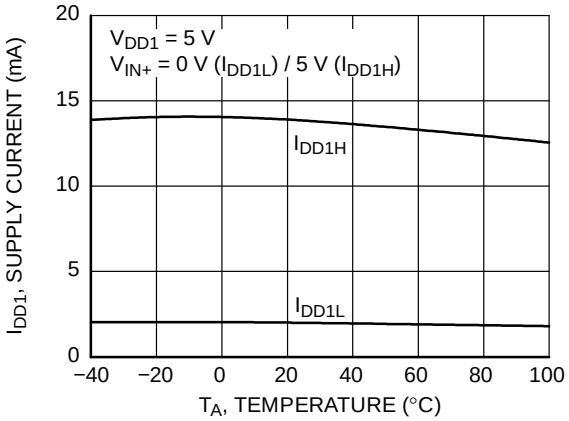

Figure 11. Supply Current (I_{DD1}) vs. Temperature

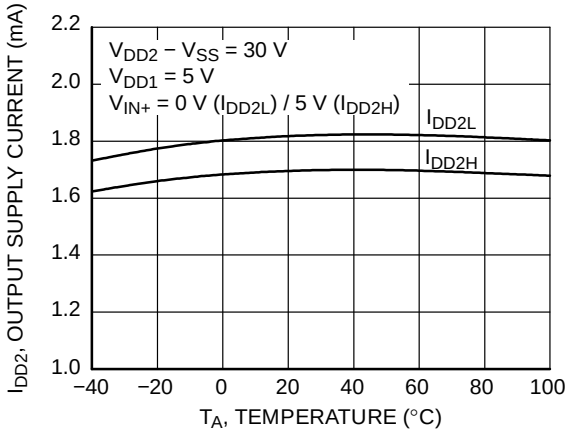

Figure 12. Output Supply Current (I_{DD2}) vs. Temperature

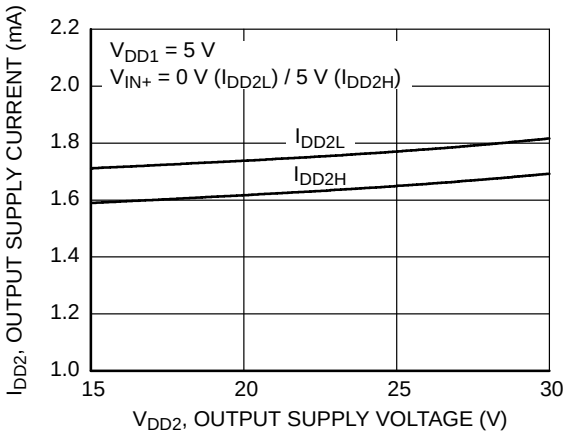

Figure 13. Output Supply Current (I_{DD2}) vs. Output Supply Voltage (V_{DD2})

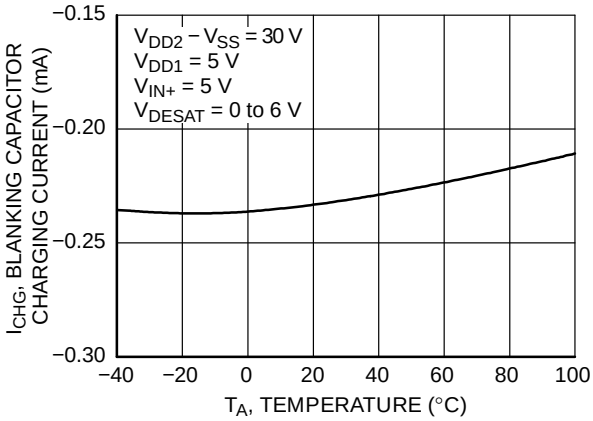

Figure 14. Blanking Capacitor Charge Current (I_{CHG}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

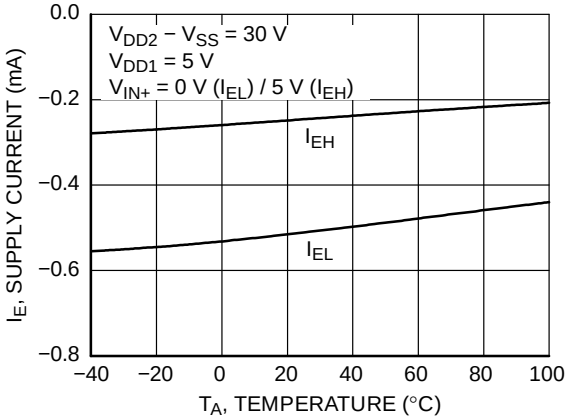

Figure 15. Supply Current (I_E) vs. Temperature

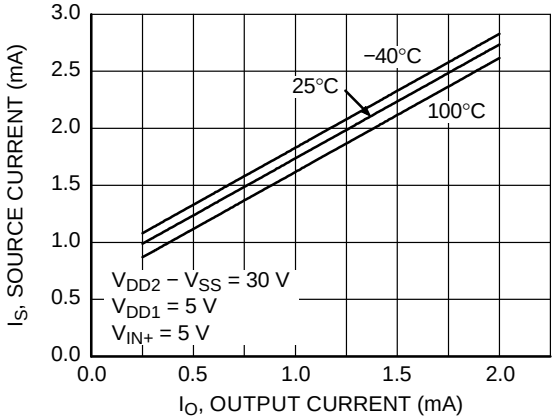

Figure 16. Source Current (I_S) vs. Output Current (I_O)

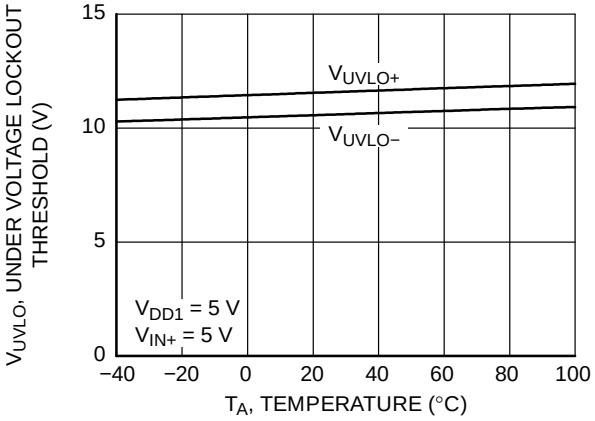

Figure 17. Under Voltage Lockout Threshold (V_{UVLO}) vs. Temperature

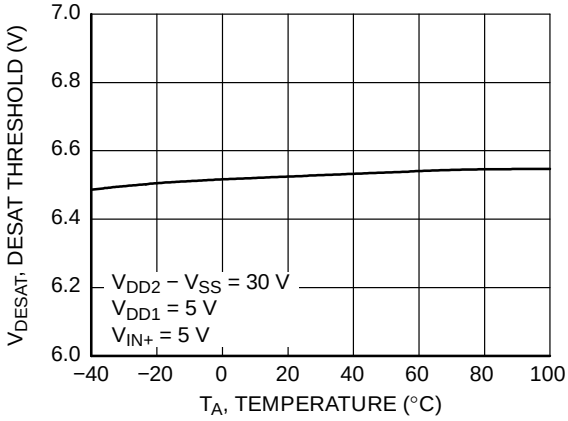

Figure 18. DESAT Threshold (V_{DESAT}) vs. Temperature

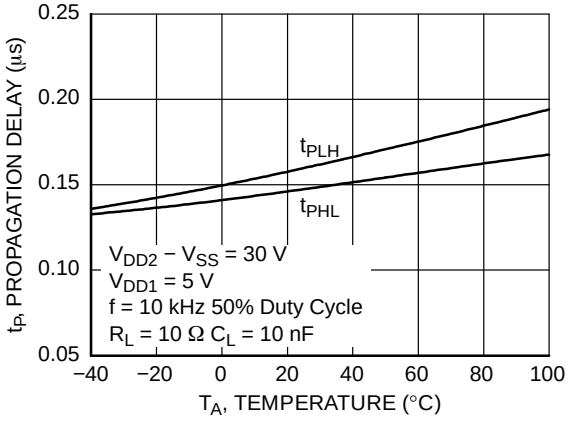

Figure 19. Propagation Delay (t_P) vs. Temperature

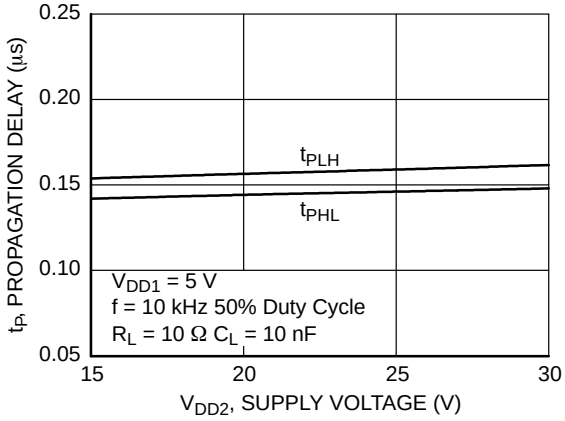

Figure 20. Propagation Delay (t_P) vs. Supply Voltage (V_{DD2})

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

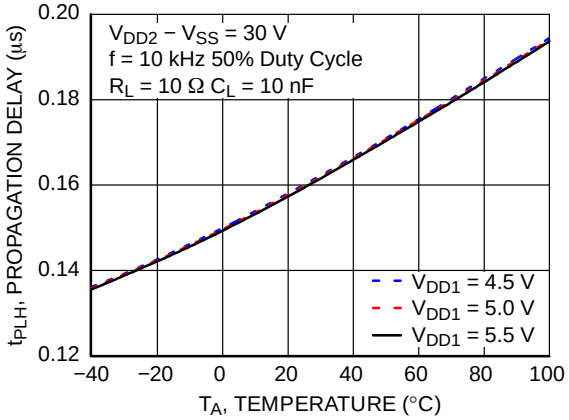

Figure 21. Propagation Delay Time to Logic High Output (t_{PLH}) vs. Temperature

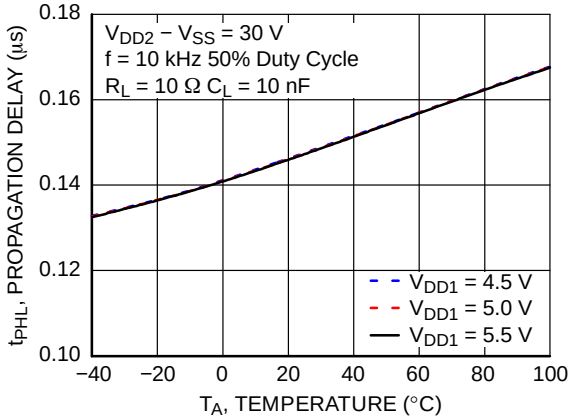

Figure 22. Propagation Delay Time to Logic Low Output (t_{PHL}) vs. Temperature

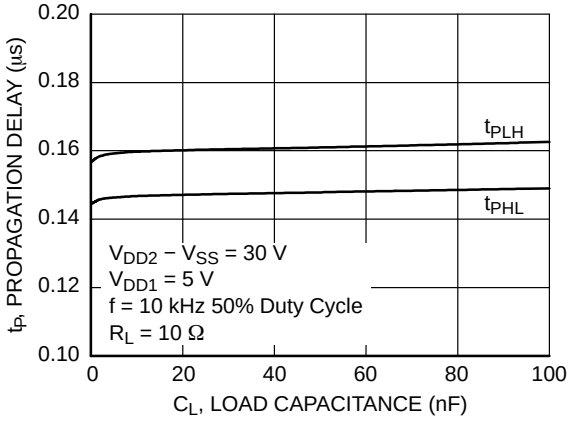

Figure 23. Propagation Delay (t_P) vs. Load Capacitance (C_L)

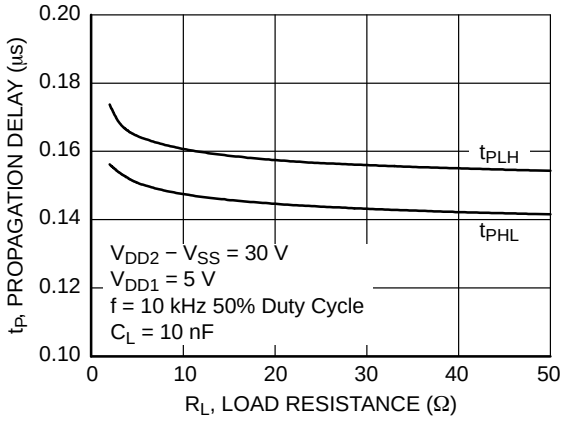

Figure 24. Propagation Delay (t_P) vs. Load Resistance (R_L)

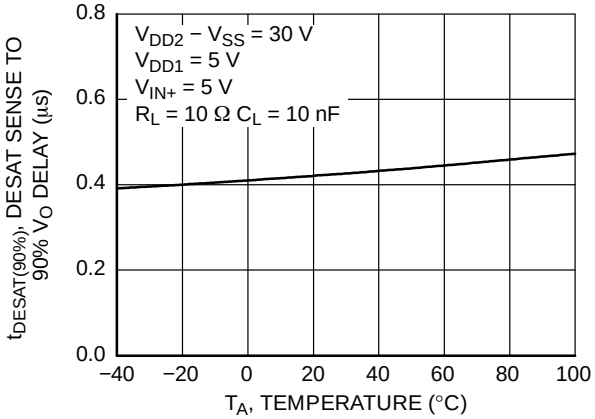

Figure 25. DESAT Sense to 90% V_O Delay ($t_{DESAT(90\%)}$) vs. Temperature

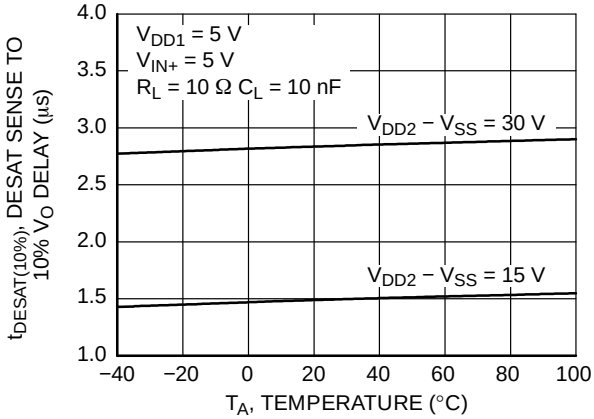

Figure 26. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

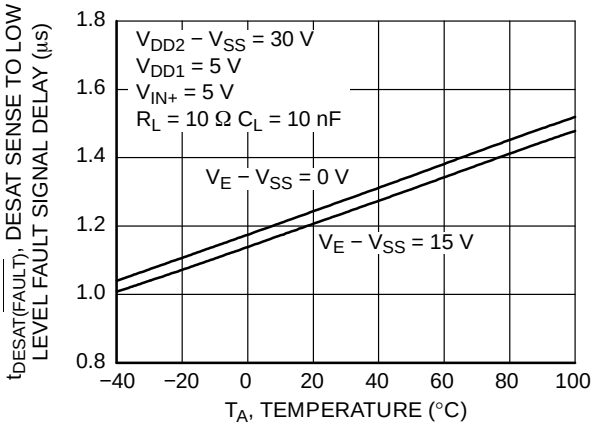

Figure 27. DESAT Sense to Low Level FAULT Signal Delay ($t_{DESAT(\overline{FAULT})}$) vs. Temperature

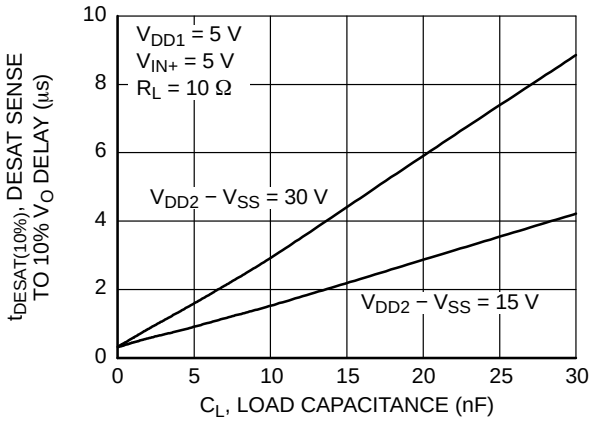

Figure 28. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Capacitance (C_L)

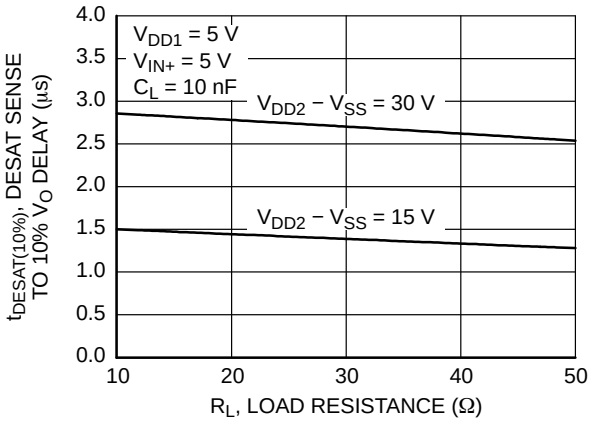

Figure 29. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Resistance (R_L)

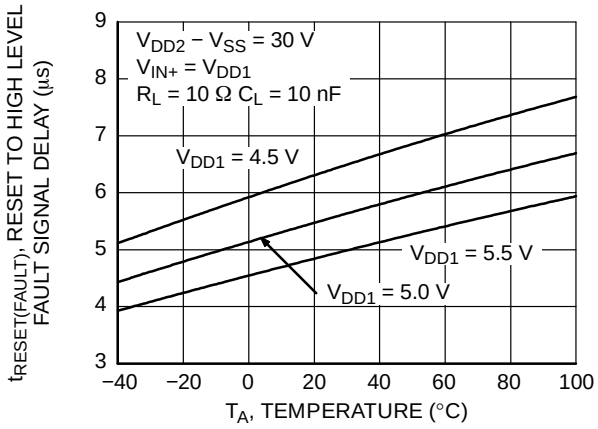

Figure 30. RESET to High Level FAULT Signal Delay ($t_{RESET(\overline{FAULT})}$) vs. Temperature

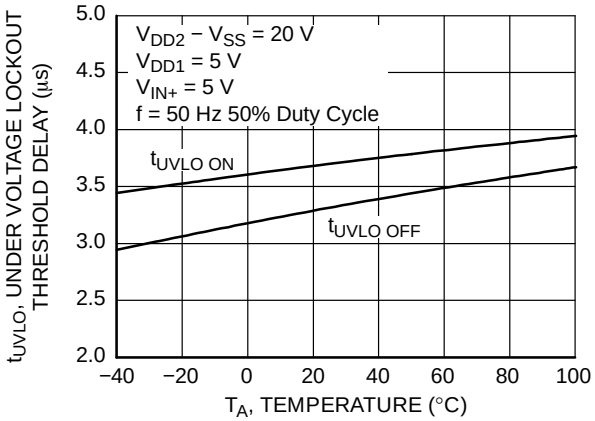

Figure 31. Under Voltage Lockout Threshold Delay (t_{UVLO}) vs. Temperature

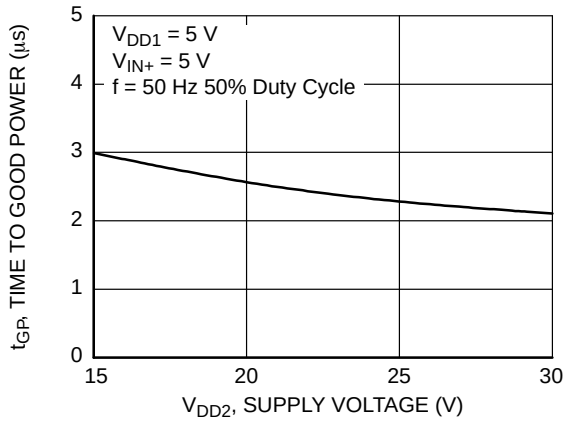

Figure 32. Time to Good Power (t_{GP}) vs. Supply Voltage (V_{DD2})

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

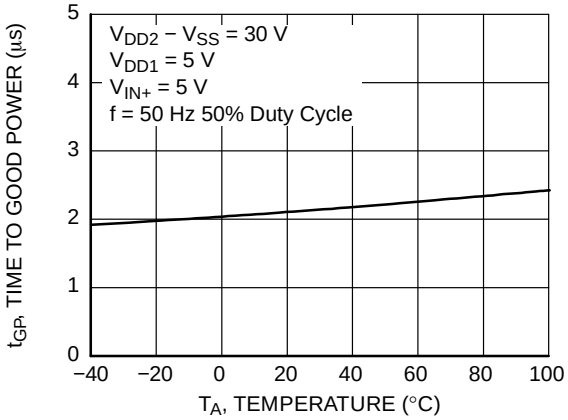

Figure 33. Time to Good Power (t_{GP}) vs. Temperature

TEST CIRCUITS

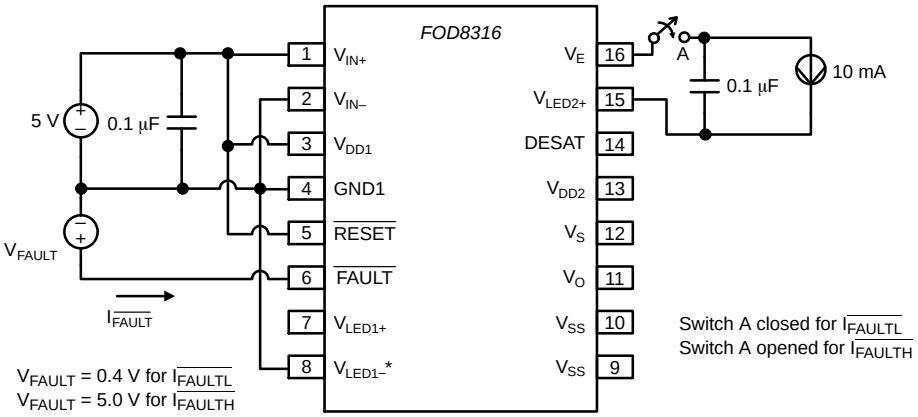

Figure 34. Fault Output Current ($I_{\overline{FAULTL}}$) and ($I_{\overline{FAULTH}}$) Test Circuit

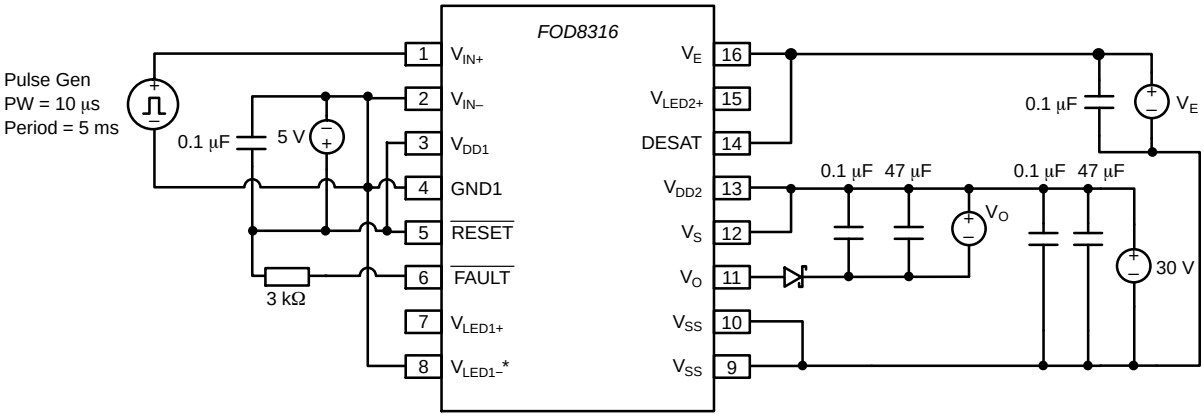

Figure 35. High Level Output Current (I_{OH}) Test Circuit

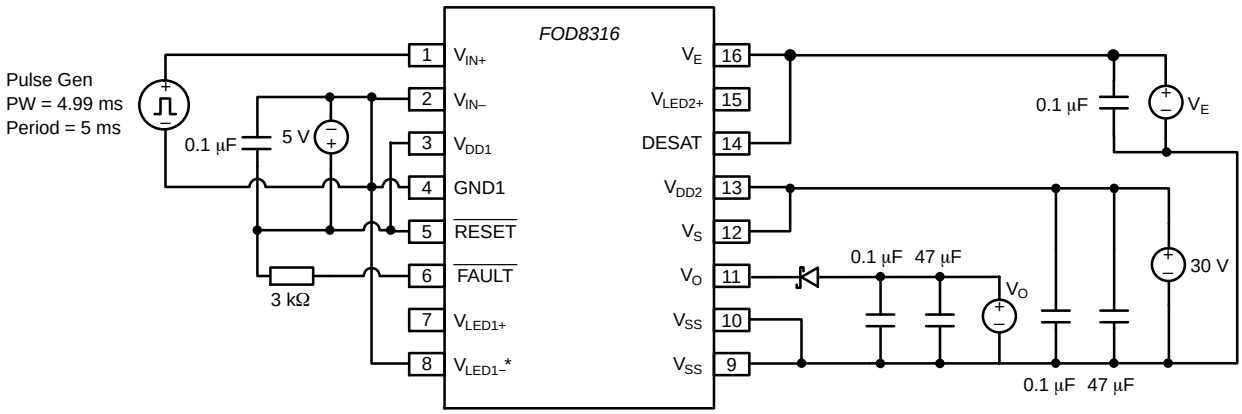

Figure 36. Low Level Output Current (I_{OL}) Test Circuit

TEST CIRCUITS (CONTINUED)

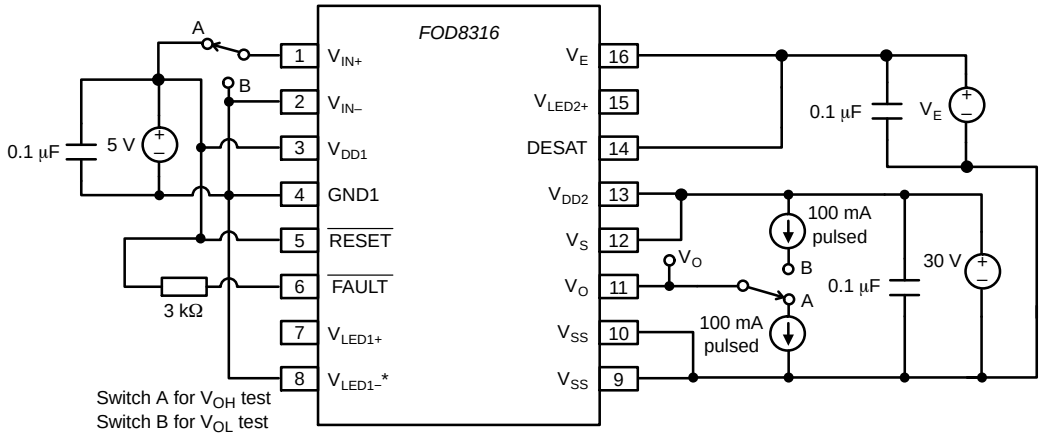

Figure 37. High Level (V_{OH}) and Low Level (V_{OL}) Output Voltage Test Circuit

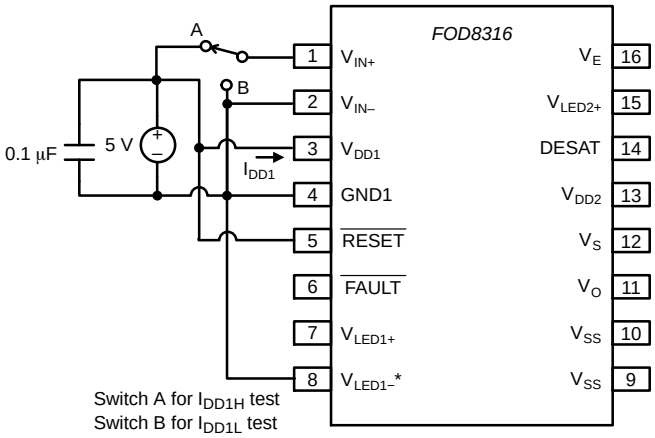

Figure 38. High Level (I_{DD1H}) and Low Level (I_{DD1L}) Supply Current Test Circuit

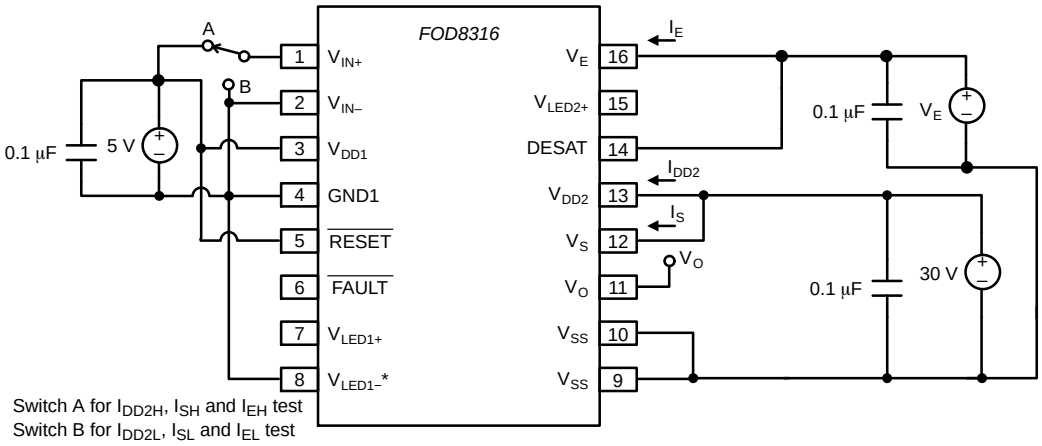

Figure 39. High Level (I_{DD2H}), Low Level (I_{DD2L}) Output Supply Current, High Level (I_{SH}), Low Level (I_{SL}) Source Current, V_E High Level (I_{EH}), and V_E Low Level (I_{EL}) Supply Current Test Circuit

TEST CIRCUITS (CONTINUED)

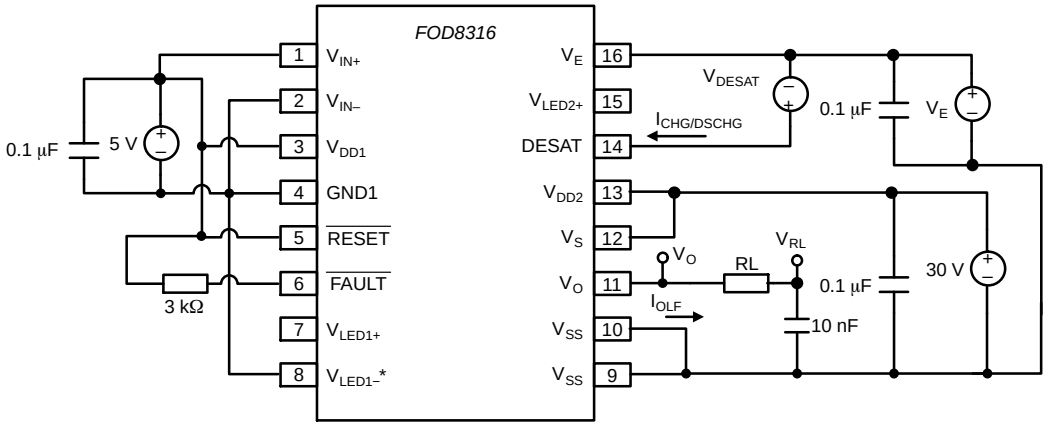

Figure 40. Low Level Output Current During Fault Conditions (I_{OLF}), Blanking Capacitor Charge Current (I_{CHG}), Blanking Capacitor Discharging Current (I_{DSCHG}) and DESAT Threshold (V_{DESAT}) Test Circuit

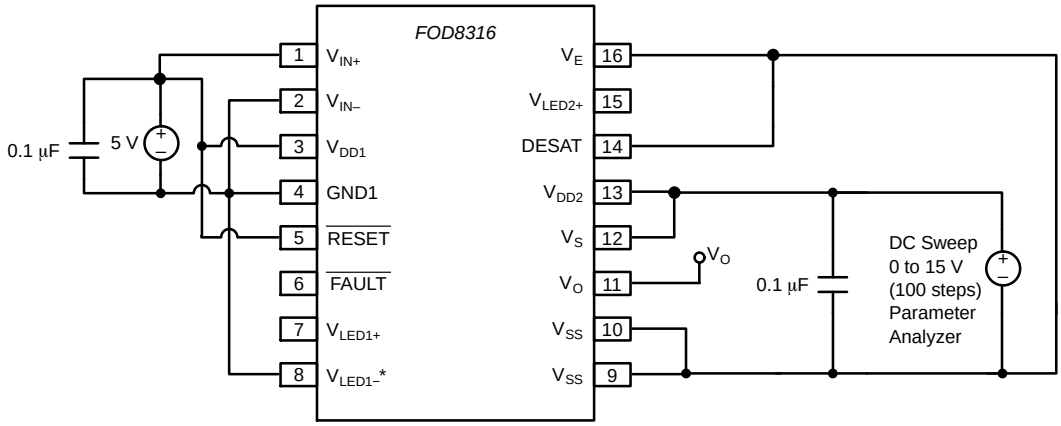

Figure 41. Under Voltage Lockout Threshold (V_{UVLO}) Test Circuit

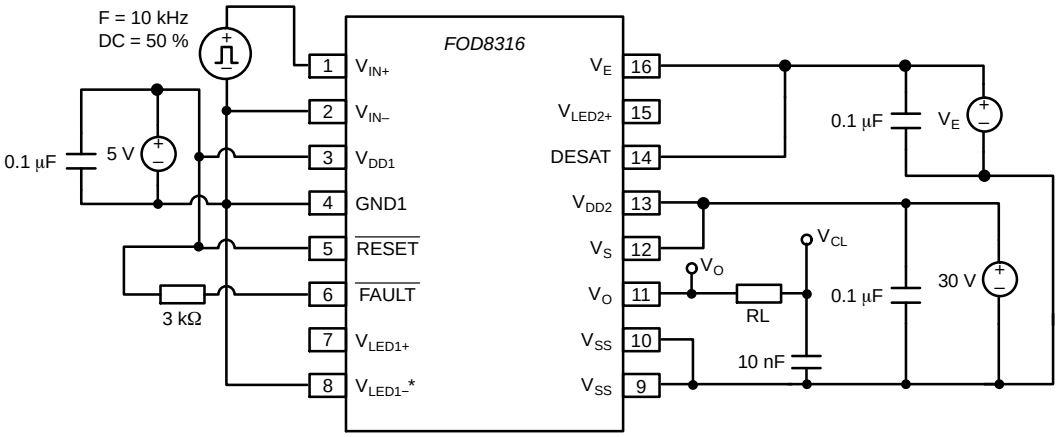

Figure 42. Propagation Delay (t_{PLH}, t_{PHL}), Pulse Width Distortion (PWD), Rise Time (t_R) and Fall Time (t_F) Test Circuit

TEST CIRCUITS (CONTINUED)

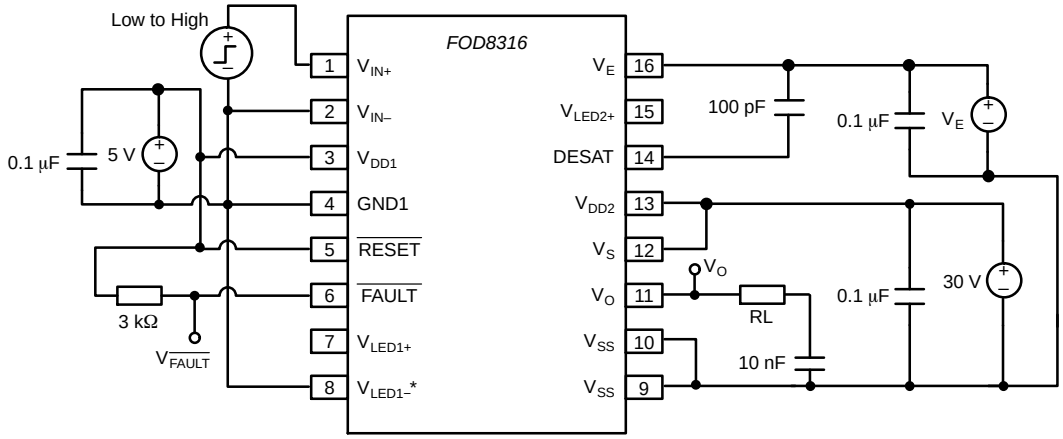

Figure 43. DESAT Sense ($t_{DESAT(90\%)}$, $t_{DESAT(10\%)}$), DESAT Fault ($t_{DESAT(\overline{FAULT})}$), and ($t_{DESAT(LOW)}$) Test Circuit

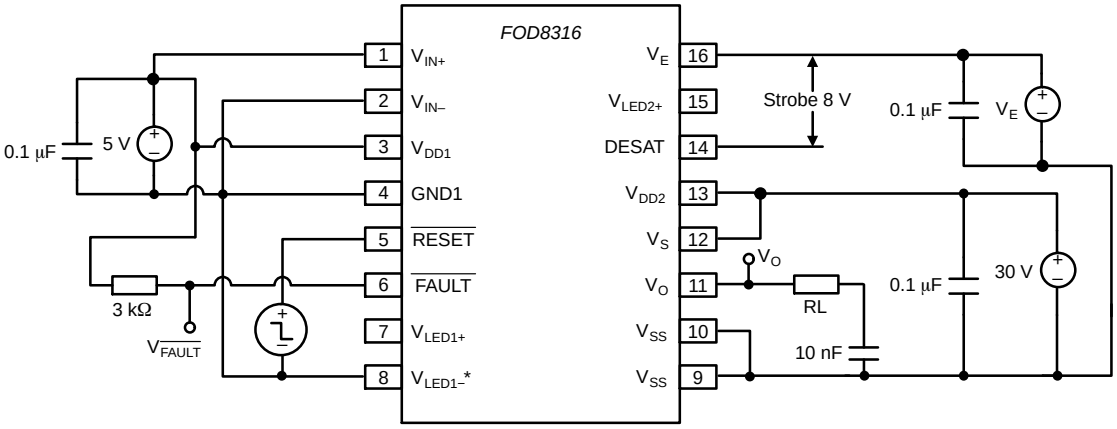

Figure 44. Reset Delay ($t_{\overline{RESET}(\overline{FAULT})}$) Test Circuit

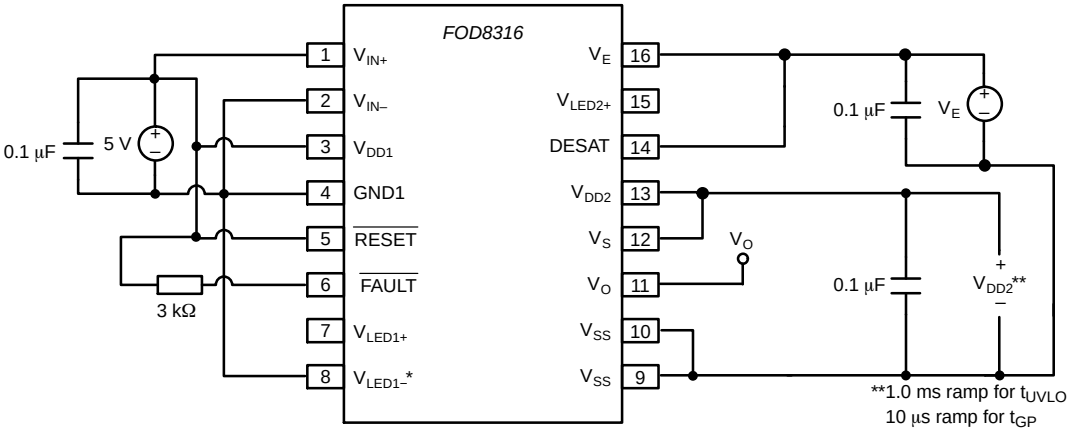

Figure 45. Under Voltage Lockout Delay (t_{UVLO}) and Time to Good Power (t_{GP}) Test Circuit

TEST CIRCUITS (CONTINUED)

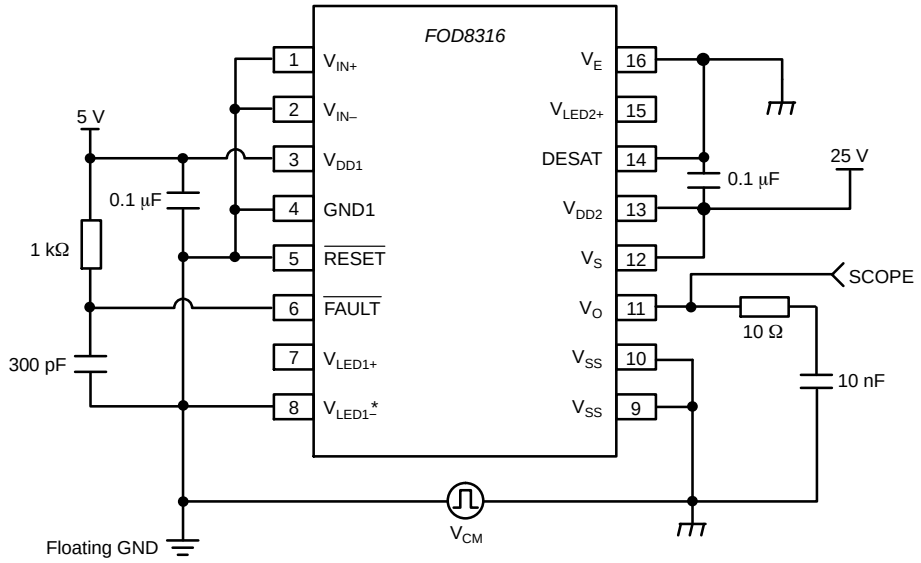

Figure 46. Common Mode Low (CM_L) Test Circuit @ LED1 Off

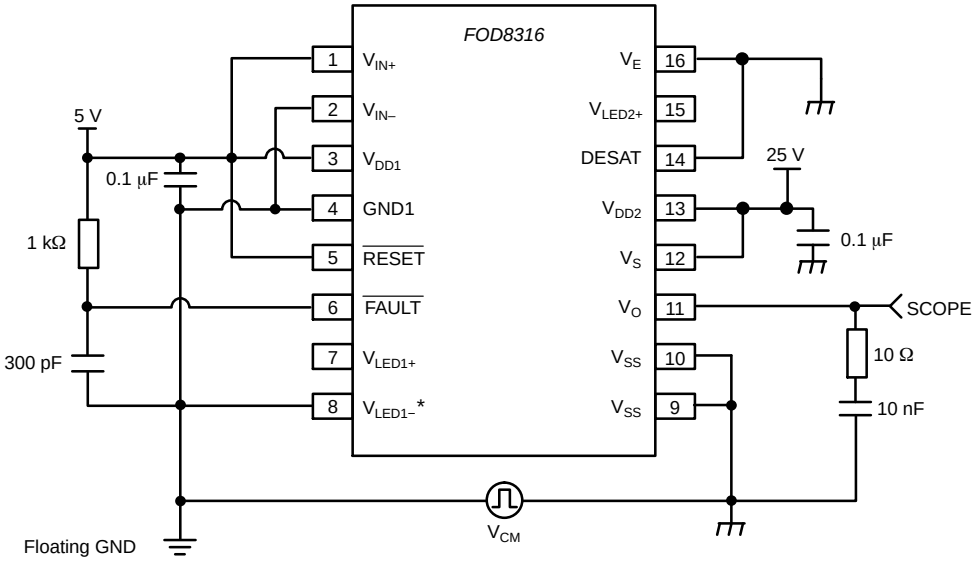

Figure 47. Common Mode High (CM_H) Test Circuit @ LED1 On

TEST CIRCUITS (CONTINUED)

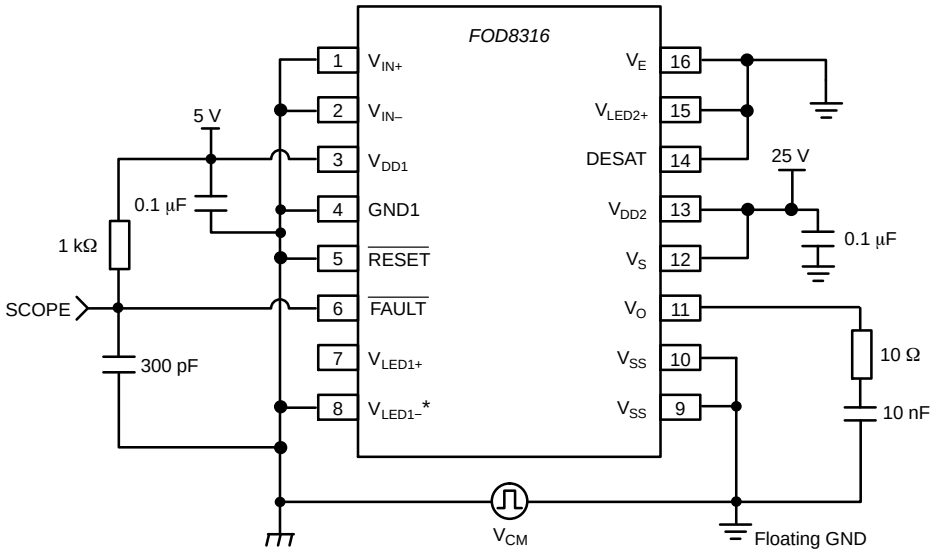

Figure 48. Common Mode High (CM_H) Test Circuit @ LED2 Off

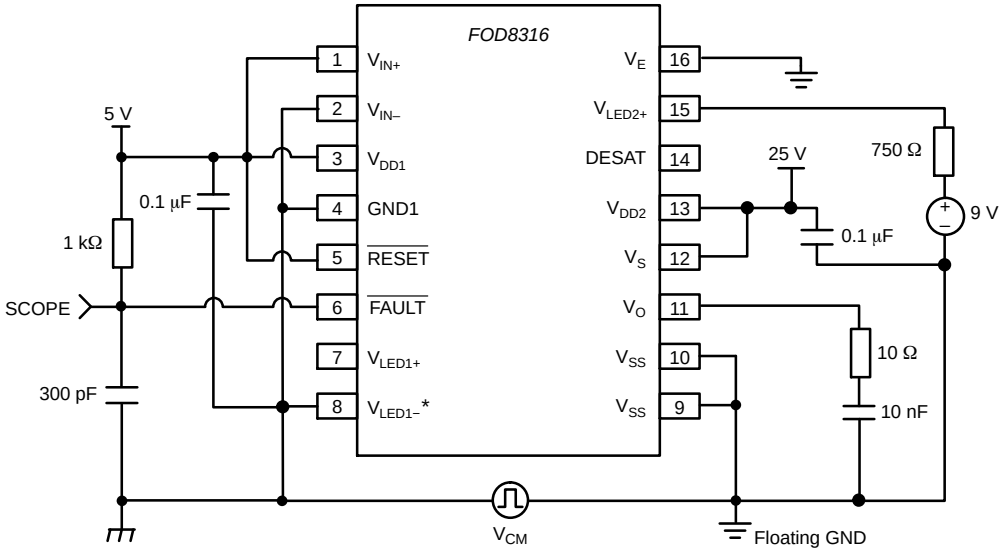

Figure 49. Common Mode Low (CM_L) Test Circuit @ LED2 On

TIMING DIAGRAMS

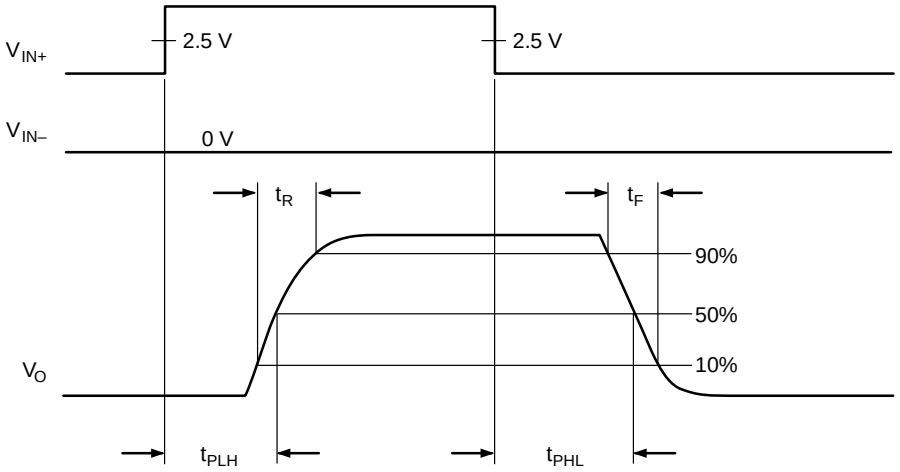

Figure 50. Propagation Delay (t_{PLH}, t_{PHL}), Rise Time (t_R), and Fall Time (t_F) Timing Diagram

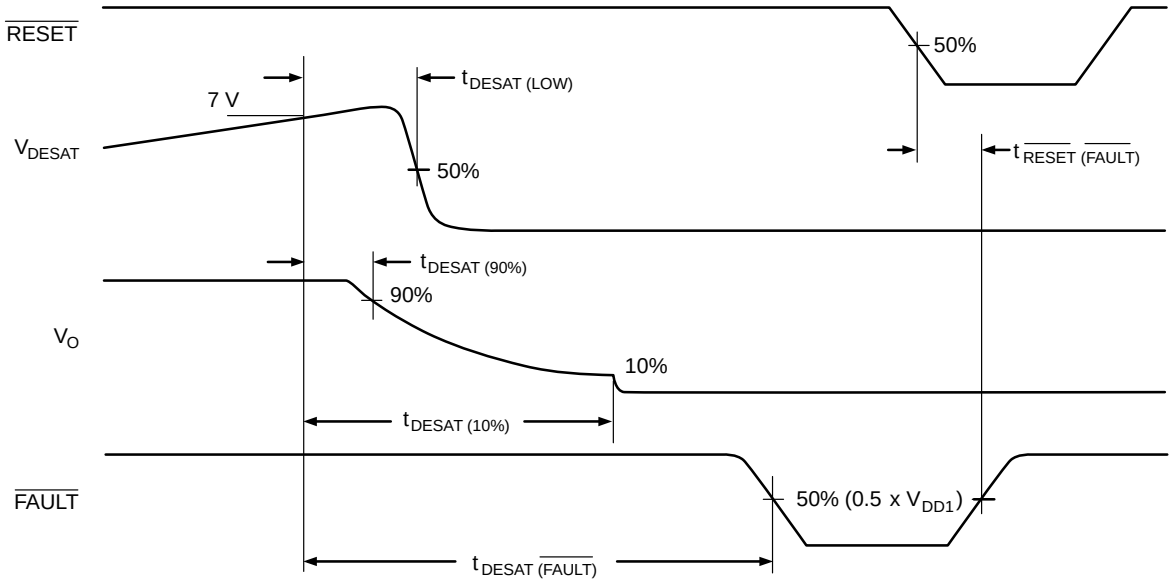

Figure 51. Definitions for Fault Reset Input ($\overline{RESET}$), Desaturation Voltage Input (DESAT), Output Voltage (V_O), and Fault Output ($\overline{FAULT}$) Timing Waveforms

APPLICATION INFORMATION

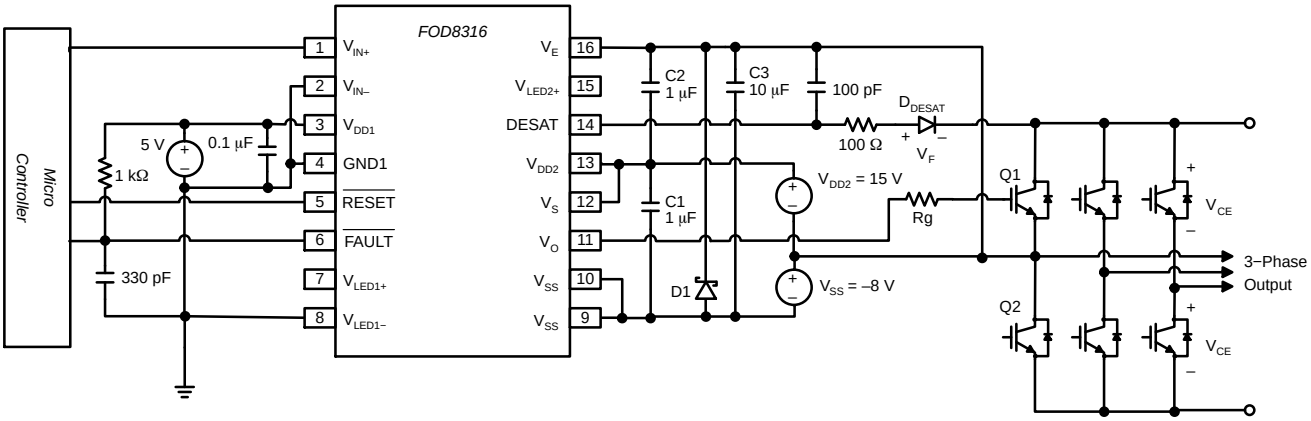

Figure 52. Recommended Application Circuit

Functional Description

The typical application circuit is shown in Figure 52 and the functional behavioral of the FOD8316 is illustrated by the detailed internal schematic shown in Figure 53. This helps explain the interaction and sequence of internal and external signals, together with the timing diagrams.

Non−Inverting and Inverting Inputs

There are two CMOS/TTL compatible inputs, V_{IN+} and V_{IN-} to control the IGBT, in non−inverting and inverting configurations respectively. When V_{IN-} is set to LOW, V_{IN+} controls the driver output, V_O, in non−inverting configuration. When V_{IN+} is set to HIGH, V_{IN-} controls the driver output in inverting configuration.

The relationship between the inputs and output are illustrated in the Figure 54.

During normal operation, when no fault is detected, the $\overline{FAULT}$ output, which is an open−drain configuration, will be latched to HIGH state. This allows the gate driver to be controlled by the input logic signal.

When a fault is detected, the $\overline{FAULT}$ output will be latched to LOW state. This condition will remain until the $\overline{RESET}$ pin is also pulled low for a period longer than $PW_{\overline{RESET}}$. While setting the $\overline{RESET}$ pin to a low state, the input pins must be pulled to low to ensure an output state (V_{IN+} is low or V_{IN-} is HIGH).

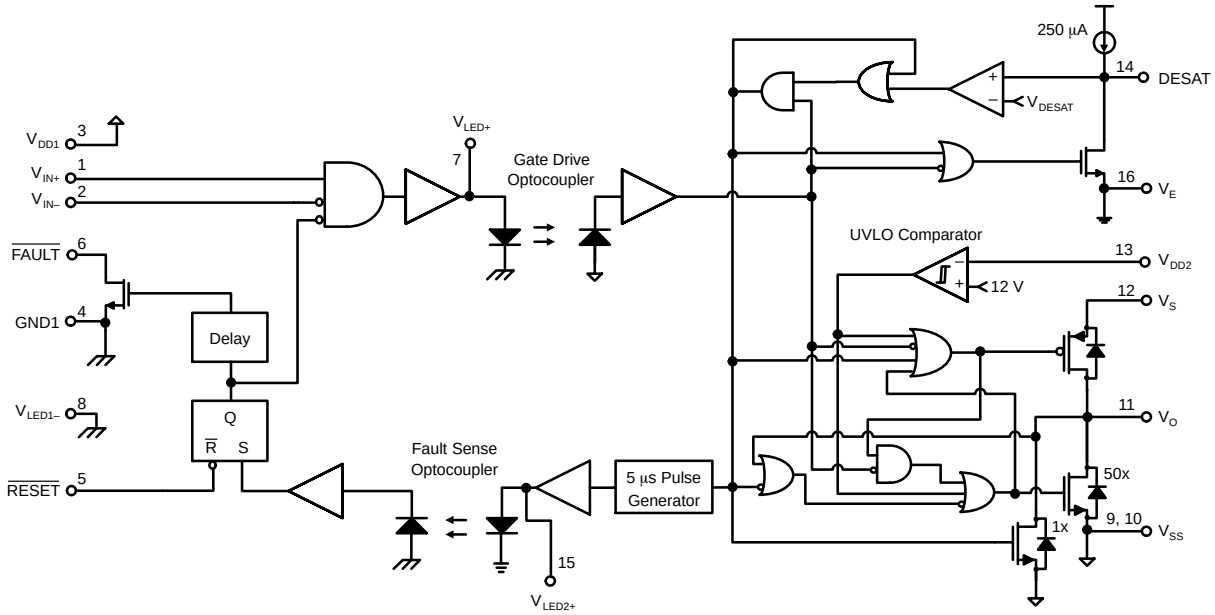

Figure 53. Detailed Internal Schematic

Gate Driver Output

A pair of PMOS and NMOS transistors made up the output driver stage, which facilitates close to rail−to−rail output swing. This feature allows a tight control of gate voltage during on−state and short circuit condition. The output driver is typically capable of sinking 2 A and sourcing 2 A at room temperature. Due to the low $RDS_{(ON)}$ of the MOSFETs, the power dissipation is reduced as compared to those bipolar−type driver output stages. The absolute maximum rating of the output peak current, $I_{O(PEAK)}$ is 3 A, thus the careful selection of the gate resistor, Rg, is required to limit the short circuit current of the IGBT.

As shown in Figure 53, the gate driver output is influenced by signals from the photodetector circuitry, the UVLO comparator, and the DESAT signals. Under no fault condition, normal operation resumes while the supply voltage is above the UVLO threshold, the output of the photodetector will drive the MOSFETs of the output stage.

The logic circuitry of the output stage will ensure that the push−pull devices will never be turned “ON” simultaneously. When the output of the photodetector is HIGH, the output, V_O will be pulled to HIGH state by turning on the PMOS. When the output of the photodetector is LOW, V_O will be pulled to LOW state by turning on the NMOS.

When V_{DD2} supply goes below V_{UVLO}, which is the designated ULVO threshold at the comparator, V_O will be pulled down to LOW state regardless of photodetector output.

When desaturation is detected, V_O will turn off slowly as it is pulled low by the 1XNMOS device, the input to the Fault Sense circuitry will be latched to HIGH state and turns on the LED. When V_O goes below 2 V, the 50XNMOS device turns on again, clamping the IGBT gate firmly to V_{SS}. The Fault Sense signal will remain latched in the HIGH state until the LED of the gate driver circuitry turns off.

Desaturation Protection, FAULT Output

Desaturation detection protection ensures the protection of the IGBT at short circuit by monitoring the collector−emitter voltage of the IGBT in the half bridge. When the DESAT voltage goes up and reaches above the threshold voltage, a short circuit condition is detected and the driver output stage will execute a “soft” IGBT turn−off and will be eventually driven low. This sequence is illustrated in Figure 55. The $\overline{FAULT}$ open−drain output is triggered active low to report a desaturation error. It could only be cleared by activating active low by the external controller to the $\overline{RESET}$ input.

The DESAT fault detector should be disabled for a short time period (blanking time) before the IGBT turns on to allow the collector voltage to fall below DESAT threshold. This blanking period protects against false trigger of the DESAT while the IGBT is turning on.

“Soft” Turn−Off

The soft turn−off feature ensures the safe turn off of the IGBT under fault condition. This reduces the voltage spike on the collector of the IGBT. Without this, the IGBT would see a heavy spike on the collector, resulting in a permanent damage to the device when it’s turned off immediately.

“Under Voltage Lockout (UVLO)

Under voltage detection prevents the application of insufficient gate voltage to the IGBT. This could be dangerous, as it would drive the IGBT out of saturation and into the linear operation where the losses are very high and quickly overheats. This feature ensures proper operating of the IGBTs. The output voltage, V_O, remains LOW irregardless of the inputs, as long as the supply voltage, $V_{DD2} - V_E$, is less than V_{ULVO+}. When the supply voltage falls below V_{ULVO-}, V_O goes LOW, as illustrated in Figure 56.

Time to Good Power

At initial power up, the LED is off and the output of the gate driver should be in the LOW or OFF state. Sometimes race conditions exist that cause the output to follow V_D (assuming V_{DD2} and V_E are connected externally), until all of the circuits in the output IC have stabilized. This condition can result in output transitions or transients that are coupled to the driven IGBT. These transients can cause the high− and low−side IGBTs to conduct shoot−through current that can damage power semiconductor devices.

ON has introduced an initial turn−on delay, called “time to good power”. This delay, typically 2.5 μs, is only present during the initial power−up of the device. Once powered, the “time to good power” delay is determined by the delay of the UVLO circuitry. If the LED is ON during the initial turn−on activation, low−to−high transition at the output of the gate driver will only occur 2.5 μs after the V_{DD2} power is applied.

Dual Supply Operation − Negative Bias at V_{SS}

The IGBT’s off−state noise immunity can be enhanced by providing a negative gate−to−emitter bias when the IGBT is in the OFF state. This static off−state bias can be supplied by connecting a separate negative voltage source between the V_E (pin 16) and V_{SS} (pin 9 & 10). Figure 53 illustrates the two distinct grounds. The primary ground reference is the IGBT’s emitter connection. V_E (pin 16). The under−voltage threshold and desaturation voltage detection are referenced to the IGBT’s emitter (V_E) ground.

The recommended application circuit, Figure 52, shows the interconnection of the V_{DD2} and V_E supplies. The IGBT’s gate to emitter voltage is the absolute value sum of the V_{DD2} supply and the V_{SS} reverse bias. The negative voltage supply at V_{SS} appears at the gate drive input, V_O, when the FOD8316 is in the LOW state. When the input drives the output high, the output voltage, V_O, will have the potential of the V_{DD2} and V_{SS}.

Figure 52 shows the operation with a dual or split power supply. The Vss supply provides the negative gate bias, and $V_{DD2} + V_{SS}$ supplies power to the output IC. The V_{SS} and V_{DD2} supplies require three power supply bypass capacitors. These capacitors provide the low equivalent series resistant (ESR) paths for the instantaneous gate charging and discharging currents. Selecting capacitors with

low ESR will optimize the available output current. C3 is a low ESR 1812 style, 10 µF, multilayer ceramic capacitor. This capacitor is the primary filter for the Vss and V_{DD2} supplies. C1 and C2 are also low ESR capacitors. They provide the primary gate charge and discharge paths. The Schottky diode, D1, is connected between V_E and V_{SS} to protect against a reverse voltage greater than 0.5 V.

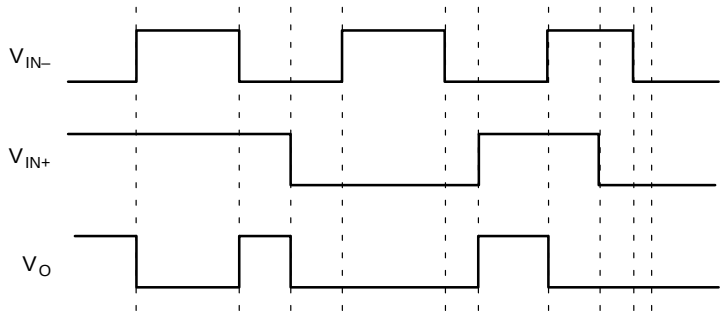

Figure 54. Input/Output Relationship

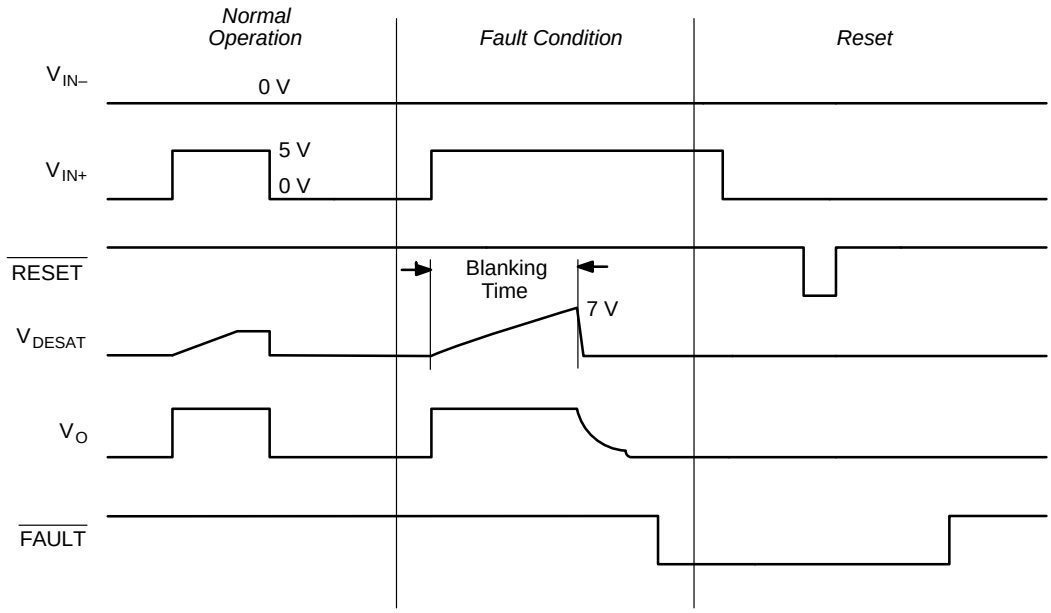

Figure 55. Timing Relationship Among Desaturation Voltage (DESAT), Fault Output ($\overline{FAULT}$) and Fault Reset Input ($\overline{RESET}$)

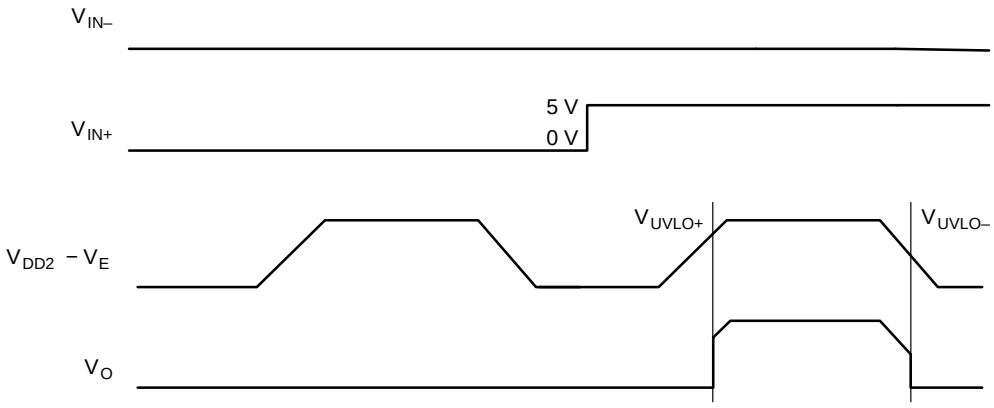

Figure 56. Under Voltage Lockout (UVLO) for Output Side

REFLOW PROFILE

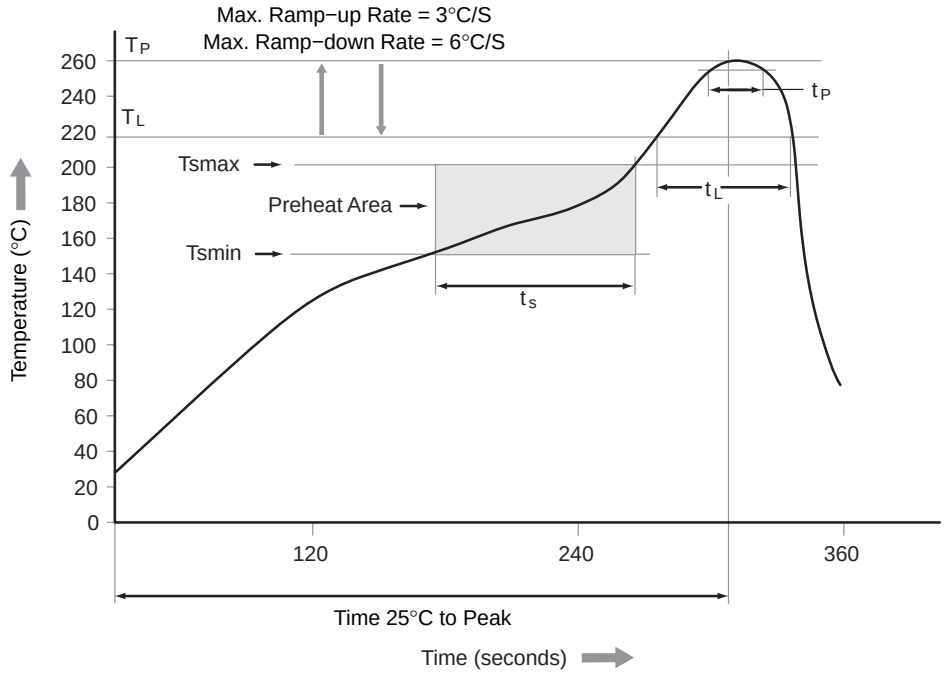

Figure 57. Reflow Profile

Table 1.

Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 to 120 seconds
Ramp−up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp−Down Rate (T_P to T_L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD8316	SOIC16 W, SO 16−Pin (Pb−Free)	50 Units / Tube
FOD8316R2	SOIC16 W, SO 16−Pin (Pb−Free)	750 Units / Tape & Reel
FOD8316V	SOIC16 W, SO 16−Pin, DIN EN/IEC 60747−5−5 Option (Pb−Free)	50 Units / Tube
FOD8316R2V	SOIC16 W, SO 16−Pin, DIN EN/IEC 60747−5−5 Option (Pb−Free)	750 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

30. All packages are lead free per JEDEC: J−STD−020B standard.

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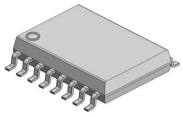

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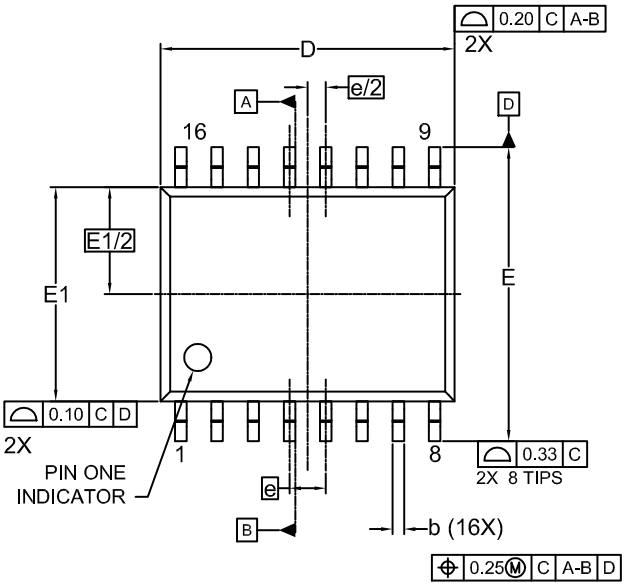

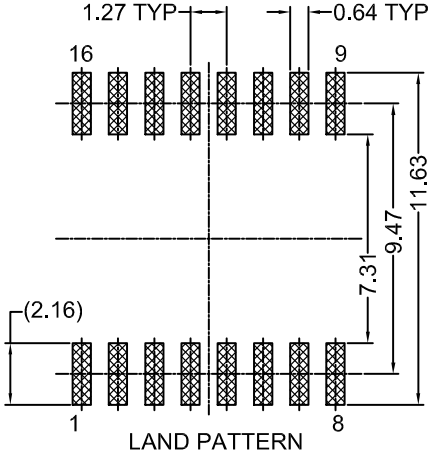

LAND PATTERN
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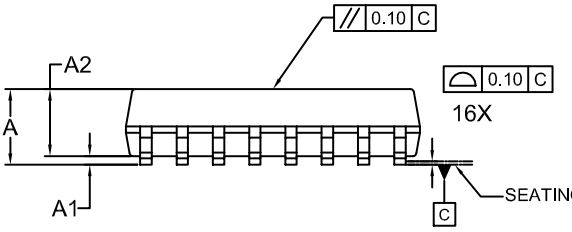
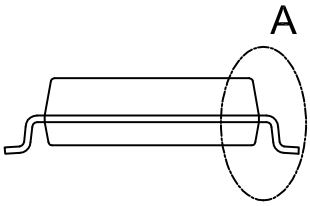
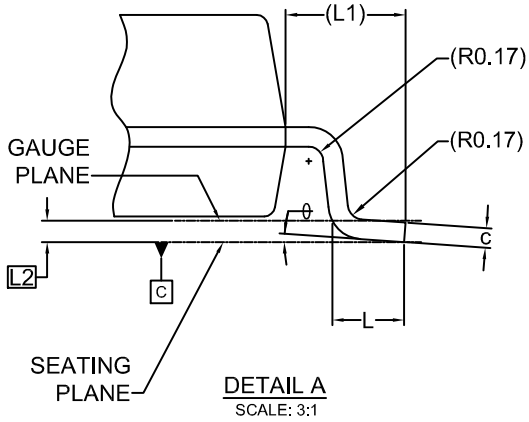
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.







DETAIL A
SCALE: 3:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING REFERS TO JEDEC MS-013, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M-1994
E) LAND PATTERN STANDARD: SOIC127P1030X275-16N
F) DRAWING FILE NAME: MKT-M16FREV2
G) OPTOCOUPLER COMES IN WHITE MOLD BODY.

DIM	MILLIMETER		
	MIN.	NOM.	MAX.
A	–	–	3.00
A1	0.15	0.30	0.45
A2	2.25	2.35	2.45
b	0.31	0.41	0.51
c	0.19	0.22	0.25
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
E1/2	3.75 BSC		
e	1.27 BSC		
e/2	0.635 BSC		
L	0.40	0.84	1.27
L1	1.42 REF		
L2	0.25 BSC		
θ	0°	–	8°

GENERIC MARKING DIAGRAM*

AWLYWW
XXXXXXXXXX
XXXXXXXXXX

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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