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FODM8061

High Noise Immunity, 3.3V/5V, 10Mbit/sec Logic Gate Output (Open Collector) Optocoupler

Features

- High Noise Immunity characterized by common mode transient immunity (CMTi)
 - 20kV/μs Minimum CMTi
- High Speed
 - 10Mbit/sec Data Rate (NRZ)
 - 80ns max. Propagation Delay
 - 25ns max. Pulse Width Distortion
 - 40ns max. Propagation Delay Skew
- 3.3V LVTTTL/LVCMOS Compatibility
- Specifications guaranteed over 3V to 5.5V supply voltage and -40°C to +110°C temperature range
- Safety and regulatory approvals
 - UL1577, 3750 VAC_{RMS} for 1 min.
 - IEC60747-5-2

Applications

- Microprocessor system interface
 - SPI, I²C
- Industrial fieldbus communications
 - DeviceNet, CAN, RS485
- Programmable logic control
- Isolated data acquisition system
- Voltage level translator
- Isolating MOSFET/IGBT gate drivers

Description

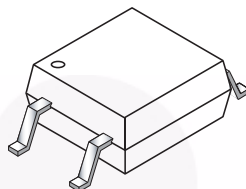
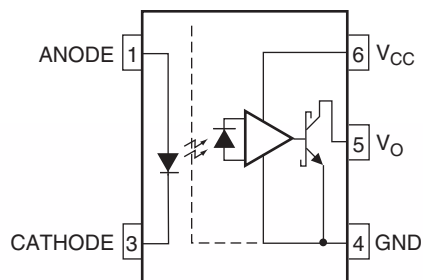
The FODM8061 is a 3.3V/5V high-speed logic gate output (open collector) optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode transient immunity specifications.

This optocoupler consists of an AlGaAS LED at the input, optically coupled to a high speed integrated photo-detector logic gate. The output of the detector IC is an open collector schottky-clamped transistor. The coupled parameters are guaranteed over the wide temperature range of -40°C to +110°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/FO/FODM611.html
- www.fairchildsemi.com/pf/FO/FODM8071.html

Functional Schematic



Truth Table

LED	Output
Off	High
On	Low

Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V _O	Output Voltage
6	V _{CC}	Output Supply Voltage

Safety and Insulation Ratings for Mini-Flat Package (SO5 Pin)

As per IEC60747-5-2. This optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For rated main voltage < 150Vrms		I-IV		
	For rated main voltage < 300Vrms		I-III		
	Climatic Classification		40/110/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V _{PR}	Input to Output Test Voltage, Method b, V _{IORM} x 1.875 = V _{PR} , 100% Production Test with t _m = 1 sec, Partial Discharge < 5 pC	1060			
V _{PR}	Input to Output Test Voltage, Method a, V _{IORM} x 1.5 = V _{PR} , Type and Sample Test with t _m = 60 sec, Partial Discharge < 5 pC	848			
V _{IORM}	Max Working Insulation Voltage	565			V _{peak}
V _{IOTM}	Highest Allowable Over Voltage	4000			V _{peak}
	External Creepage	5.0			mm
	External Clearance	5.0			mm
	Insulation thickness	0.5			mm
T _{Case}	Safety Limit Values, Maximum Values allowed in the event of a failure, Case Temperature	150			°C
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500V	10 ⁹			Ω

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +110	$^\circ\text{C}$
T_J	Junction Temperature	-40 to +125	$^\circ\text{C}$
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10sec	$^\circ\text{C}$
I_F	Forward Current	50	mA
V_R	Reverse Voltage	5.0	V
V_{CC}	Supply Voltage	0 to 7.0	V
V_O	Output Voltage	-0.5 to $V_{CC}+0.5$	V
I_O	Average Output Current	50	mA
PD_I	Input Power Dissipation ⁽¹⁾⁽²⁾	100	mW
PD_O	Output Power Dissipation ⁽¹⁾⁽²⁾	85	mW

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+110	$^\circ\text{C}$
V_{CC}, V_{DD}	Supply Voltages ⁽³⁾	3.0	5.5	V
V_{FL}	Logic Low Input Voltage	0	0.8	V
I_{FH}	Logic High Input Current ⁽⁴⁾	6.3	15	mA
I_{FL}	Logic Low Input Current		250	μA
N	Fan Out (at $R_L = 1\text{k}\Omega$)		5	TTL Loads
R_L	Output Pull-up Resistor	330	4k	Ω

Isolation Characteristics ($T_A=25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	freq= 60Hz, t = 1.0min, $I_{I-O} \leq 10\mu\text{A}^{(5)(6)}$	3750			$V_{AC_{RMS}}$
R_{ISO}	Isolation Resistance	$V_{I-O} = 500\text{V}^{(5)}$		10^{12}		Ω
C_{ISO}	Isolation Capacitance	$V_{I-O} = 0\text{V}$, freq=1.0MHz ⁽⁵⁾		0.6		pF

Notes:

- No derate required to 110 $^\circ\text{C}$.
- Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
- 0.1 μF bypass capacitor must be connected between pins 4 and 6.
- Recommended I_{FH} is 9.3mA for operation above $T_A = 100^\circ\text{C}$.
- Device is considered a two terminal device: Pins 1 and 3 are shorted, and Pins 4, 5, and 6 are shorted together.
- 3,750 $V_{AC_{RMS}}$ for 1 minute duration is equivalent to 4,500 $V_{AC_{RMS}}$ for 1 second duration.

Electrical Characteristics (Apply over all recommended conditions)

($T_A = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $3.0\text{V} \leq V_{CC} \leq 5.5\text{V}$), unless otherwise specified.
 Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
INPUT CHARACTERISTICS						
V_F	Forward Voltage	$I_F = 10\text{mA}$, Fig. 1	1.05	1.45	1.8	V
BV_R	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5.0			V
I_{FHL}	Threshold Input Current	$V_O = 0.6\text{V}$, $I_{OL}(\text{sinking}) = 13\text{mA}$, $T_A < 85^{\circ}\text{C}$, Fig. 2		3.4	5.0	mA
		$T_A = 85^{\circ}\text{C}$ to 110°C		4.2	7.5	
OUTPUT CHARACTERISTICS						
V_{OL}	Logic LOW Output Voltage	$I_F = \text{rated } I_{FHL}$, $I_{OL}(\text{sinking}) = 13\text{mA}$, Fig.3		0.4	0.6	V
I_{OH}	Logic HIGH Output Current	$I_F = 250\mu\text{A}$, $V_O = 3.3\text{V}$, Fig. 4		8.0	50.0	μA
		$I_F = 250\mu\text{A}$, $V_O = 5.0\text{V}$, Fig. 4		2.1	30.0	μA
I_{CCL}	Logic LOW Output Supply Current	$I_F = 10\text{mA}$, $V_{CC} = 3.3\text{V}$, Fig. 5, 7		6.0	8.5	mA
		$I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$, Fig. 5, 7		7.5	10.0	mA
I_{CCH}	Logic HIGH Output Supply Current	$I_F = 0\text{mA}$, $V_{CC} = 3.3\text{V}$, Fig. 6, 7		4.0	7.0	mA
		$I_F = 0\text{mA}$, $V_{CC} = 5.0\text{V}$, Fig. 6, 7		6.0	9.0	mA

Switching Characteristics (Apply over all recommended conditions)

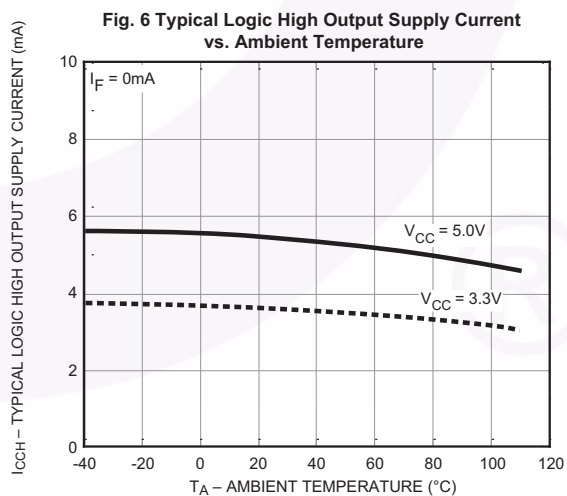
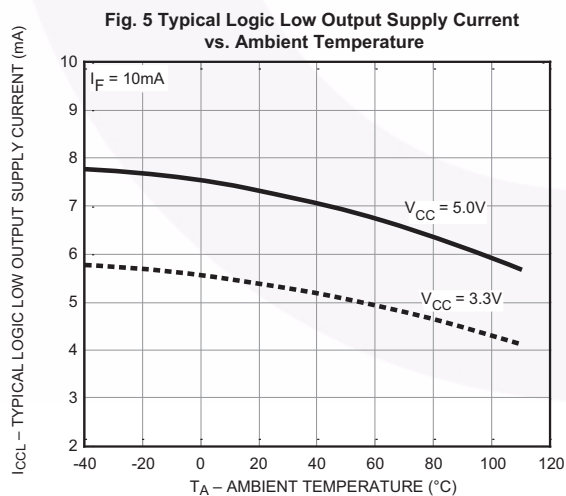
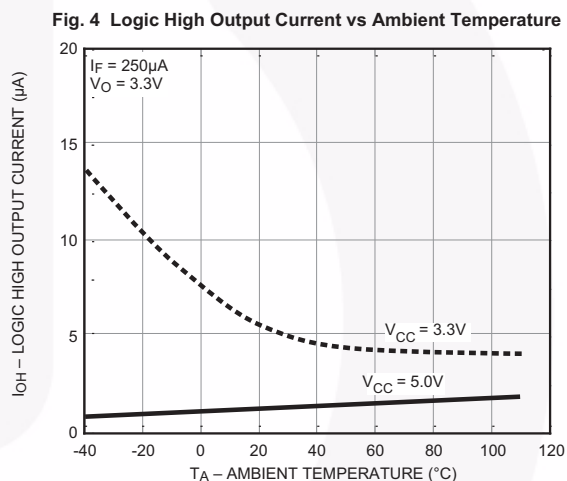
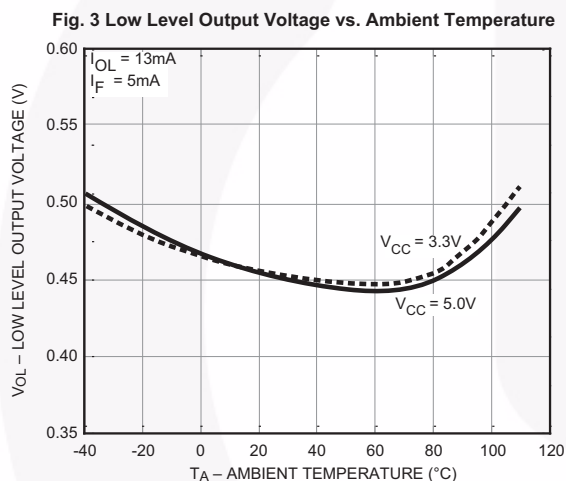
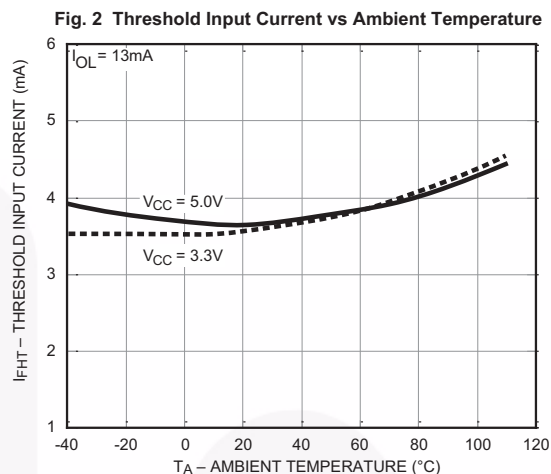
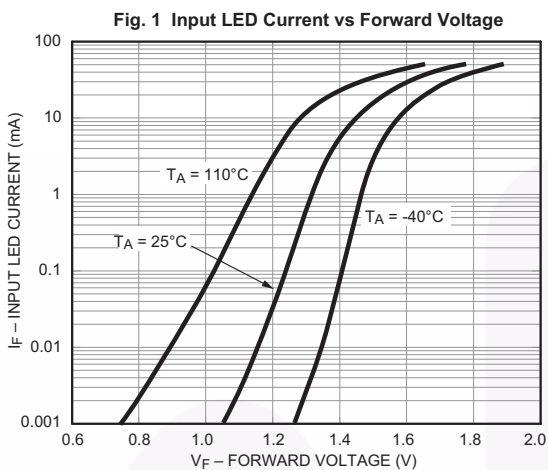
($T_A = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $3.0\text{V} \leq V_{CC} \leq 5.5\text{V}$, $I_F = 7.5\text{mA}$), unless otherwise specified.
 Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Date Rate		$R_L = 350\Omega$			10	Mbps
t_{PHL}	Propagation Delay Time to Logic Low Output	$R_L = 350\Omega$, $C_L = 15\text{pF}$, Fig. 8 and 11		43	80	ns
t_{PLH}	Propagation Delay Time to Logic High Output	$R_L = 350\Omega$, $C_L = 15\text{pF}$, Fig. 8 and 11		50	80	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$R_L = 350\Omega$, $C_L = 15\text{pF}$, Fig. 9		7	25	ns
t_{PSK}	Propagation Delay Skew	$R_L = 350\Omega$, $C_L = 15\text{pF}^{(7)}$			40	ns
t_R	Output Rise Time, (10% to 90%)	$R_L = 350\Omega$, $C_L = 15\text{pF}$, Fig. 10 and 11		20		ns
t_F	Output Fall Time, (90% to 10%)	$R_L = 350\Omega$, $C_L = 15\text{pF}$, Fig. 10 and 11		10		ns
$ CM_H $	Common Mode Transient Immunity at Output High	$I_F = 0\text{mA}$, $V_O > 0.8 \times V_{CC}$, $V_{CM} = 1000\text{V}^{(8)}$, Fig. 12	20	40		kV/ μs
$ CM_L $	Common Mode Transient Immunity at Output Low	$I_F = 7.5\text{mA}$, $V_O < 0.8\text{V}$, $V_{CM} = 1000\text{V}^{(8)}$, Fig. 12	20	40		kV/ μs

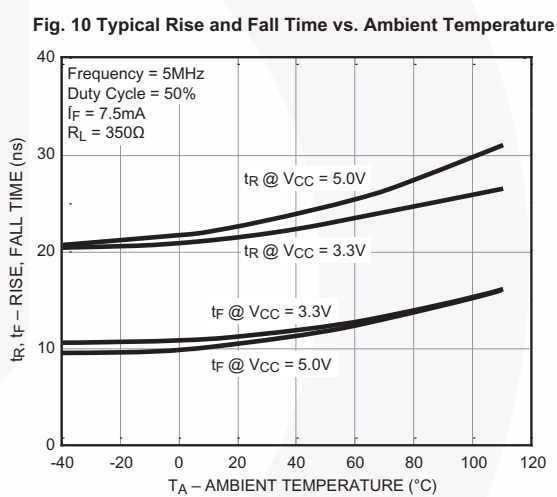
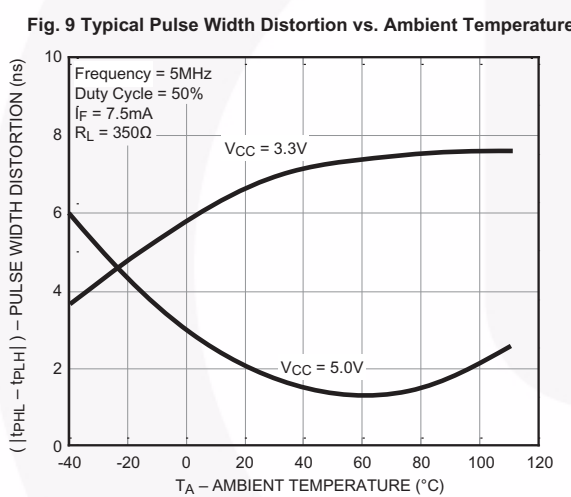
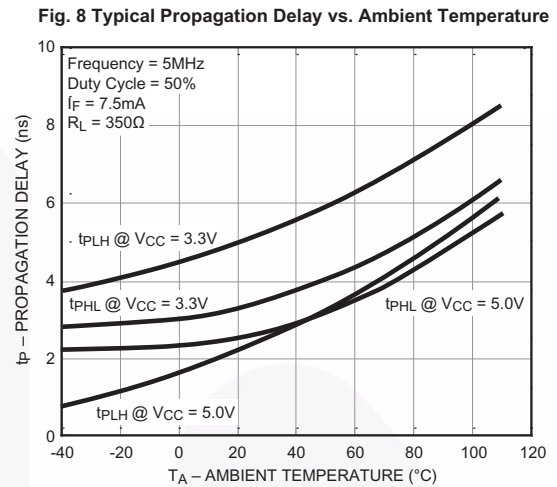
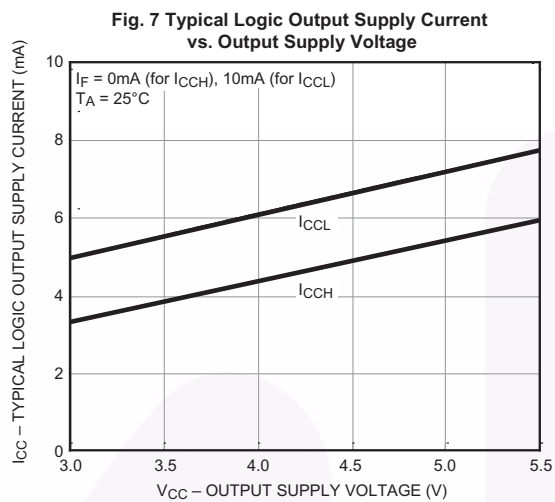
Notes

- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature ($\pm 5^{\circ}\text{C}$), at same operating conditions, with equal loads ($R_L = 350\Omega$ and $C_L = 15\text{pF}$), and with an input rise time less than 5ns.
- Common mode transient immunity at output high is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common pulse signal, V_{cm} , to assure that the output will remain low.

Typical Performance Curves



Typical Performance Curves (Continued)



Schematics

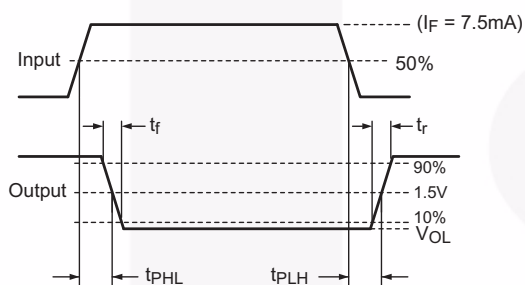
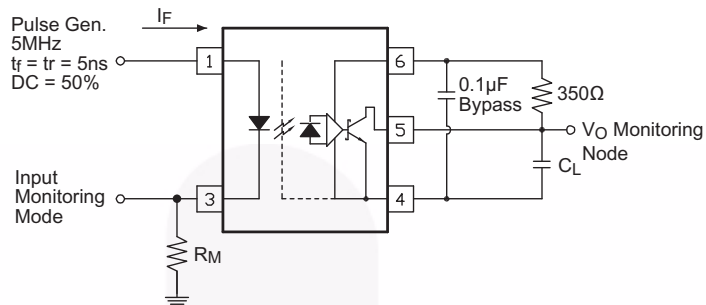


Figure 11. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

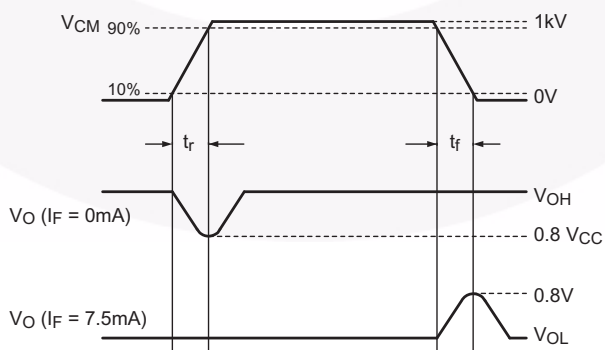
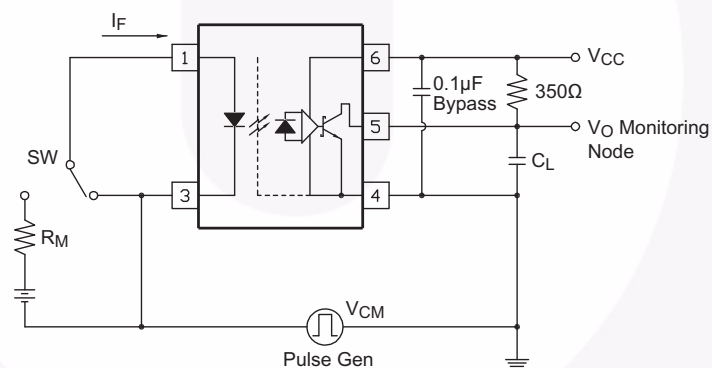
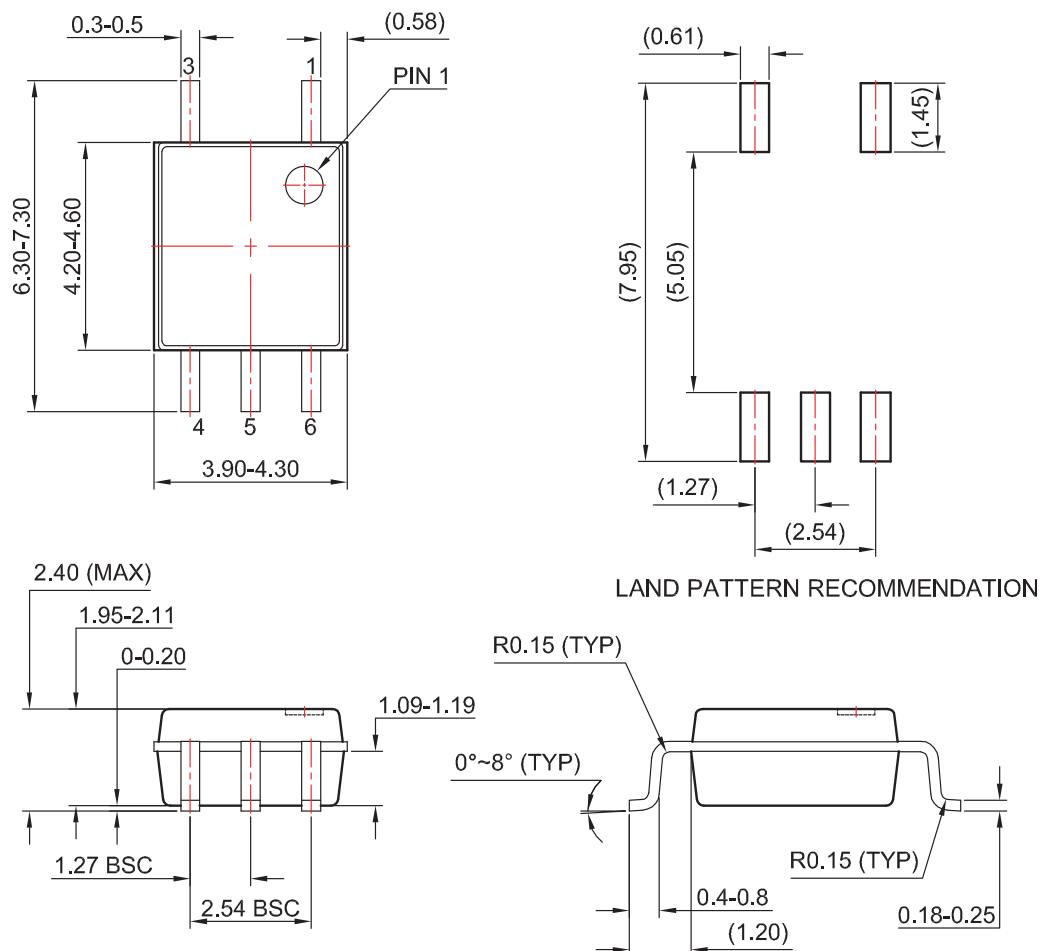


Figure 12. Test Circuit for Instantaneous Common Mode Rejection Voltage

Package Dimensions



Notes:

1. No standard applies to this package.
2. All dimensions are in millimeters.
3. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.
4. Drawings filename and revision: MKT-MFP05A.

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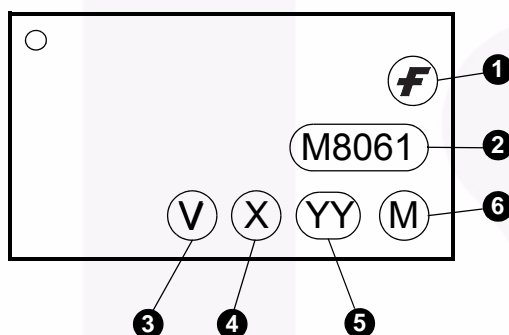
<http://www.fairchildsemi.com/packaging/>

Ordering Information

Option	Order Entry Identifier (Example)	Description
No Suffix	FODM8061	Mini-Flat 5-pin, shipped in tubes (100 units per tube)
R2	FODM8061R2	Mini-Flat 5-pin, tape and reel (2,500 units per reel)

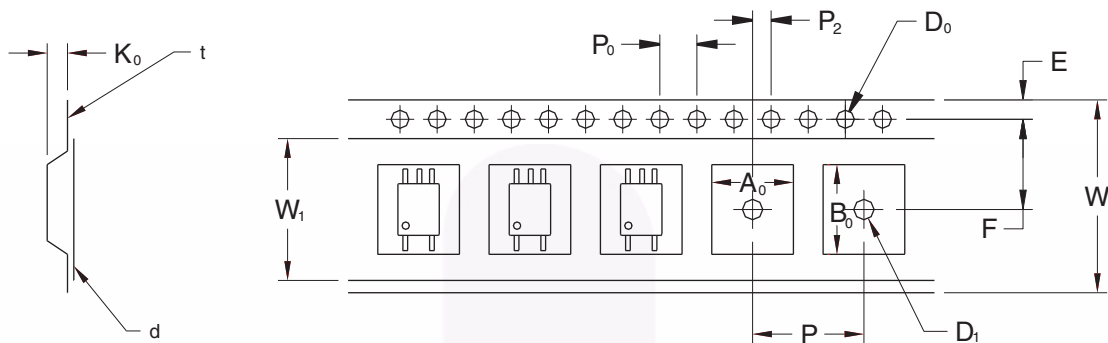
 All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information



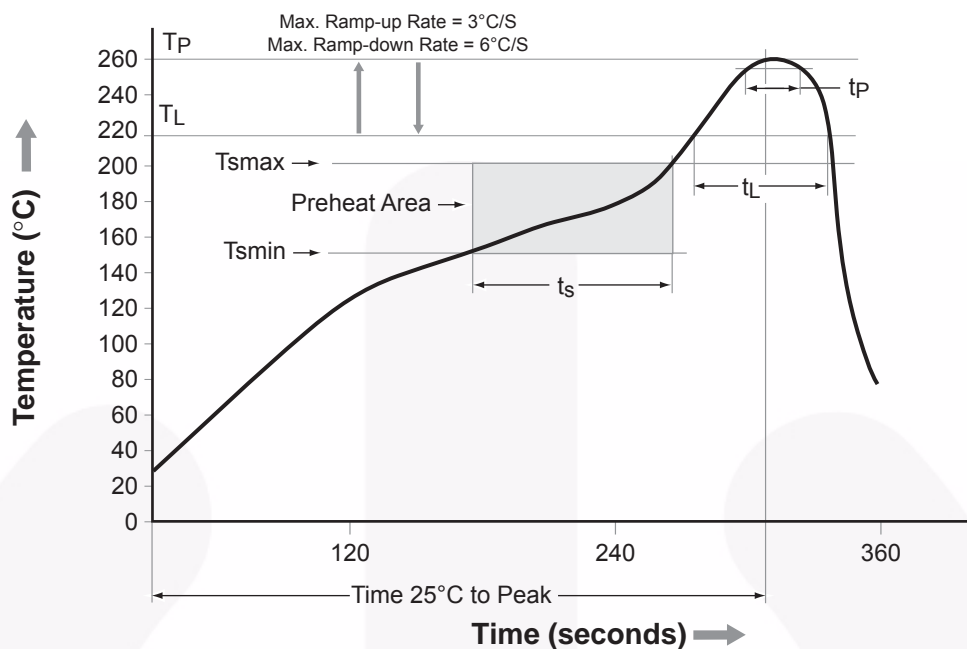
Definitions	
1	Fairchild logo
2	Device number
3	IEC60747-5-2 (VDE marking)
4	One digit year code, e.g., '9'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Tape and Reel Dimensions



		2.54 Pitch
Description	Symbol	Dimensions (mm)
Tape Width	W	12.00 +0.30/-0.10
Tape Thickness	t	0.30 ±0.05
Sprocket Hole Pitch	P ₀	4.00 ±0.10
Sprocket Hole Diameter	D ₀	1.50 +0.10/-0.0
Sprocket Hole Location	E	1.75 ±0.10
Pocket Location	F	5.50 ±0.10
	P ₂	2.00 ±0.10
Pocket Pitch	P	8.00 ±0.10
Pocket Dimension	A ₀	4.40 ±0.10
	B ₀	7.30 ±0.10
	K ₀	2.30 ±0.10
Pocket Hole Diameter	D ₁	1.50 Min.
Cover Tape Width	W ₁	9.20
Cover Tape Thickness	d	0.065 ±0.010
Max. Component Rotation or Tilt		10° Max.
Devices Per Reel		2500
Reel Diameter		330mm (13")

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60–120 seconds
Ramp-up Rate (tL to tp)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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