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November 2013

FQPF2N80

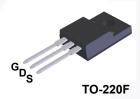
N-Channel QFET $^{\circledR}$ MOSFET 800 V, 1.5 A, 6.3 Ω

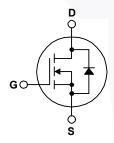
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 1.5 A, 800 V, $R_{DS(on)}$ = 6.3 Ω (Max.) @ V_{GS} = 10 V, I_D = 0.75 A
- Low Gate Charge (Typ. 12 nC)
- Low Crss (Typ. 5.5 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQPF2N80	Unit	
V_{DSS}	Drain-Source Voltage		800	V	
I _D	Drain Current - Continuous (T _C = 25°C)		1.5	А	
	- Continuous (T _C = 100°C)		0.95	А	
I _{DM}	Drain Current - Pulsed	(Note 1)	6.0	Α	
V _{GSS}	Gate-Source Voltage		± 30	V	
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	180	mJ	
I _{AR}	Avalanche Current	(Note 1)	1.5	Α	
E _{AR}	Repetitive Avalanche Energy	(Note 1)	3.5	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns	
P_D	Power Dissipation (T _C = 25°C)		35	W	
	- Derate above 25°C		0.28	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C	

Thermal Characteristics

Symbol	Parameter	FQPF2N80	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	3.57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Package Marking and Ordering Information

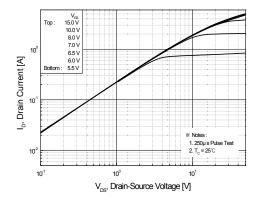
Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF2N80	FQPF2N80	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	800			V
ΔBV_{DSS} / ΔT_{J}	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.9		V/°C
I _{DSS}	Zara Oata Vallana Busin Ourset	V _{DS} = 800 V, V _{GS} = 0 V			10	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 640 V, T _C = 125°C			100	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10 V, I _D =0.75 A		4.9	6.3	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 0.75 A		2.2		S
C _{iss}	Input Capacitance Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 0 MHz		425 45	550 60	pF pF
	1 1	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz				•
C _{rss}	Reverse Transfer Capacitance			5.5	7.0	pF
	ing Characteristics				T ==	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 2.4 \text{ A},$		12	35	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		30	70	ns
t _{d(off)}	Turn-Off Delay Time	(Note 4)		25	60	ns
t _f	Turn-Off Fall Time	, ,	/	28	65	ns
Q _g	Total Gate Charge	$V_{DS} = 640 \text{ V}, I_{D} = 2.4 \text{ A},$		12 2.6	15	nC
Q _{gs}	Gate-Source Charge Gate-Drain Charge	V _{GS} = 10 V (Note 4)		6.0		nC nC
Q _{gd}	Gate-Dialii Charge	(Note 4)		0.0		IIC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
Is	Maximum Continuous Drain-Source Diode Forward Current				1.5	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current			/	6.0	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.5 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2.4 A,		480		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	/	2.0	\	μС

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 150 mH, I_{AS} = 1.5 A, V_{DD} = 50 V, R_S = 25 Ω , starting T_J = 25°C. 3. I_{SD} \leq 2.4 A, di/dt \leq 200 A/ μ s, V_{DD} \leq BV_{DSS}, starting T_J = 25°C. 4. Essentially independent of operating temperature.

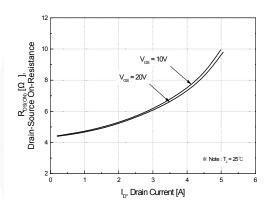
Typical Characteristics



10⁻¹ 25°C -55°C ** Notes: 1. V_{GS} = 50V 2. 250 ys Pulse Test 4 6 8 10 V_{GS}, Gate-Source Voltage [V]

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



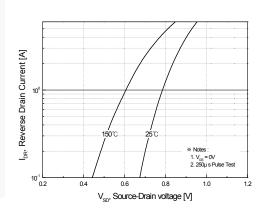
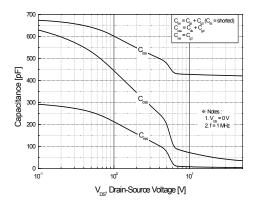


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature



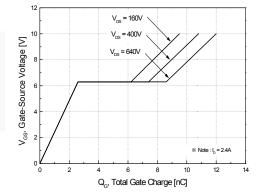
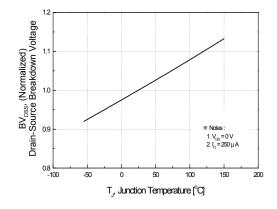


Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)



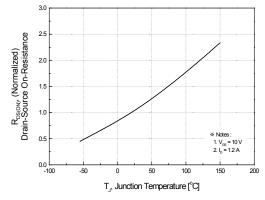
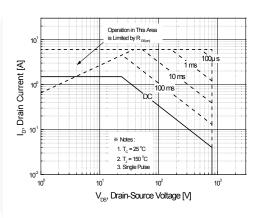


Figure 7. Breakdown Voltage Variation vs Temperature

Figure 8. On-Resistance Variation vs Temperature



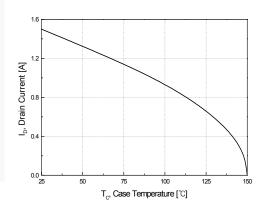


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

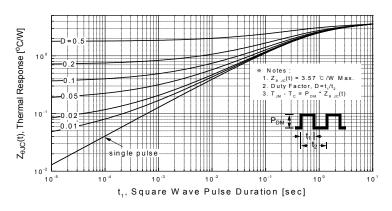


Figure 11. Transient Thermal Response Curve

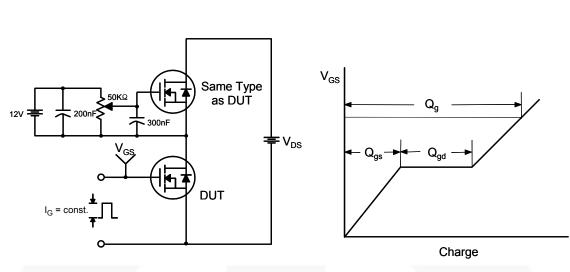


Figure 12. Gate Charge Test Circuit & Waveform

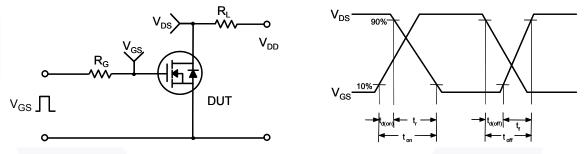


Figure 13. Resistive Switching Test Circuit & Waveforms

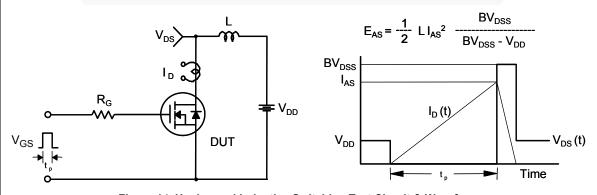
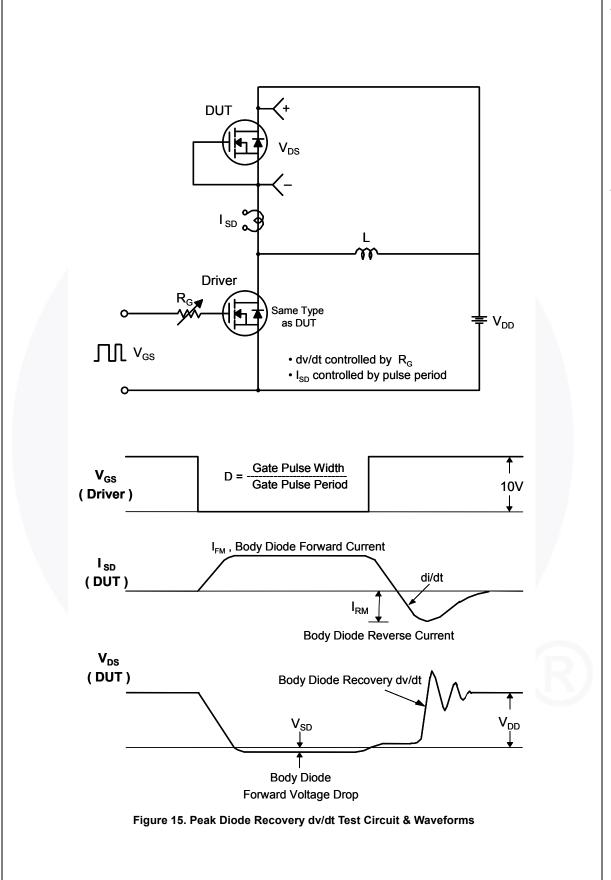


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

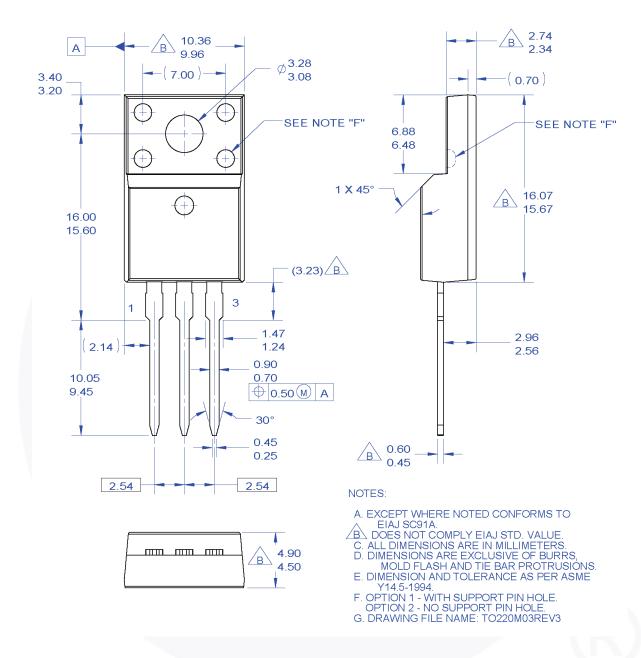


Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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