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March 2013

FSA2268 / FSA2268T Low-Voltage Dual-SPDT (0.4Ω) Analog Switch with 16kV ESD

Features

- 0.4Ω Typical On Resistance (R_{ON}) for +3.0V Supply
- 0.25Ω Maximum R_{ON} Flatness for +3.0V Supply
- -3db Bandwidth: > 50MHz
- Low I_{CCT} Current Over an Expanded Control Input Range
- Packaged in Pb-free 10-Lead µMLP (1.4 x 1.8mm)
- Power-Off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.3V
- HBM JEDEC: JESD22-A114
  - I/O to GND: 13.5kV
  - Power to GND: 16.0kV
- Noise Immunity Termination Resistors in FSA2268T

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2268 is a high-performance, dual Single Pole Double Throw (SPDT) analog switch that features ultra-low R_{ON} of 0.4Ω (typical) at 3.0V V_{CC}. The FSA2268 operates over a wide V_{CC} range of 1.65V to 4.3V and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2268 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2268T includes termination resistors that improve noise immunity during overshoot excursions, off-isolation coupling, or “pop-minimization.”

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Package Description
FSA2268UMX	GF	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm, 0.4mm Pitch
FSA2268TUMX	GH	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm, 0.4mm Pitch
FSA2268L10X	GH	10-Lead, MicroPak™, 1.6mm Wide

Analog Symbols

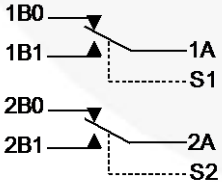


Figure 1. FSA2268

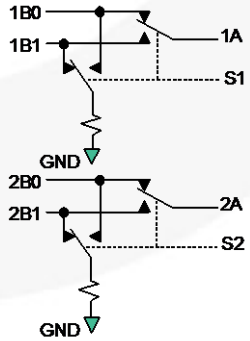


Figure 2. FSA2268T (with Noise Termination Resistors)

Pin Configuration

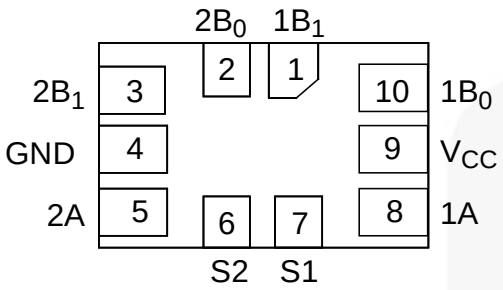


Figure 3. Pin Assignment 10-Pin UMLP (Top-Through View)

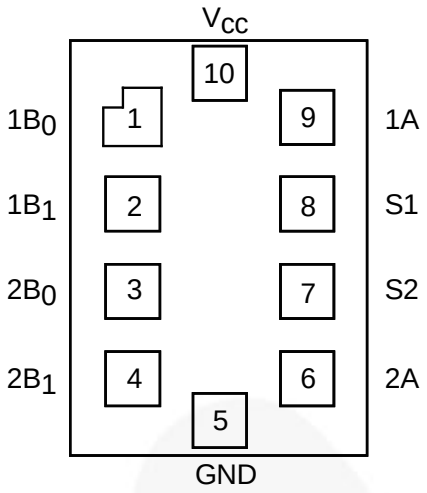


Figure 4. 10-Lead MicroPak™

Pin Descriptions

Pin # UMLP	Pin # MicroPak™	Name	Description
1	2	$1B_1$	Data Ports
2	3	$2B_0$	Data Ports
3	4	$2B_1$	Data Ports
4	5	GND	Ground
5	6	2A	Data Ports
6	7	S2	Switch Select Pins
7	8	S1	Switch Select Pins
8	9	1A	Data Ports
9	10	V_{CC}	Supply Voltage
10	1	$1B_0$	Data Ports

Truth Table

Control Input, Sn	Function
LOW Logic Level	nB0 connected to nA (FSA2268/2268T); nB1 terminated to GND (FSA2268T only)
HIGH Logic Level	nB1 connected to nA (FSA2268/2268T); nB0 terminated to GND (FSA2268T only)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{SW}	Switch I/O Voltage[1]	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	-0.5	V_{CC} + 0.3	V
		T Version nBn Pin Off	0	1.4	
V_{IN}	Control Input Voltage[1]	S1, S2	-0.5	5.5	V
I_{IK}	Input Clamp Diode Current			-50	mA
I_{SW}	Switch I/O Current (Continuous)			350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)			+260	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	Level
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND		13.5	kV
		Power to GND		16.0	
		All Other Pins		9.0	
	Charged Device Model, JEDEC: JESD22-C101			2.0	kV

Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	1.65	4.30	V
V_{IN}	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A=-40 to +85ºC		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		3.6 to 4.3				1.7		V
			2.7 to 3.6				1.5		
			2.3 to 2.7				1.4		
			1.65 to 1.95				0.9		
V_{IL}	Input Voltage Low		3.6 to 4.3					0.7	V
			2.7 to 3.6					0.5	V
			2.3 to 2.7					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage (S1,S2)	V_{IN}=0 to V_{CC}	1.65 to 4.30				-0.5	0.5	µA
$I_{NO(0FF)}$, $I_{NC(OFF)}$ FSA2268	Off Leakage Current of Port nB0 and nB1	nA=0.3V, V_{CC}–0.3V nB0 or nB1=V_{CC}-0.3V, 0.3V, or Floating Figure 6	1.95 to 4.30	-10		10	-50	50	nA
$I_{NC(OFF)}$ FSA2268T	Off Leakage Current of Port nB0 and nB1 (with Termination Resistors)	nA=0.3V, nB0 or nB1=0V or Floating Figure 6	1.95 to 4.30	-10		10	-50	50	µA
$I_{A(ON)}$	On Leakage Current of Port nA	nA=0.3V, V_{CC}–0.3V nB0 or nB1=V_{CC}-0.3V, 0.3V, or Floating Figure 7	1.95 to 4.30	-20		20	-100	100	nA
I_{OFF} FSA2268	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), V_{IN}=0V to 4.3V, V_{CC}=0V nB0, nB1=Floating	0V					±1	µA
I_{OFF} FSA2268T	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), V_{IN}=0V to 4.3V, V_{CC}=0V nB0, nB1=0V or Floating	0V					±40	µA
R_{ON}	Switch On Resistance(2)(5)	I_{ON}=100mA, nB0 or nB1=0.7V, 3.6V Figure 5	4.30		0.30			0.50	Ω
		I_{ON}=100mA, nB0 or nB1=0.7V, 2.3V Figure 5	3.00		0.40			0.55	
		I_{ON}=100mA, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V Figure 5	2.30		0.52				
		I_{ON}=100mA, nB0 or nB1=0V, 0.7V, 1.65V Figure 5	1.65		1.00				
ΔR_{ON}	On Resistance Matching Between Channels(3)(5)	I_{ON}=100mA, nB0 or nB1=0.7V	4.30		0.04			0.13	Ω
			3.00		0.06			0.13	
			2.30		0.12				
			1.65		1.00				

Continued on following page…

DC Electrical Characteristics (Continued)

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A=-40 to +85ºC		Unit
				Min.	Typ.	Max.	Min.	Max.	
$R_{FLAT(ON)}$	On Resistance Flatness[4][5]	I_{OUT}=100mA, nB0 or nB1=0V to V_{CC}	4.30					0.25	Ω
			3.00					0.25	
			2.30		0.5				
			1.65		0.6				
R_{TERM}	Internal Termination Resistors[6]				200				Ω
I_{CC}	Quiescent Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.30	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	Input at 2.6V	4.30		3			7	µA
		Input at 1.8V			7			15	

Notes:

2. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
3. $\Delta R_{ON}=R_{ON\ max} - R_{ON\ min}$ measured at identical V_{CC}, temperature, and voltage.
4. Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
5. Guaranteed by characterization, not production tested, for V_{CC}=1.65-3.00V.
6. Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are for V_{CC}=3.3V at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A=-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.6 to 4.3			55	15	60	ns	Figure 8 Figure 9
			2.7 to 3.6			60	15	65		
			2.3 to 2.7			65	15	70		
			1.65 to 1.95		70					
t_{OFF}	Turn-Off Time	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.6 to 4.3			30	5	35	ns	
			2.7 to 3.6			35	5	40		
			2.3 to 2.7			40	5	45		
			1.65 to 1.95		40					
t_{BBM}	Break-Before-Make Time	nB0 or nB1=1.5V, R_L=50Ω, C_L=35pF	3.6 to 4.3		15		2		ns	Figure 10
			2.7 to 3.6		15		2			
			2.3 to 2.7		15		2			
			1.65 to 1.95		16		2			
Q	Charge Injection	C_L=1.0nF, V_S=0V, R_S=0Ω	1.65 to 4.30		25				pC	Figure 14
OIRR	Off Isolation	f=100kHz, R_L=50Ω, C_L=0pF	1.65 to 4.30		-70				dB	Figure 12
Xtalk	Crosstalk	f=100kHz, R_L=50Ω, C_L=0pF	1.65 to 4.30		-70				dB	Figure 13
BW	-3db Bandwidth	R_L=50Ω, C_L=0pF	1.65 to 4.30		>50				MHz	Figure 11
THD	Total Harmonic Distortion	f=20Hz to 20kHz, R_L=32Ω, V_{IN}=2V_{pp}	1.65 to 4.30		.06				%	Figure 17

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	f=1MHz	0		1.5		pF	Figure 15
C_{OFF}	B Port Off Capacitance	f=1MHz	3.3		30		pF	Figure 15
C_{ON}	A Port On Capacitance	f=1MHz	3.3		120		pF	Figure 16

Test Diagrams

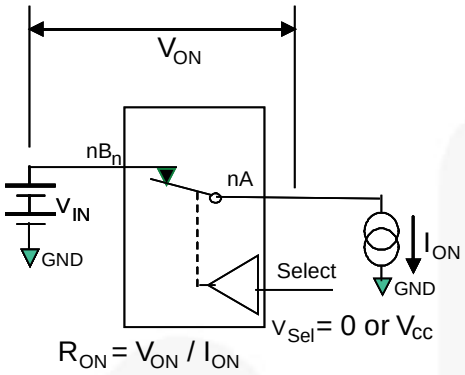
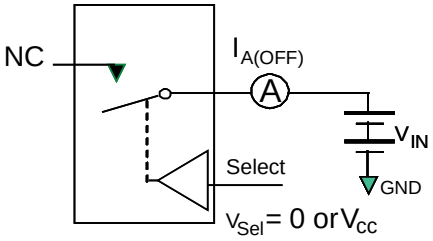


Figure 5. On Resistance



**Each switch port is tested separately.

Figure 6. Off Leakage (Ports tested separately)

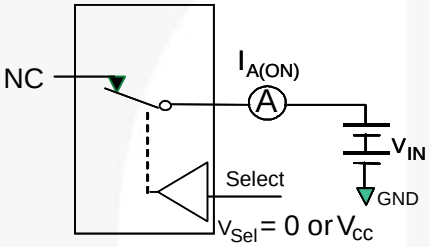


Figure 7. On Leakage

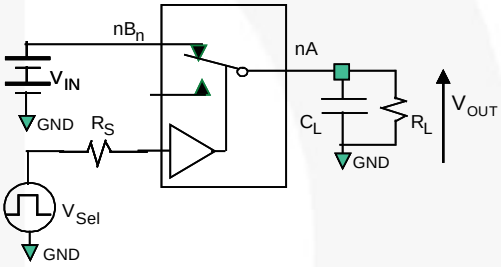


Figure 8. Test Circuit Load

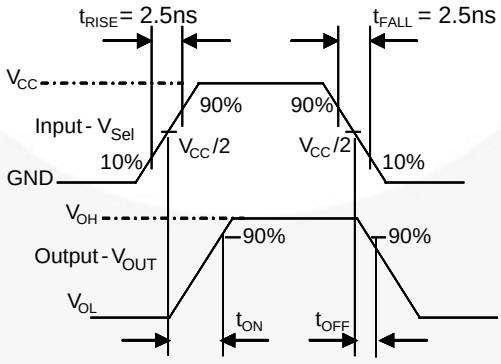
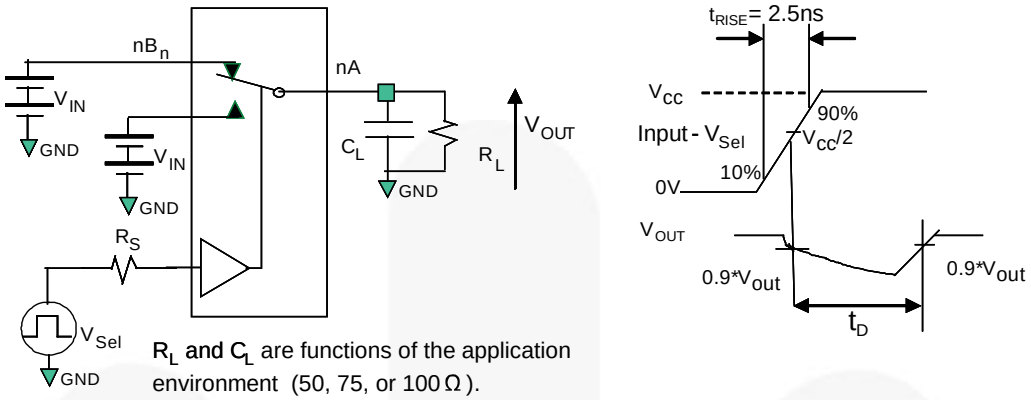


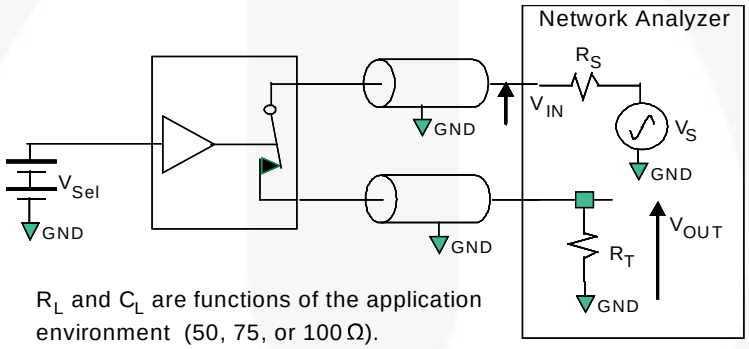
Figure 9. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)



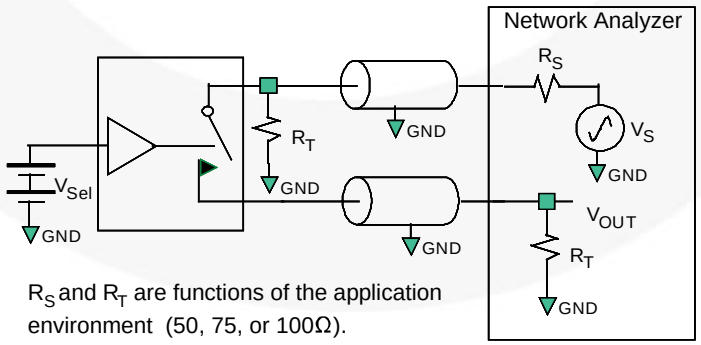
R_L and C_L are functions of the application environment (50, 75, or 100 Ω).
C_L includes test fixture and stray capacitance.

Figure 10. Break-Before-Make Interval Timing



R_L and C_L are functions of the application environment (50, 75, or 100 Ω).
C_L includes test fixture and stray capacitance.

Figure 11. Bandwidth

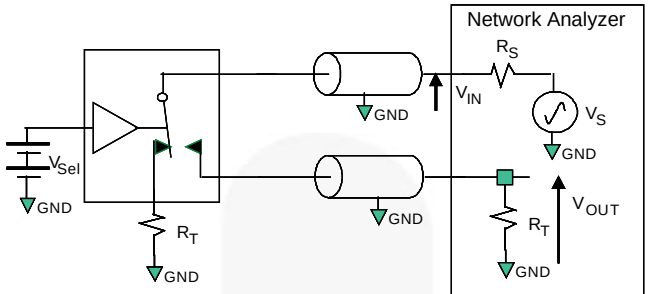


R_S and R_T are functions of the application environment (50, 75, or 100Ω).

Off-Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 12. Channel Off Isolation

Test Diagrams (Continued)



R_S and R_T are functions of the application environment (50, 75, or 100Ω).

CROSSTALK = 20 Log (V_{OUT}/ V_{IN})

Figure 13. Adjacent Channel Crosstalk

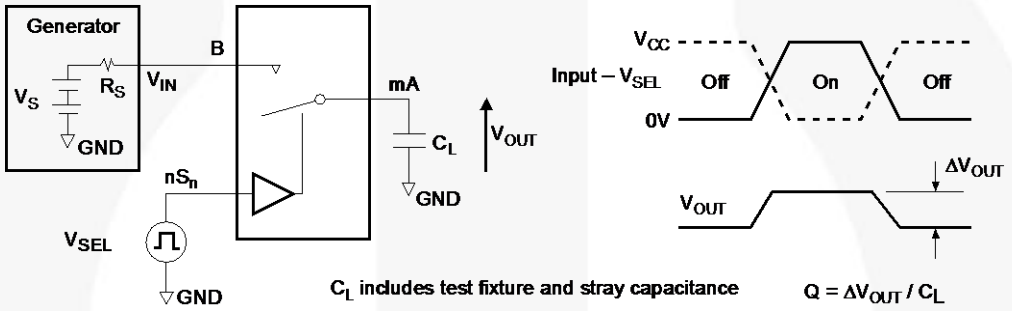


Figure 14. Charge Injection Test

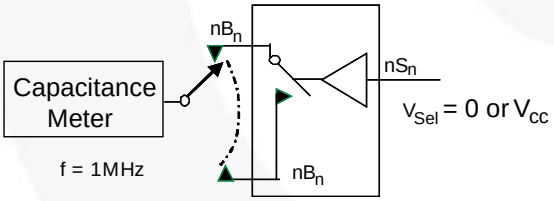


Figure 15. Channel Off Capacitance

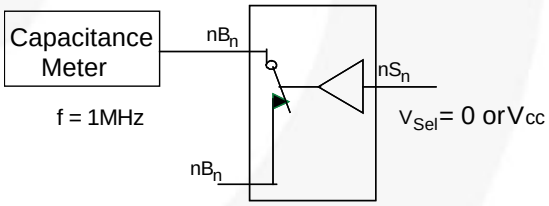
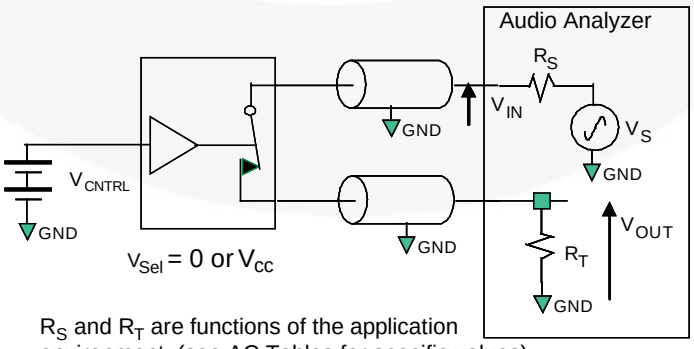


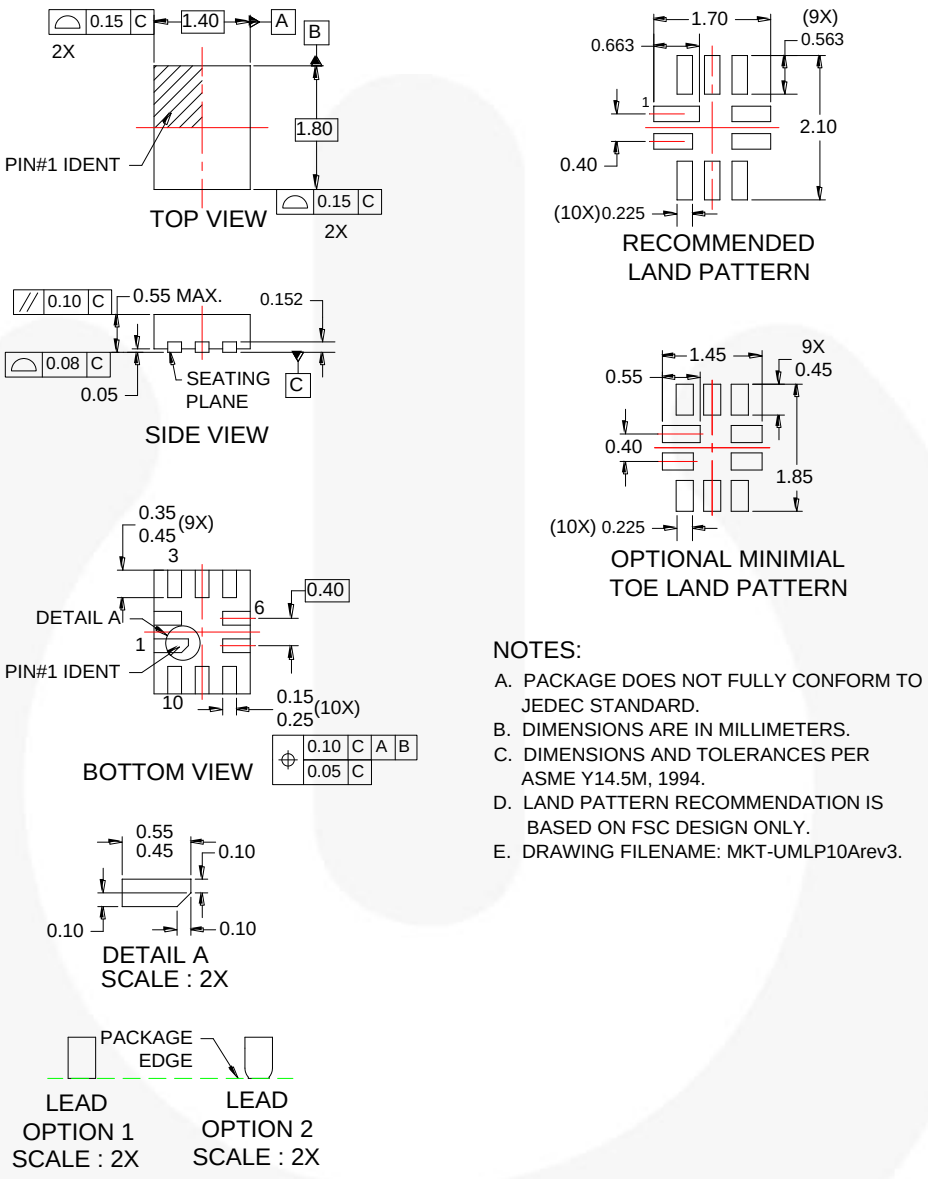
Figure 16. Channel On Capacitance



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 17. Total Harmonic Distortion

Physical Dimensions



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP10Arev3.

Figure 18. 10-Lead Quad Ultrathin Molded Leadless Package (UMLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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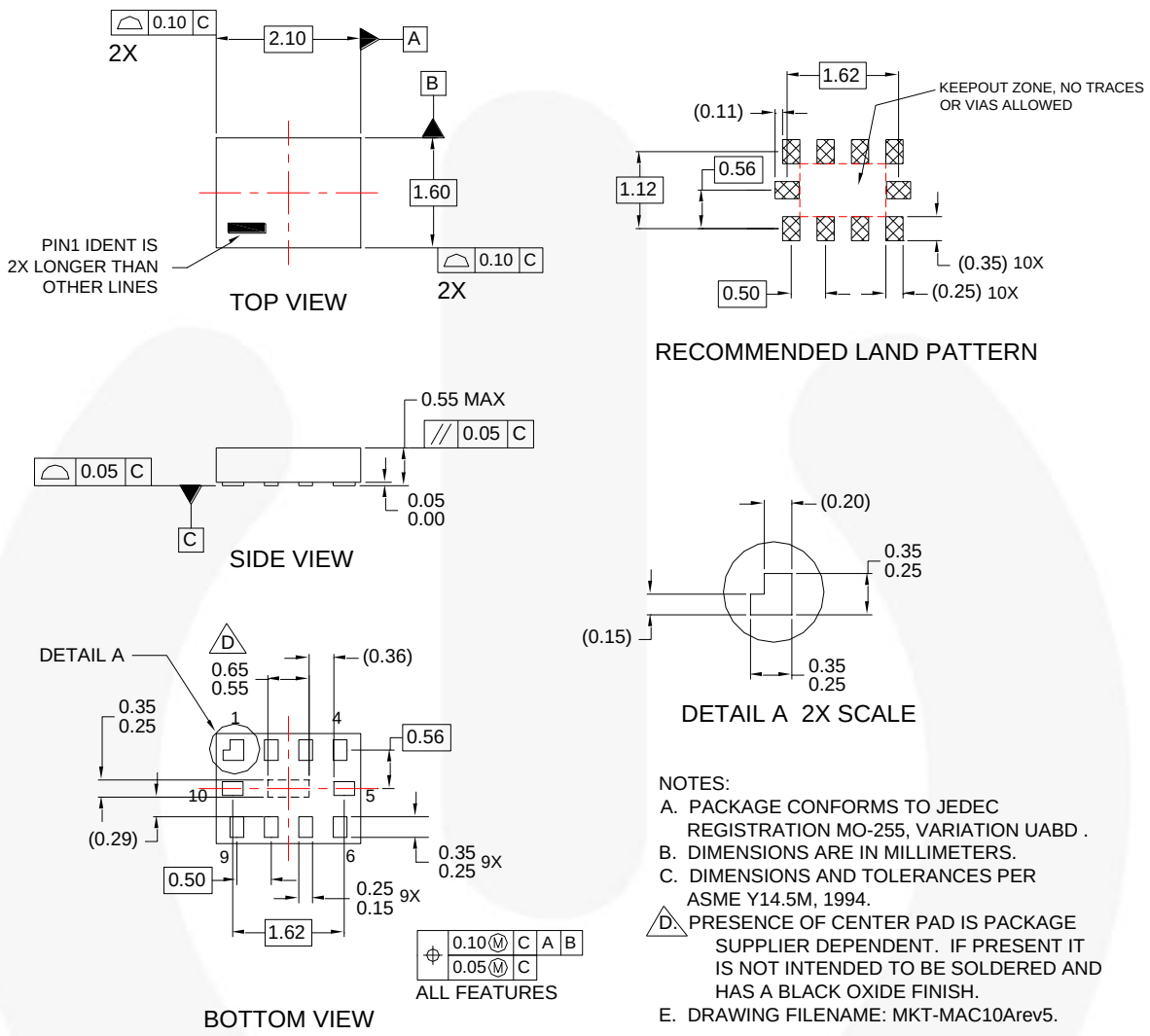
For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:
http://www.fairchildsemi.com/products/analog/pdf/UMLP10_TNR.pdf.

Physical Dimensions (Continued)



NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD .

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev5.

Figure 19. 10-Lead, MicroPak™, 1.6mm Wide

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http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

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CROSSVOLT™
CTL™
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Dual Cool™
EcoSPARK®
EfficientMax™
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FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
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SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
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