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FSA2457 — Dual DPDT, 5Ω Analog Data Switch

Features

- Low On Capacitance for Data Path: 12pF Typical
- Low On Resistance for Data Path: 5Ω Typical
- Low Power Quiescent Consumption: 1μA Maximum
- Wide -3db Bandwidth: > 160MHz
- Packaged in Green 16-Lead UMLP (1.8 x 2.6mm)
- 4kV JEDEC: JESD22-A114 HBM
- 2kV JEDEC: JESD22-C101 CDM

Applications

- Cell Phone, PDA, Digital Camera, Portable GPS
- LCD Monitor, TV, Set-Top Box

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.


Description

The FSA2457 is a bi-directional, low-power, dual double-pole double-throw (4PDT) analog switch targeted at dual 1-bit SIM/SD/MMC card and/or GPS signal multiplexing. It is optimized for switching the WLAN-SIM data and control signals at 52Mbps.

The FSA2457 is compatible with the requirements of 1-bit SIM/SD/MMC cards and is ideal for interfacing to GPS baseband processors. The FSA2457 features a low on capacitance (C_{ON}) of 12pF to ensure high-speed data transfer.

The FSA2457 contains special circuitry that minimizes current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and portable GPS systems.

Ordering Information

| Part Number | Top Mark |  Eco Status | Operating Temperature Range | Package |
|-------------|----------|--|-----------------------------|--|
| FSA2457UMX | GD | Green | -40 to +85°C | 16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6mm |

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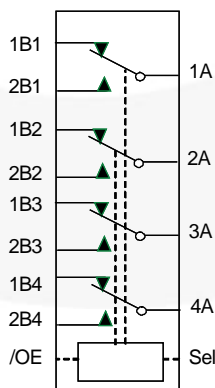


Figure 1. Analog Symbol

Pin Configuration

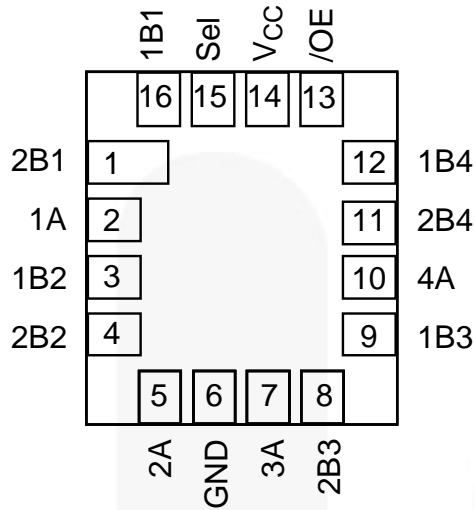


Figure 2. Pad Assignment UMLP16 (Top Through View)

Pin Definitions

| Pin | Description |
|----------|--------------------------------|
| 1Bn, 2Bn | Multiplexed Data Source Inputs |
| nA | Common Data Ports |
| Sel | Switch Select |
| /OE | Output Enable (Active LOW) |

Truth Table

| Sel | /OE | Function |
|------------|------------|--|
| Logic LOW | Logic LOW | 1B1 = 1A, 1B2 = 2A, 1B3 = 3A, 1B4 = 4A |
| Logic HIGH | Logic LOW | 2B1 = 1A, 2B2 = 2A, 2B3 = 3A, 2B4 = 4A |
| X | Logic HIGH | Data Ports Disconnected |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------|--|------------|----------------|-------|
| V_{CC} | Supply Voltage | -0.5 | +4.6 | V |
| V_{CNTRL} | DC Input Voltage (Sel, /OE) ⁽¹⁾ | -0.5 | +4.6 | V |
| V_{SW} | DC Switch I/O Voltage ⁽¹⁾ 1Bn, 2Bn, nA | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | -50 | | mA |
| I_{OUT} | DC Output Current – V_{SW} | | 128 | mA |
| T_{STG} | Storage Temperature | -65 | +150 | °C |
| MSL | Moisture Sensitivity Level (JEDEC J-STD-020A) | | 1 | Level |
| ESD | Human Body Model, JEDEC: JESD22-A114 | All Pins | 4 | kV |
| | | I/O to GND | 8 | |
| | Charged Device Model, JEDEC: JESD22-C101 | 2 | | |

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------|---|------|----------|------|
| V_{CC} | Supply Voltage | 2.7 | 3.6 | V |
| V_{CNTRL} | Control Input Voltage (Sel, /OE) ⁽²⁾ | 0 | V_{CC} | V |
| V_{SW} | Switch I/O Voltage 1Bn, 2Bn, nA | -0.5 | V_{CC} | V |
| I_{OUT} | DC Output Current 1Bn, 2Bn, nA | | 25 | mA |
| T_A | Operating Temperature | -40 | 85 | °C |

Note:

- The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C, 3.3V V_{CC} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ | | | Units |
|---------------------------------|---|---|--------------|---|------|------|---------------|
| | | | | Min. | Typ. | Max. | |
| V_{IK} | Clamp Diode Voltage | $I_{IN} = -18\text{mA}$ | 2.7 | | | -1.2 | V |
| V_{IH} | Input Voltage High | | 2.7 to 3.0 | 1.8 | | | V |
| | | | 3.3 to 3.6 | 2.0 | | | |
| V_{IL} | Input Voltage Low | | 2.7 to 3.6 | | | 0.8 | V |
| I_{IN} | Control Input Leakage (Sel) | $V_{SW} = 0$ to V_{CC} | 3.6 | -1 | | 1 | μA |
| $I_{nc(off)},$ $I_{no(off)}$ | Off State Leakage | 1Bn, 2Bn = 0V or V_{CC} Figure 4 | 3.6 | -1 | | 1 | μA |
| R_{ON} | Data Path Switch On Resistance ⁽³⁾ | $V_{SW} = 0, 2.0\text{V}, I_{ON} = -20\text{mA}$ Figure 3, Figure 12 | 2.7 | | 5.0 | 7.0 | Ω |
| ΔR_{ON} | Data Path Delta On Resistance ⁽⁴⁾ | $V_{SW} = 0\text{V}, I_{ON} = -20\text{mA}$ | 2.7 | | 0.3 | | Ω |
| I_{CC} | Quiescent Supply Current | $V_{CNTRL} = 0$ or $V_{CC}, I_{OUT} = 0$ | 3.6 | | | 1.0 | μA |

Notes:

- Measured by the voltage drop between nB0, 1Bn and relative common port pins at the indicated current through the switch. On resistance is determined by the lower voltage on the relative ports.
- Guaranteed by characterization.

AC Electrical Characteristics

All typical value are for $V_{CC} = 3.3V$ at $25^{\circ}C$ unless otherwise specified.

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | | Units |
|-----------|--|--|--------------|--|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| t_{ON} | Turn-On Time Sel or /OE to Output (nA) | $R_L = 50\Omega$, $C_L = 30pF$ $V_{SW} = 1.5V$ Figure 5, Figure 6 | 2.7 to 3.6 | | | 7.0 | ns |
| t_{OFF} | Turn-Off Time Sel or /OE to Output (nA) | $R_L = 50\Omega$, $C_L = 30pF$ $V_{SW} = 1.5V$ Figure 5, Figure 6 | 2.7 to 3.6 | | | 4.0 | ns |
| O_{IRR} | Off Isolation ⁽⁵⁾ (nA) | $R_L = 50\Omega$, $f = 25MHz$, $C_L = 30pF$ Figure 9, Figure 13 | 2.7 to 3.6 | | -45 | | dB |
| Xtalk | Non-Adjacent Channel Crosstalk ⁽⁵⁾ (nA) | $R_L = 50\Omega$, $f = 25MHz$, $C_L = 30pF$ Figure 7 | 2.7 to 3.6 | | -54 | | dB |
| BW | -3db Bandwidth ⁽⁵⁾ (nA) | $R_L = 50\Omega$, $C_L = 30pF$ Figure 8, Figure 14 | 2.7 to 3.6 | | >160 | | MHz |

Note:

5. Guaranteed by characterization.

Capacitance

| Symbol | Parameter | Conditions | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | | Units |
|-----------|--|---|--|------|------|-------|
| | | | Min. | Typ. | Max. | |
| C_{IN} | Control Pin Input Capacitance | $V_{CC} = 0V$ | | 1.8 | | pF |
| C_{ON} | On Capacitance ⁽⁶⁾ (nA) | $V_{CC} = 3.3V$, $f = 1MHz$ Figure 10 | | 12.0 | | pF |
| C_{OFF} | Off Capacitance ⁽⁶⁾ (nA) | $V_{CC} = 3.3V$ Figure 9 | | 6.0 | | pF |

Note:

6. Guaranteed by characterization.

Test Diagrams

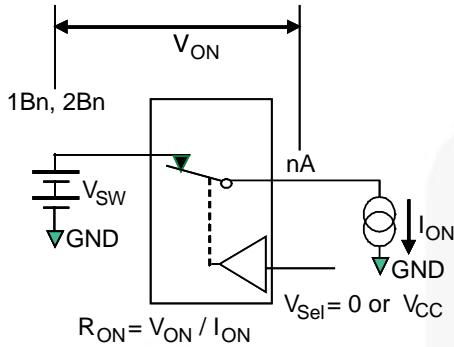


Figure 3. On Resistance

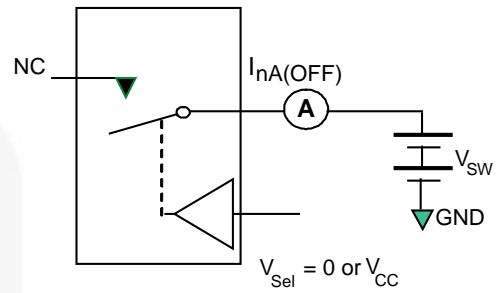
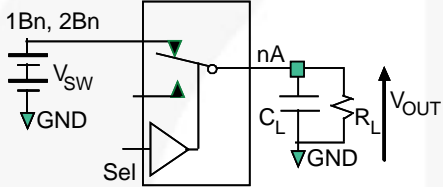


Figure 4. Off Leakage



R_L and C_L are functions of the application environment (see tables for specific values). C_L includes test fixture and stray capacitance.

Figure 5. AC Test Circuit Load

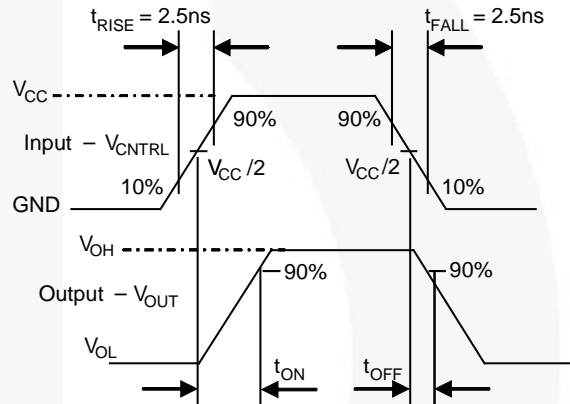
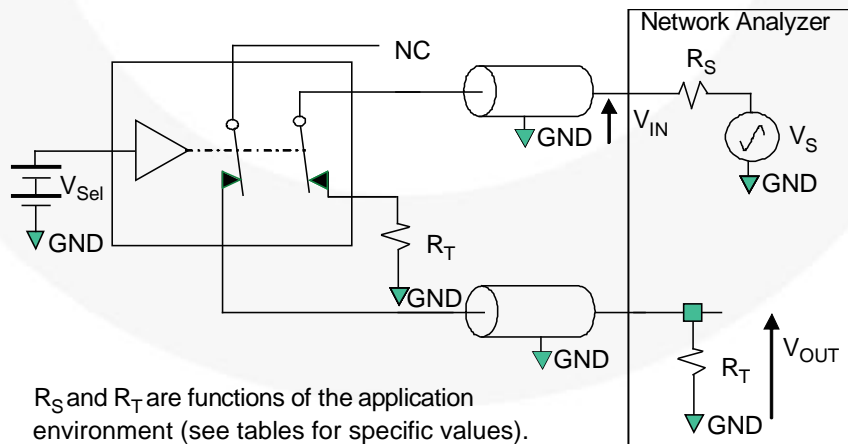


Figure 6. Turn-On / Turn-Off Waveforms



R_S and R_T are functions of the application environment (see tables for specific values).

$$\text{Crosstalk} = 20 \text{ Log } (V_{\text{OUT}} / V_{\text{IN}})$$

Figure 7. Non-Adjacent Channel-to-Channel Crosstalk

Test Diagrams (Continued)

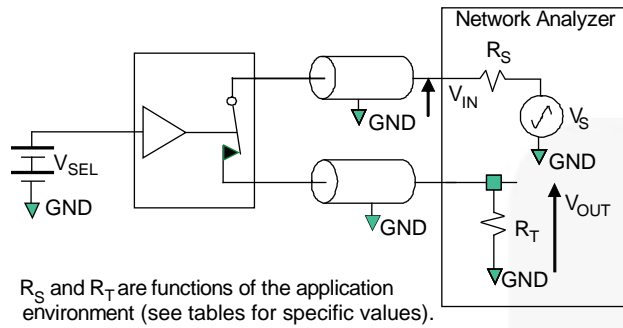


Figure 8. Bandwidth

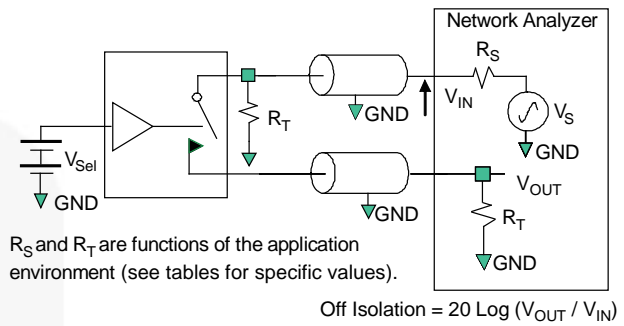


Figure 9. Channel Off Isolation

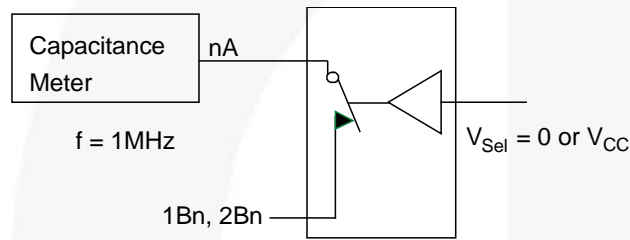


Figure 10. Channel On Capacitance

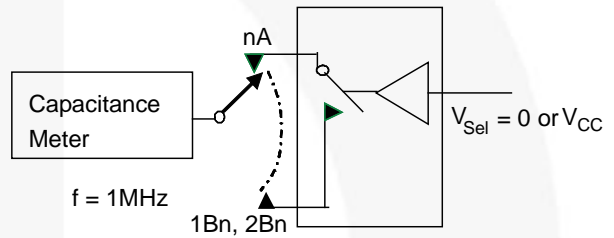


Figure 11. Channel Off Capacitance

Typical Performance Characteristics

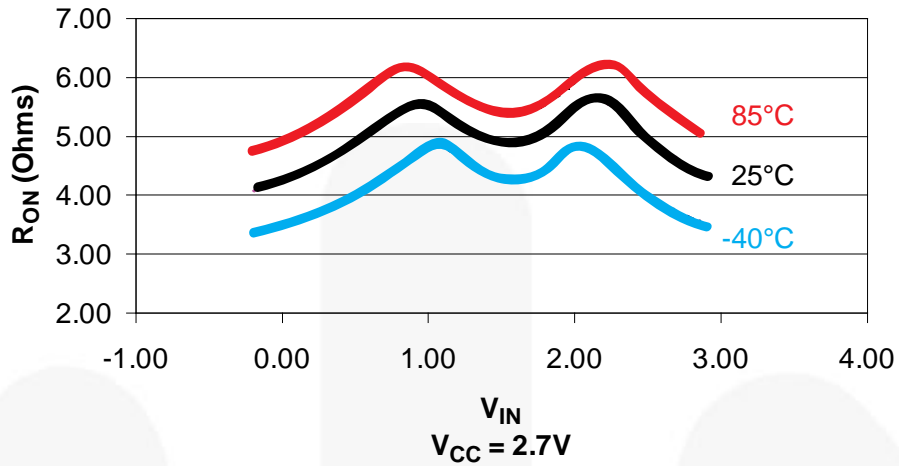


Figure 12. R_{ON}

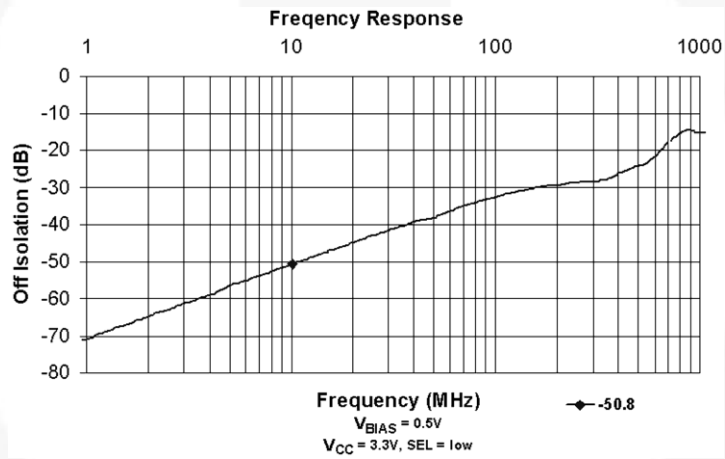


Figure 13. Off Isolation

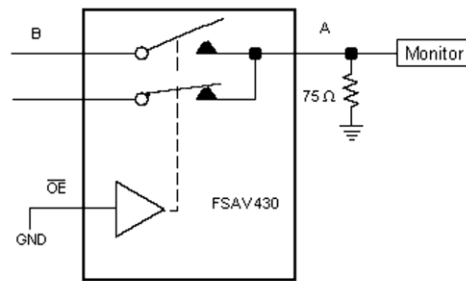
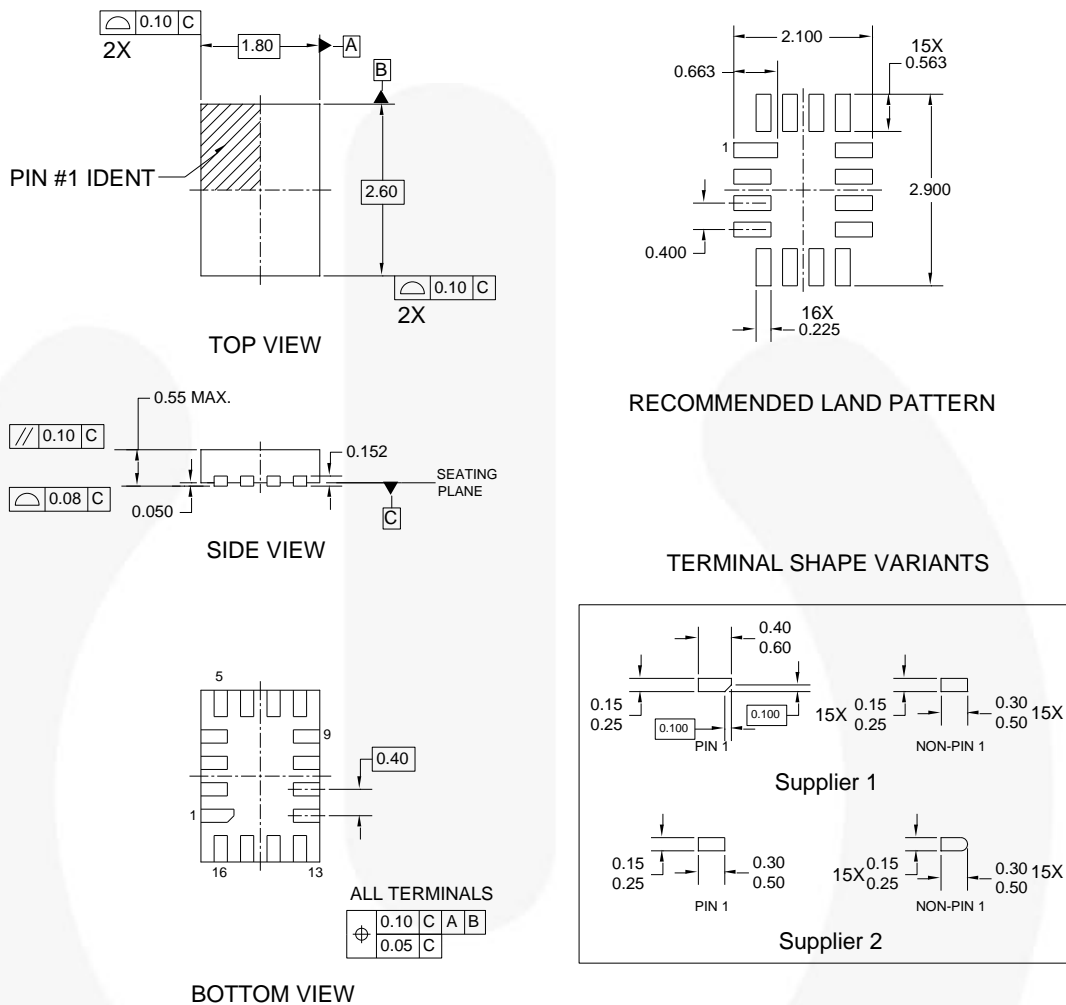


Figure 14. Bandwidth

Physical Dimensions



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- F. DRAWING FILE NAME : UMLP16AREV3

Figure 15. 16-Lead Ultrathin Molded Leadless Package (UMLP)







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