One Megabit per Second Triple Digital Isolators

Check for Samples: ISO7230A, ISO7231A

FEATURES

- 1Mbps Signaling Rate
  - Low Channel-to-Channel Output Skew; 2ns Maximum (5V-Operation)
  - Low Pulse-Width Distortion (PWD); 10ns Maximum (5V-Operation)
- Typical 25-Year Life at Rated Working Voltage (See Application note SLLA197 and Figure 10)
- 4000V_{peak} Isolation, 560V_{peak} V_{IORM}
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IE 61010-1 and CSA Approved, IEC 60950-1
- 4kV ESD Protection
- Operate With 3.3V or 5V Supplies
- High Electromagnetic Immunity (See Application note SLLA181)
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

See the Product Notification section. The ISO7230A and ISO7231A are triple-channel digital isolators each with multiple channel configurations and output-enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

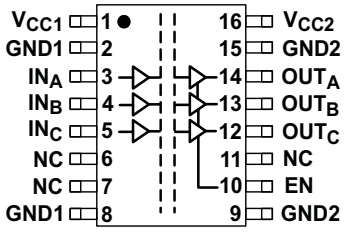
The ISO7230 triple-channel device has all three channels in the same direction while the ISO7231 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state.

The ISO7230A and ISO7231A have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2ns in duration from being passed to the output of the device.

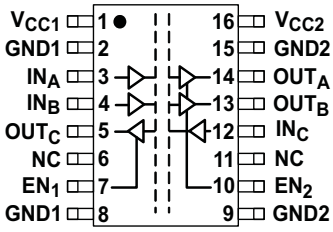
In each device a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3V, 5V, or any combination. All inputs are 5V tolerant when supplied from a 3.3V supply and all outputs are 4mA CMOS. These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

ISO7230
DW PACKAGE



ISO7231
DW PACKAGE



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTION DIAGRAM

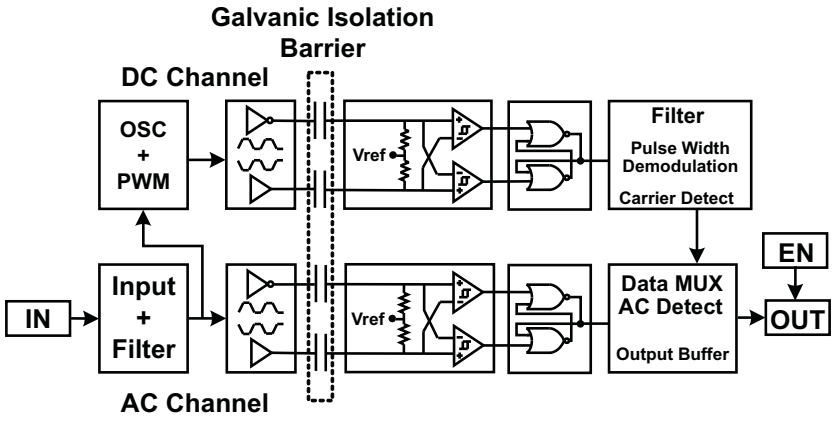


Table 1. Device Function Table ISO723x (1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER(1)
ISO7230ADW	1 Mbps	~1.5V (TTL) (CMOS compatible)	3/0	ISO7230A	ISO7230ADW (rail)
					ISO7230ADWR (reel)
ISO7231ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	2/1	ISO7231A	ISO7231ADW (rail)
					ISO7231ADWR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT, EN				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	3.15		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
t_{ui}	Input pulse width	1			µs
$1/t_{ui}$	Signaling rate	0	1500(2)	1000	kbps
V_{IH}	High-level input voltage (IN) (EN on all devices)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)	0		0.8	
T_J	Junction temperature			150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) For the 5V operation, V_{CC1} or V_{CC2} is specified from 4.5V to 5.5V.
For the 3V operation, V_{CC1} or V_{CC2} is specified from 3.15V to 3.6V.
(2) Typical signaling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V		1	3	mA
		1 Mbps			1	3	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V		6.5	11	mA
		1 Mbps			6.5	11	
I_{CC2}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V		15	22	mA
		1 Mbps			16	22	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V		13	20	mA
		1 Mbps			13	20	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0V, Single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4mA, See Figure 1			0.4	V
			I_{OL} = 20µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0V, See Figure 4	25	50		kV/µs

(1) For the 5V operation, V_{CC1} or V_{CC2} is specified from 4.5V to 5.5V.
For the 3V operation, V_{CC1} or V_{CC2} is specified from 3.15V to 3.6V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	40		95	ns
PWD	Pulse-width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$				10	
$t_{sk(o)}$	Channel-to-channel output skew [2]			0	2	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5V, V_{CC2} at 3.3V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V			1	3	mA
		1 Mbps				1	3	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V			6.5	11	mA
		1 Mbps				6.5	11	
I_{CC2}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V			9	15	mA
		1 Mbps				9.5	15	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V			8	12	mA
		1 Mbps				8	12	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4mA, See Figure 1	ISO7230	V_{CC} – 0.4			V
				ISO7231 (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4mA, See Figure 1				0.4	V
			I_{OL} = 20µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5V to 5.5V.
For the 3V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5V, V_{CC2} at 3.3V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xA	See Figure 1	40		100	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$					11	
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA			0	2.5	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		18		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3V, V_{CC2} at 5V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V			0.5	1	mA
		1 Mbps				1	2	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V			4.5	7	mA
		1 Mbps				4.5	7	
I_{CC2}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_2 at 3V			15	22	mA
		1 Mbps				16	22	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, All channels, no load, EN_1 at 3V, EN_2 at 3V			13	20	mA
		1 Mbps				13	20	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4mA, See Figure 1	ISO7230	V_{CC} – 0.4			V
				ISO7231 (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4mA, See Figure 1				0.4	V
			I_{OL} = 20µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0V, See Figure 4		25	50		kV/µs

(1) For 5V operation, V_{CC1} or V_{CC2} is specified from 4.5V to 5.5V.
For 3V operation, V_{CC1} or V_{CC2} is specified from 3.15V to 3.6V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3V and V_{CC2} at 5V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xA	See Figure 1	40		100	ns
PWD	Pulse-width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$					11	
$t_{sk(o)}$	Channel-to-channel output skew [2]	ISO723xA			0	2.5	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		12		µs

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230A	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3V		0.5	1	mA
		1 Mbps			1	2	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, all channels, no load, EN_1 at 3V, EN_2 at 3V		4.5	7	mA
		1 Mbps			4.5	7	
I_{CC2}	ISO7230A	Quiescent	V_I = V_{CC} or 0V, all channels, no load, EN_2 at 3V		9	15	mA
		1 Mbps			9.5	15	
	ISO7231A	Quiescent	V_I = V_{CC} or 0V, all channels, no load, EN_1 at 3V, EN_2 at 3V		8	12	mA
		1 Mbps			8	12	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4mA, See Figure 1			0.4	V
			I_{OL} = 20µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0V, See Figure 4	25	50		kV/µs

(1) For 5V operation, V_{CC1} or V_{CC2} is specified from 4.5V to 5.5V.
For 3V operation, V_{CC1} or V_{CC2} is specified from 3.15V to 3.6V.

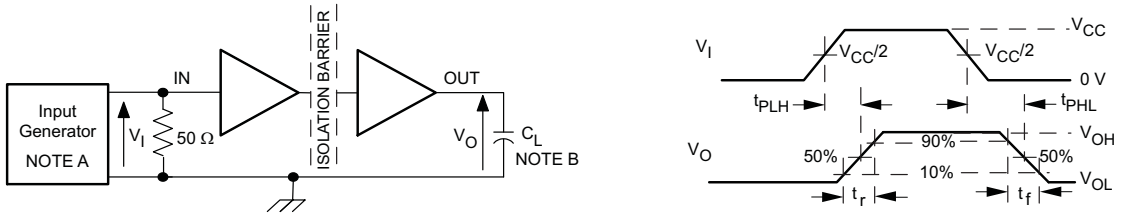
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xA	See Figure 1	45		110	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$					12	
$t_{sk(o)}$	Channel-to-channel output skew (2)	ISO723xA			0	3	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		18		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

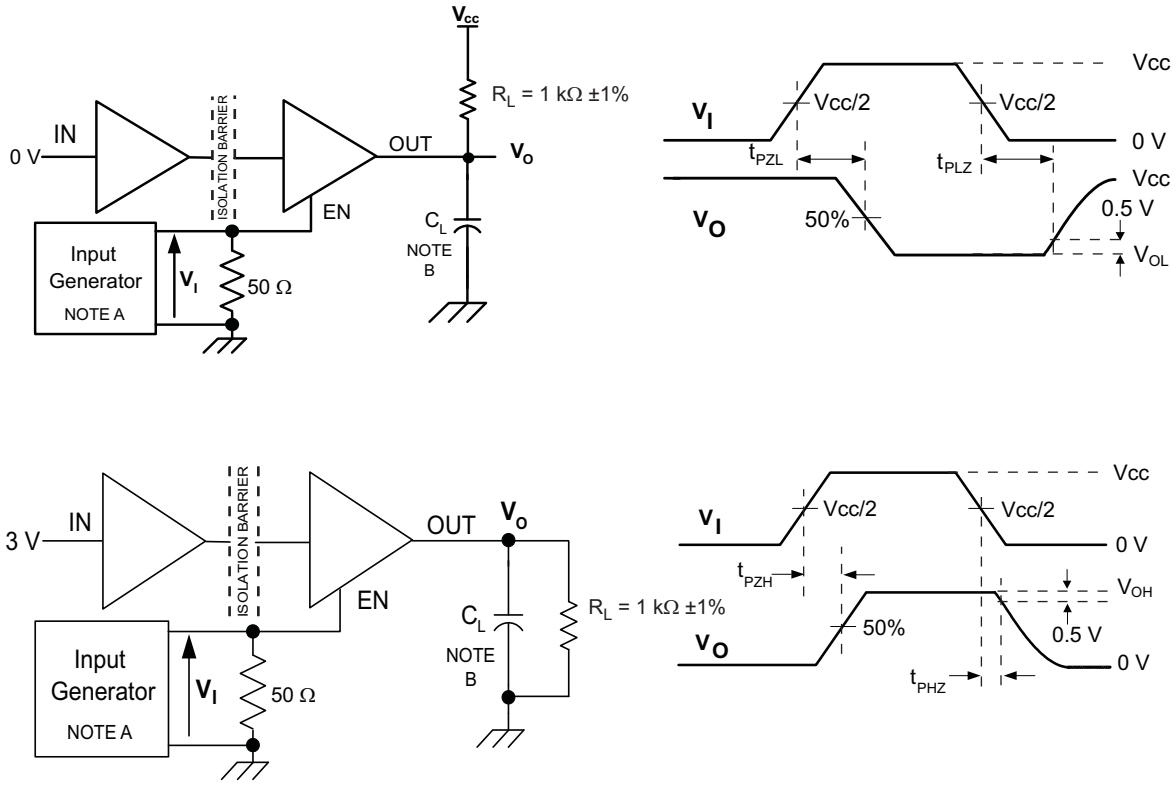
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

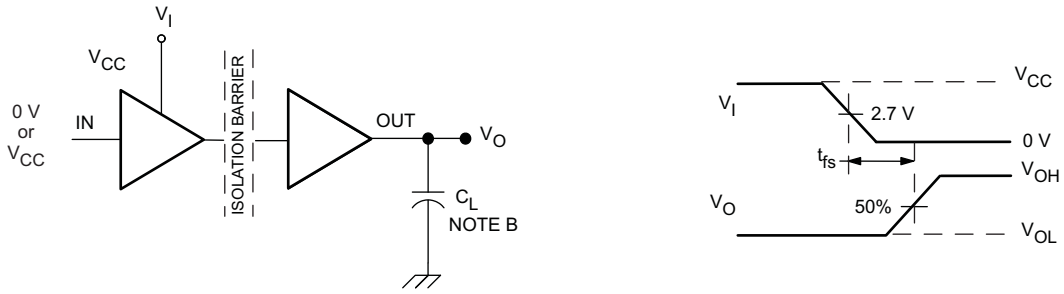


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

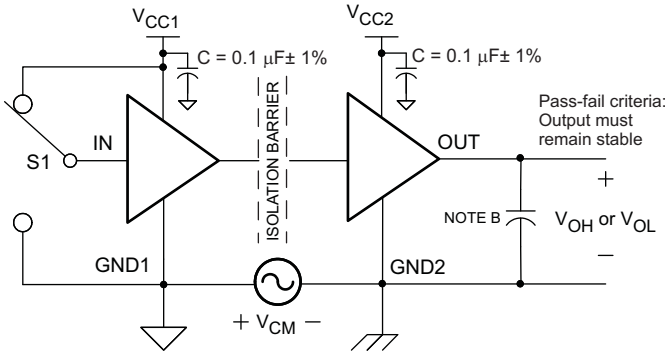
PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

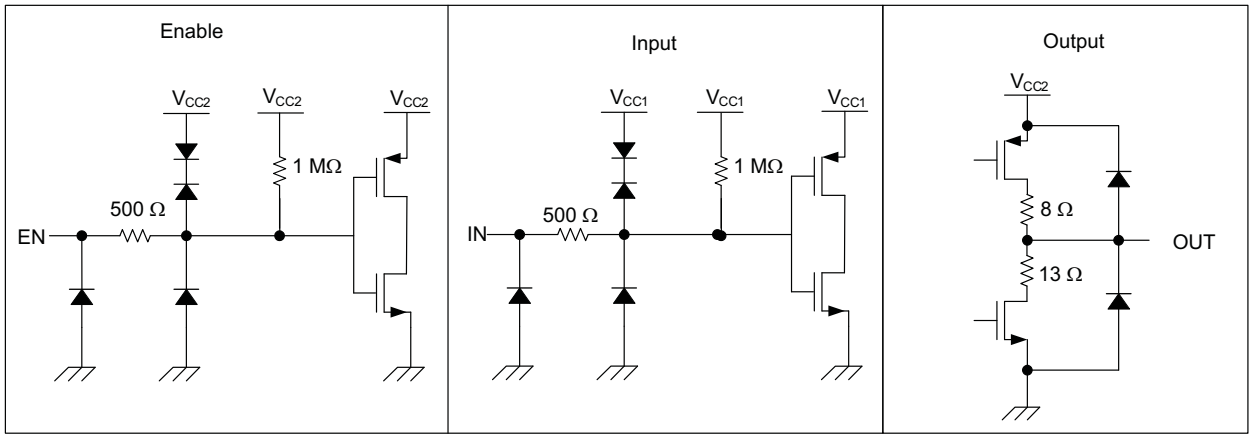
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output, V_{IO} = 500V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

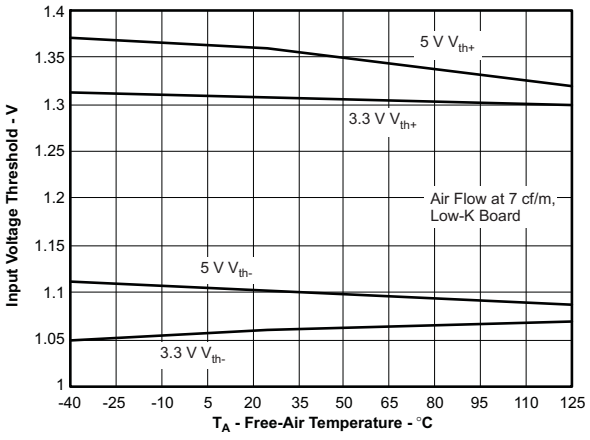


Figure 5.

V_{CC1} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

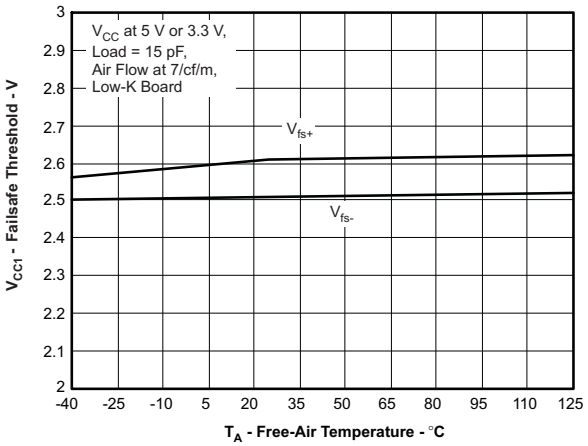


Figure 6.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

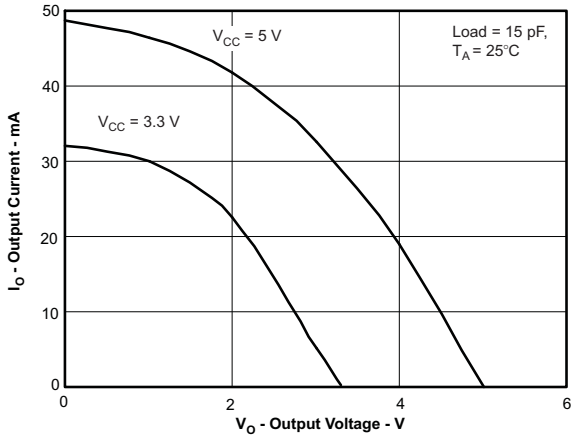


Figure 7.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

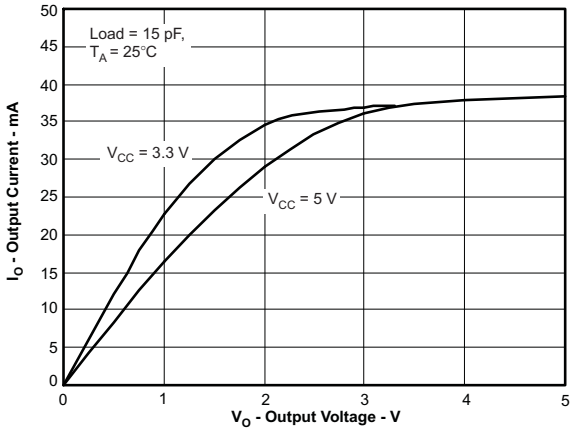


Figure 8.

APPLICATION INFORMATION

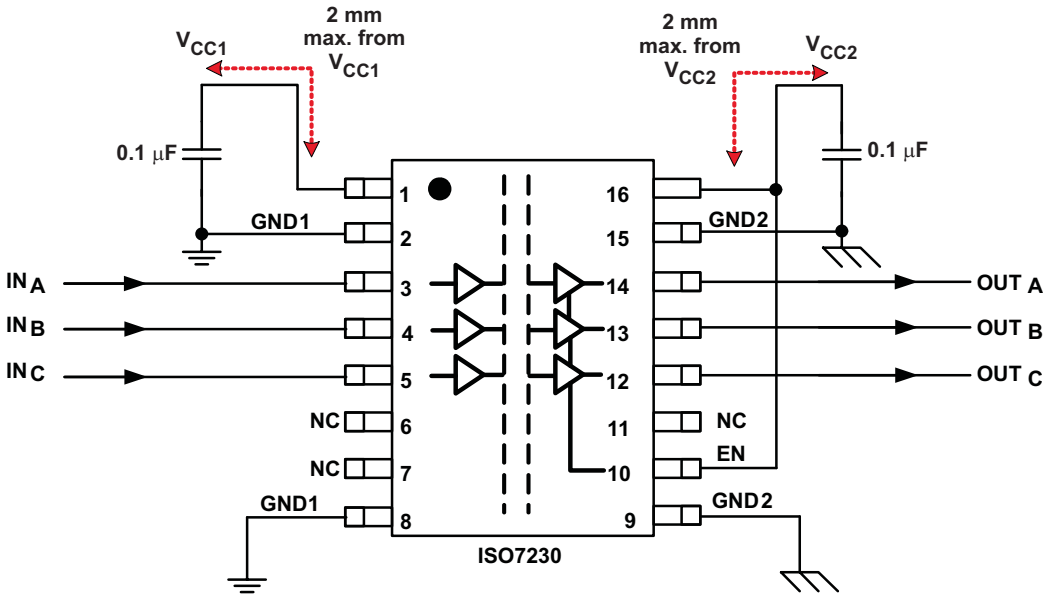


Figure 9. Typical ISO7230 Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

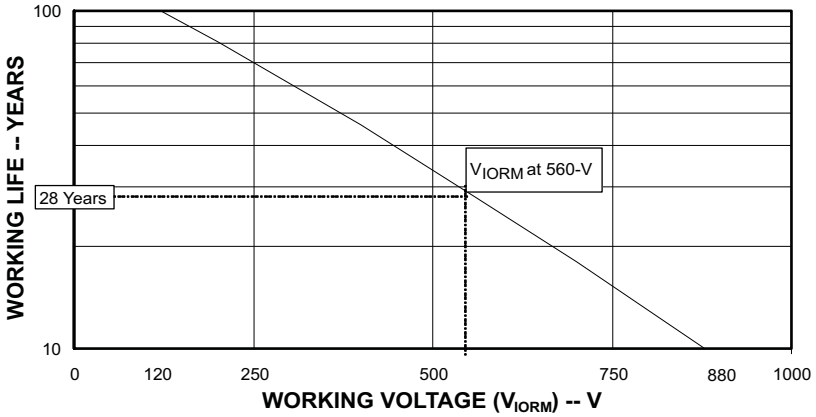


Figure 10. Time Dependant Dielectric Breakdown Testing Results

PRODUCT NOTIFICATION

An ISO723xA anomaly occurs when a negative-going pulse below the specified 1µs minimum bit width is input to the device. The output locks in a logic-low condition until the next rising edge occurs after a 1µs period.

Positive noise edges in pulses of less than the minimum specified 1µs have no effect on the device, and are properly filtered.

To prevent noise from interfering with ISO723xA performance, it is recommended that an appropriately sized capacitor be placed on each input of the device

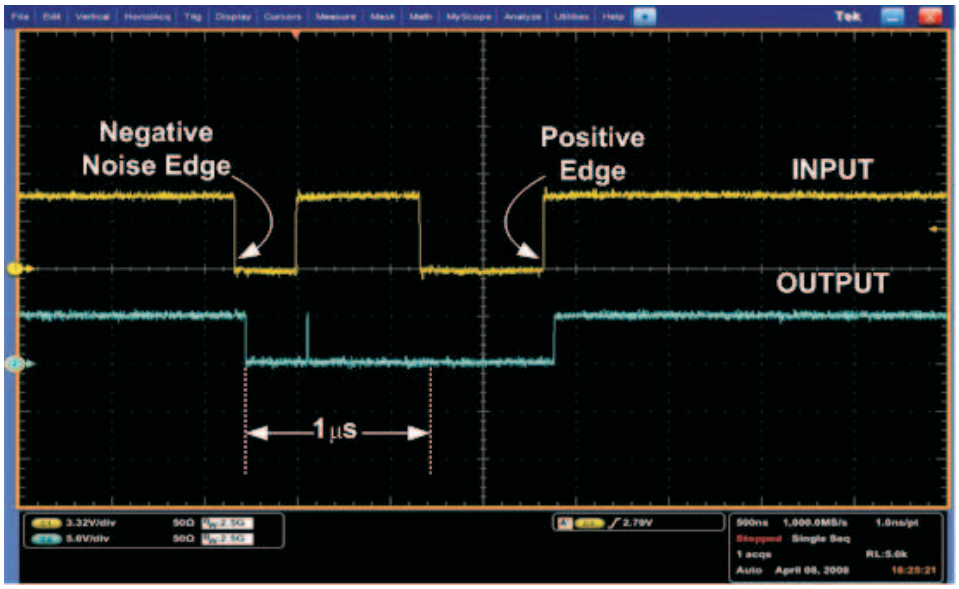


Figure 11. ISO723xA Anomaly

REVISION HISTORY

Changes from Original (May 2008) to Revision A	Page
• Added Product Notification section link.	1
• Deleted text from paragraph 2 of the Description: "and turns off internal bias circuitry to conserve power"	1
• Deleted Product Preview note	2
• Changed From: 3 To: 3.15	3
• Changed V_{CC} From: 3.6 To: 3.45	3
• Changed I_{CC1} and I_{CC2} values From: TBD	4
• Changed V_{CC} – 0.4 To: V_{CC} – 0.8	4
• Changed Typical value from 1 To: 2	4
• Changed Propagation delay max From: 80 To: 95	4
• Changed I_{CC1} and I_{CC2} values From: TBD	5
• Changed Typical value from 1 To: 2	5
• Changed Propagation delay max From: 80 To: 100	5
• Changed I_{CC1} and I_{CC2} values From: TBD	6
• Changed Typical value from 1 To: 2	6
• Changed Propagation delay max From: 80 To: 100	6
• Changed I_{CC1} and I_{CC2} values From: TBD	7
• Changed	7
• Changed Typical value from 1 To: 2	7
• Changed Propagation delay max From: 85 To: 110	7
• Changed L(101) Minimum air gap (Clearance) - minimum value from: 7.7mm to: 8.34mm	10
• Changed Typical value from 1 To: 2	10
• Changed Typical value from 1 To: 2	10
• Changed the REGULATORY INFORMATION Table	10
• Changed Figure 11	13

Changes from Revision A (June 2008) to Revision B	Page
• Changed V_{CC} From: 3.45 To: 3.6	3

Changes from Revision B (July 2008) to Revision C	Page
• Changed "1ns" to "2ns", added "(5v-Operation)"	1
• Changed "2ns" to "10ns", added "(5v-Operation)"	1
• Deleted "Low Jitter Content; 1 ns Typ at 150 Mbps"	1
• Deleted Min = 4.5 V and max = 5.5 V for Supply Voltage of the ROC Table.	3
• Changed V_{CC} From: 3.6 To: 5.5	3
• Corrected Figure 1	8
• Changed File number "1698195" to "220991"	10
• Corrected DEVICE I/O SCHEMATICS	10
• Corrected Figure 9	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7230ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230A	
ISO7230ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230A	
ISO7230ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230A	
ISO7231ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231A	
ISO7231ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231A	
ISO7231ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231A	
ISO7231ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

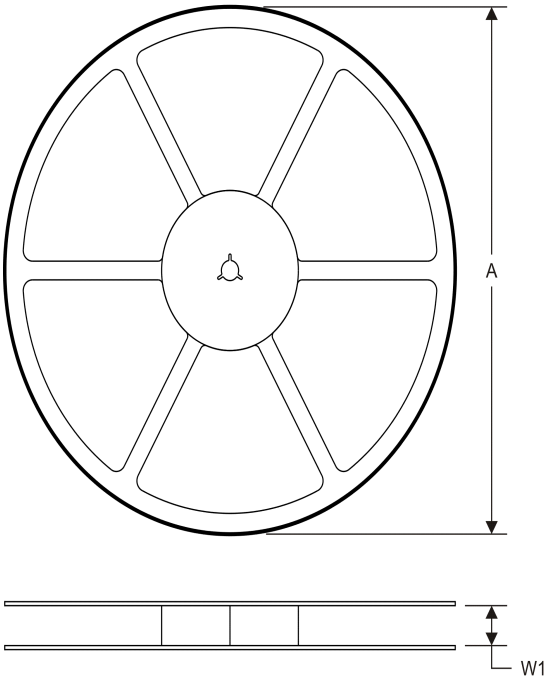
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

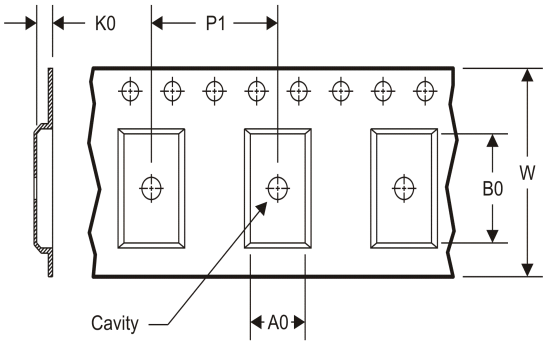
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



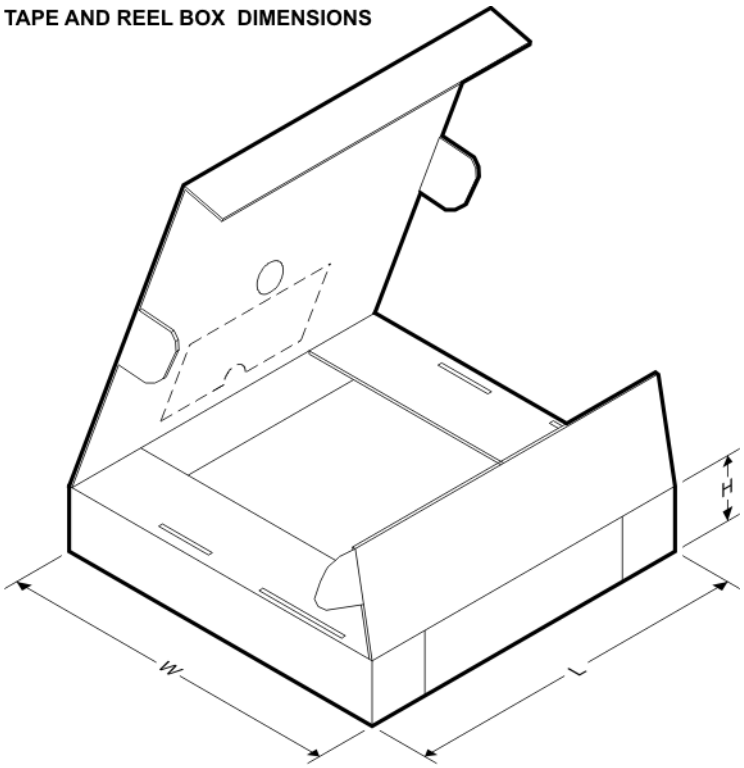
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



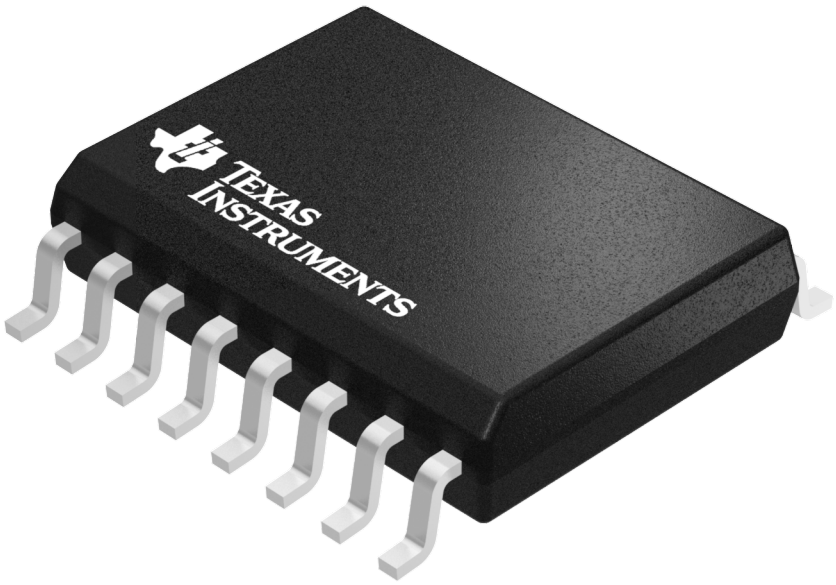
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230ADWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7231ADWR	SOIC	DW	16	2000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

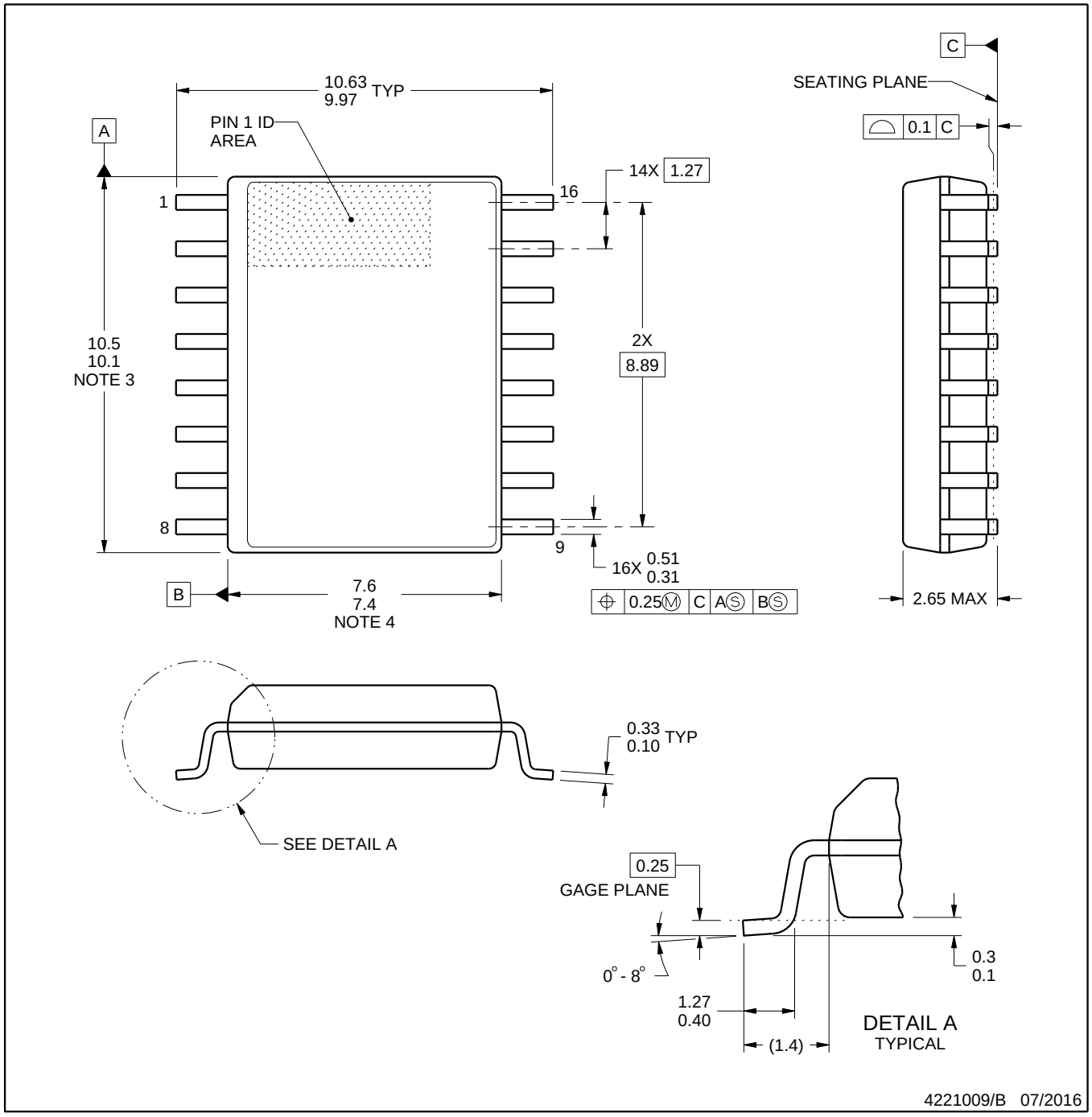
DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



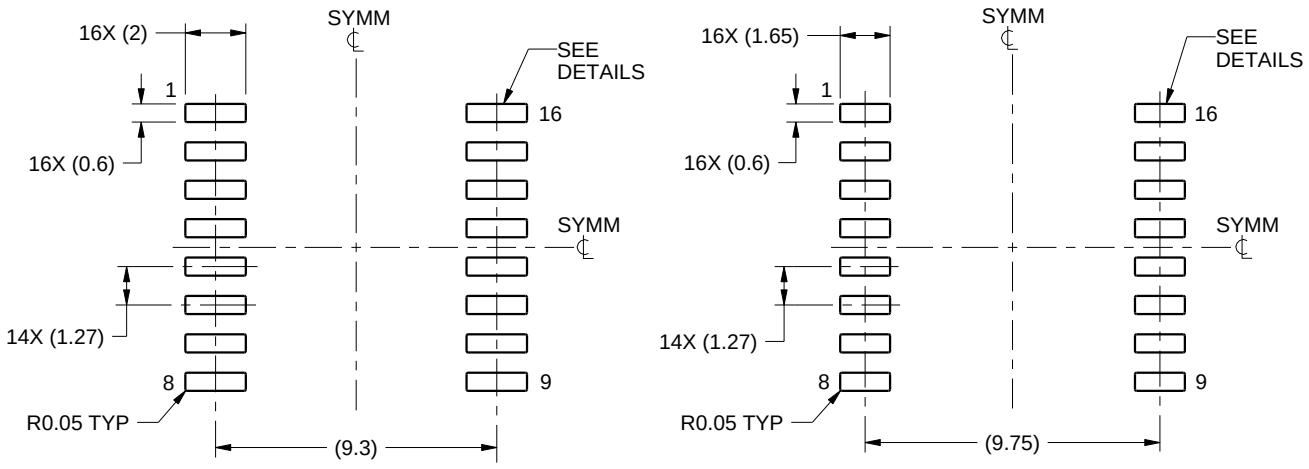
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

SOIC



NOTES:

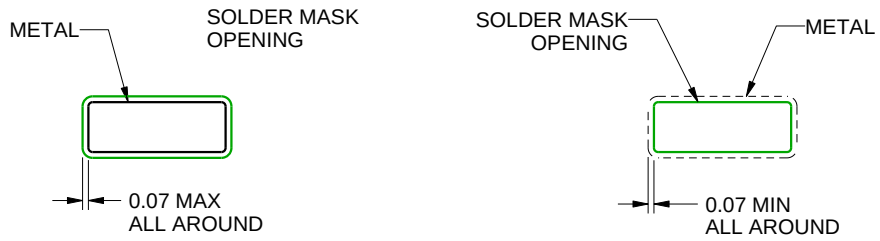
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

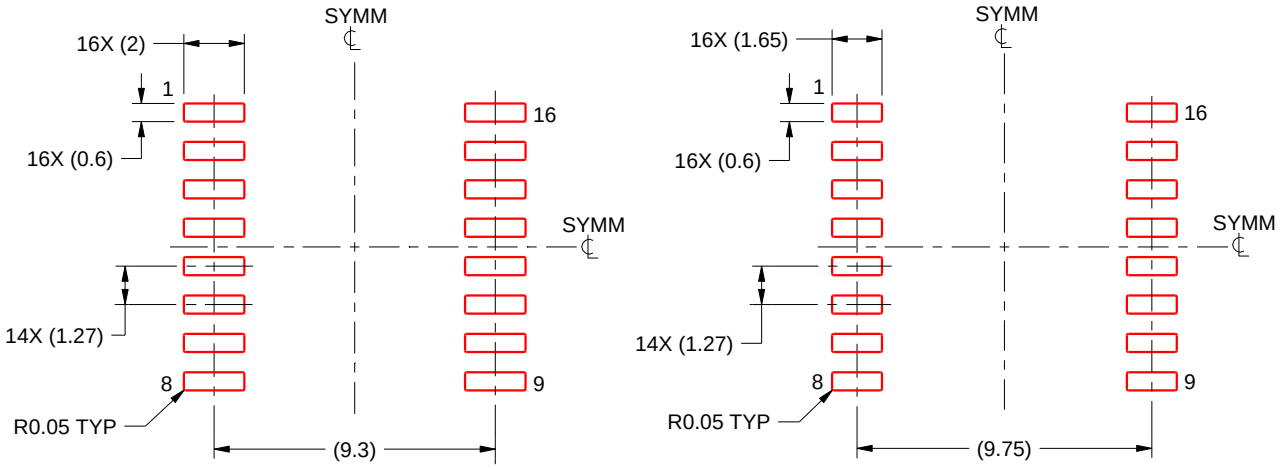
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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