# LF442 Dual Low Power JFET Input Operational Amplifier

## 1 Features

- 1/10 Supply Current of a LM1458: 400 µA (Max)
- Low Input Bias Current: 50 pA (Max)
- Low Input Offset Voltage: 1 mV (Max)
- Low Input Offset Voltage Drift: 7 µV/°C (Typ)
- High Gain Bandwidth: 1 MHz
- High Slew Rate: 1 V/µs
- Low Noise Voltage for Low Power: 35 nV/$\sqrt{Hz}$
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- High Input Impedance: $10^{12}\Omega$
- High Gain $V_O$ = ±10V, $R_L$ = 10k: 50k (Min)

## 2 Applications

- High Speed Integrators
- Fast D/A Converters
- Sample and Hold Circuits

## 3 Description

The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming ensures very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

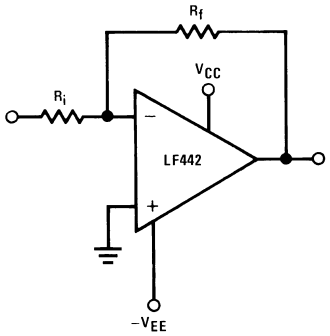
The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LF442ACN | PDIP (8) | 9.59 mm × 6.35 mm |
| LF442AMH | TO-99 (8) | 8.96 mm Diameter |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Inverting Amplifier**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (October 2013) to Revision F** — **Page**

- Deleted Max $\Delta V_{OS/\Delta T}$ specification for LF442A. ... 5

**Changes from Revision D (March 2013) to Revision E** — **Page**

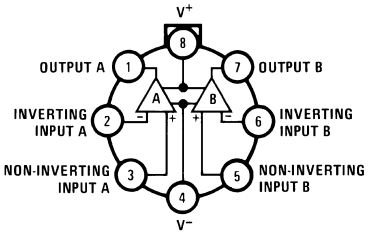
- Changed Input Noise Voltage units ... 5

**Changes from Revision C (March 2013) to Revision D** — **Page**

- Changed layout of data sheet from National to TI format ... 1

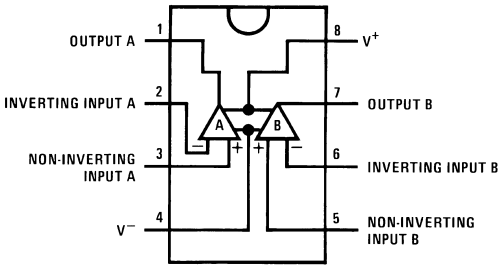
# 5 Pin Configuration and Functions

**TO Package**
**See Package Number LMC0008C**
**Top View**




Pin 4 connected to case

**PDIP Package**
**See Package Number P0008E**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| Output A | 1 | Output | Amplifier A Output |
| Inverting Input A | 2 | Input | Amplifier A Inverting Input |
| Non-Inverting Input A | 3 | Input | Amplifier A Non-Inverting Input |
| V- | 4 | Power | Negative Supply |
| Non-Inverting Input B | 5 | Input | Amplifier B Non-Inverting Input |
| Inverting Input B | 6 | Input | Amplifier B Inverting Input |
| Output B | 7 | Output | Amplifier B Output |
| V+ | 8 | Power | Positive Supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings (1)(2)

| | LF442A | LF442 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (3) | ±19V | ±15V |
| Output Short Circuit Duration (4) | Continuous | Continuous |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) Refer to RETS442X for LF442MH military specifications.
(3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

## 6.2 Absolute Maximum Ratings (1)(2)

| | LMC0008C Package | P0008E Package |
|---|---|---|
| $T_j$ max | 150°C | 115°C |
| Operating Temperature Range | See (3)(4) | See (3)(4) |
| Lead Temperature (Soldering, 10 sec.) | 260°C | 260°C |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) Refer to RETS442X for LF442MH military specifications.
(3) These devices are available in both the commercial temperature range 0°C ≤ $T_A$ ≤ 70°C and the military temperature range −55°C ≤ $T_A$ ≤ 125°C. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.
(4) The value given is in static air.

## 6.3 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage LF442A | | | ±20 | V |
| Supply Voltage LF442 | | | ±15 | V |

## 6.5 Thermal Information

| THERMAL METRIC (1) | | | LF442 LMC0008C 8 PINS | LF442 P0008E 8 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ (Typical) | Junction-to-ambient thermal resistance | 400 linear feet/min air flow | 65 | 114 | °C/W |
| | | Static air | 165 | 152 | |
| $R_{\theta JC}$ (Typical) | Junction-to-case thermal resistance | | 21 | | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.6 DC Electrical Characteristics[1][2]

| PARAMETER | | TEST CONDITIONS | | LF442A | | | LF442 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OS}$ | Input Offset Voltage | $R_S$ = 10 kΩ, $T_A$ = 25°C | | | 0.5 | 1.0 | | 1.0 | 5.0 | mV |
| | | Over Temperature | | | | | | | 7.5 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S$ = 10 kΩ | | | 7 | | | 7 | | µV/°C |
| $I_{OS}$ | Input Offset Current | $V_S$ = ±15V[1][3] | $T_j$ = 25°C | | 5 | 25 | | 5 | 50 | pA |
| | | | $T_j$ = 70°C | | | 1.5 | | | 1.5 | nA |
| | | | $T_j$ = 125°C | | | 10 | | | | nA |
| $I_B$ | Input Bias Current | $V_S$ = ±15V[1][3] | $T_j$ = 25°C | | 10 | 50 | | 10 | 100 | pA |
| | | | $T_j$ = 70°C | | | 3 | | | 3 | nA |
| | | | $T_j$ = 125°C | | | 20 | | | | nA |
| $R_{IN}$ | Input Resistance | $T_j$ = 25°C | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S$ = ±15V, $V_O$ = ±10V, $R_L$ = 10 kΩ, $T_A$ = 25°C | | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | | 25 | 200 | | 15 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 10 kΩ | | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +18 | | ±11 | +14 | | V |
| | | | | | −17 | | | −12 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S$ ≤ 10 kΩ | | 80 | 100 | | 70 | 95 | | dB |
| PSRR | Supply Voltage Rejection Ratio | See[4] | | 80 | 100 | | 70 | 90 | | dB |
| $I_S$ | Supply Current | | | | 300 | 400 | | 400 | 500 | µA |

(1) Unless otherwise specified, the specifications apply over the full temperature range and for $V_S$ = ±20V for the LF442A and for $V_S$ = ±15V for the LF442. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM}$ = 0.
(2) Refer to RETS442X for LF442MH military specifications.
(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA}P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

## 6.7 AC Electrical Characteristics[1][2]

| PARAMETER | | TEST CONDITIONS | LF442A | | | LF442 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| | Amplifier to Amplifier Coupling | $T_A$ = 25°C, f = 1 Hz-20 kHz (Input Referred) | | −120 | | | −120 | | dB |
| SR | Slew Rate | $V_S$ = ±15V, $T_A$ = 25°C | 0.8 | 1 | | 0.6 | 1 | | V/µs |
| GBW | Gain-Bandwidth Product | $V_S$ = ±15V, $T_A$ = 25°C | 0.8 | 1 | | 0.6 | 1 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A$ = 25°C, $R_S$ = 100Ω, f = 1 kHz | | 35 | | | 35 | | nV/√Hz |
| $i_n$ | Equivalent Input Noise Current | $T_A$ = 25°C, f = 1 kHz | | 0.01 | | | 0.01 | | pA/√Hz |

(1) Unless otherwise specified, the specifications apply over the full temperature range and for $V_S$ = ±20V for the LF442A and for $V_S$ = ±15V for the LF442. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM}$ = 0.
(2) Refer to RETS442X for LF442MH military specifications.

## 6.8 Typical Performance Characteristics

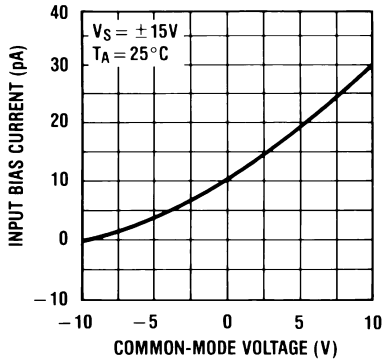



**Figure 1. Input Bias Current**

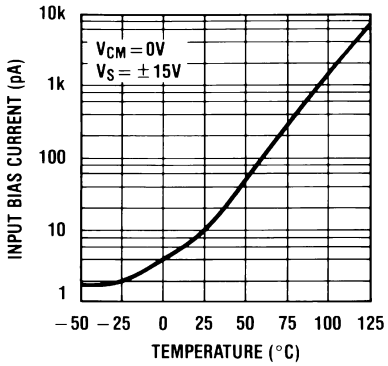



**Figure 2. Input Bias Current**

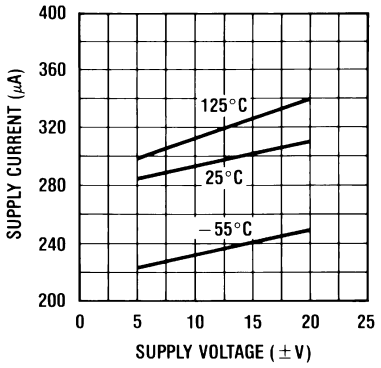



**Figure 3. Supply Current**

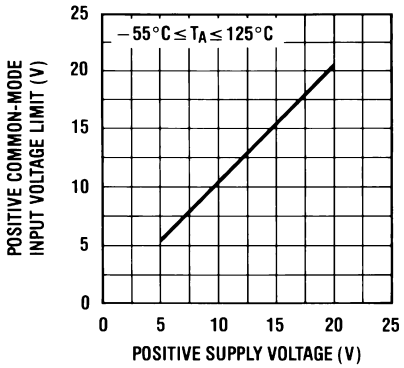



**Figure 4. Positive Common-Mode Input Voltage Limit**

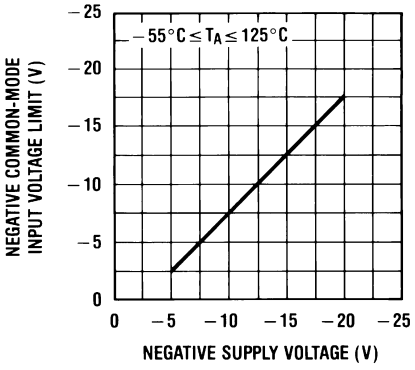



**Figure 5. Negative Common-Mode Input Voltage Limit**

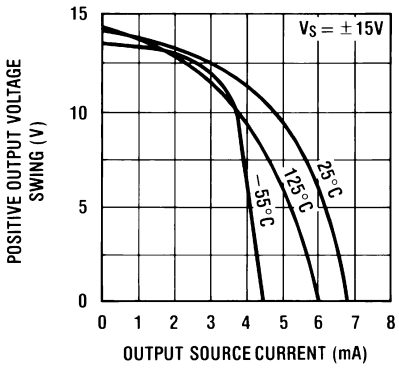



**Figure 6. Positive Current Limit**

## Typical Performance Characteristics (continued)

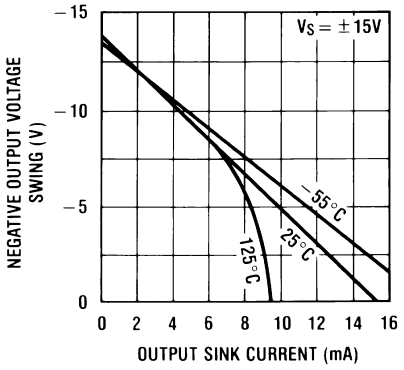



**Figure 7. Negative Current Limit**

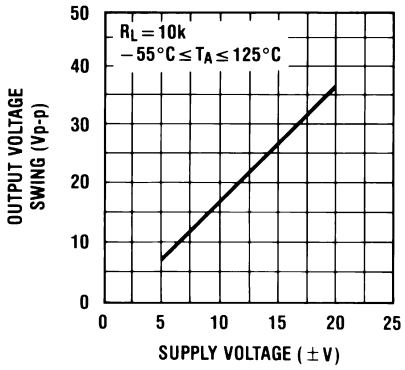



**Figure 8. Output Voltage Swing**

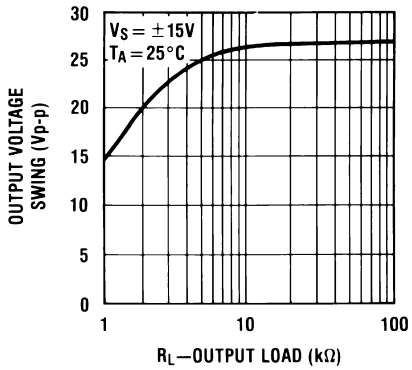



**Figure 9. Output Voltage Swing**

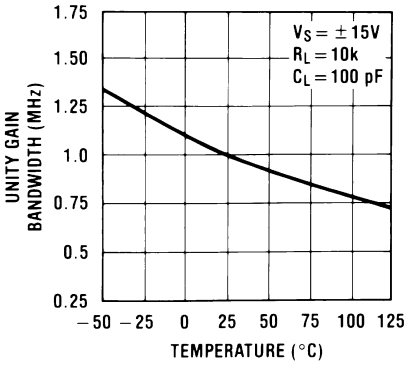



**Figure 10. Gain Bandwidth**

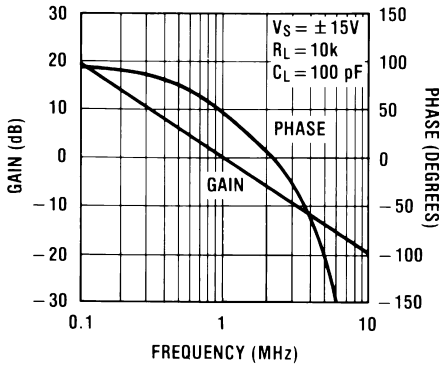



**Figure 11. Bode Plot**

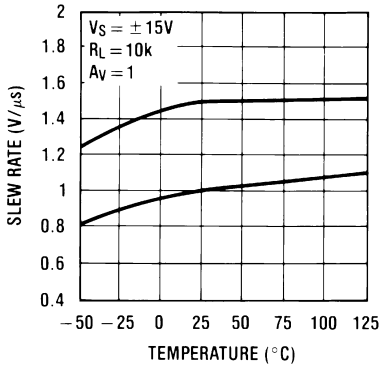



**Figure 12. Slew Rate**

## Typical Performance Characteristics (continued)

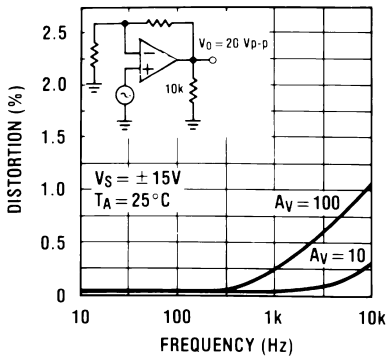



**Figure 13. Distortion vs Frequency**

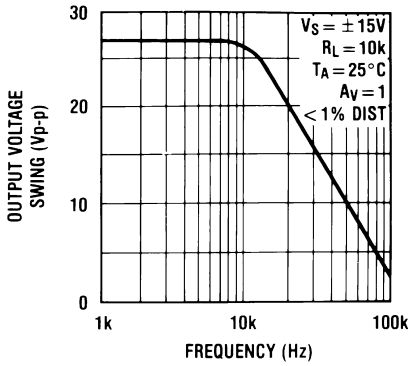



**Figure 14. Undistorted Output Voltage Swing**

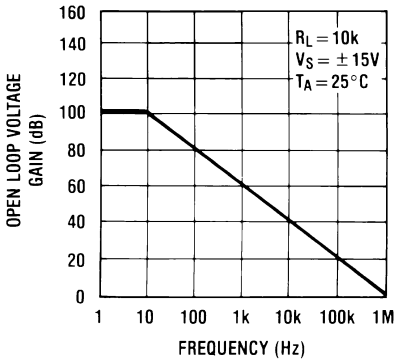



**Figure 15. Open Loop Frequency Response**

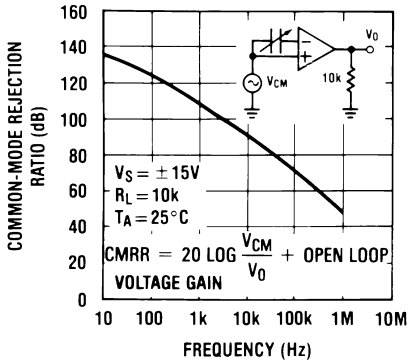



**Figure 16. Common-Mode Rejection Ratio**

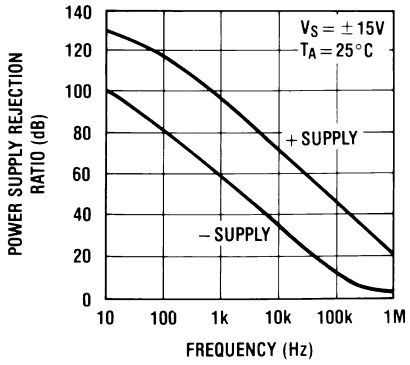



**Figure 17. Power Supply Rejection Ratio**

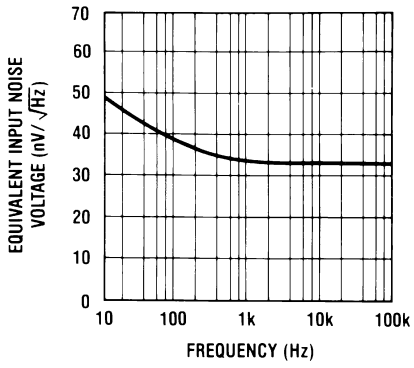



**Figure 18. Equivalent Input Noise Voltage**

## Typical Performance Characteristics (continued)

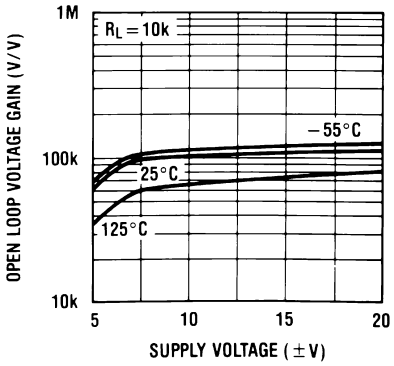



**Figure 19. Open Loop Voltage Gain**

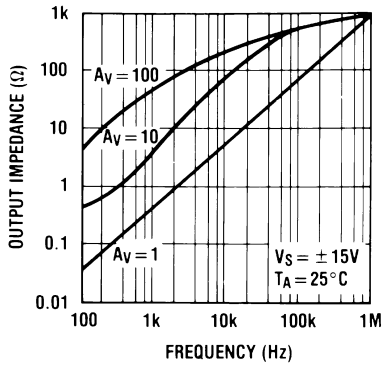



**Figure 20. Output Impedance**

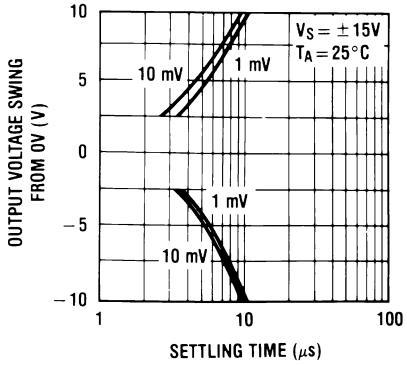



**Figure 21. Inverter Settling Time**

### 6.8.1 Pulse Response

$R_L$ = 10 kΩ, $C_L$ = 10 pF

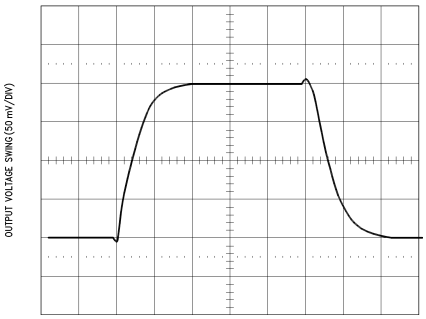



**Figure 22. Small Signal Inverting**

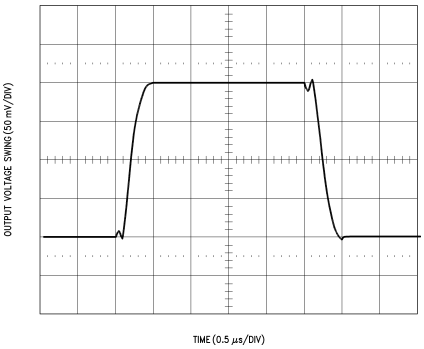



**Figure 23. Small Signal Non-Inverting**

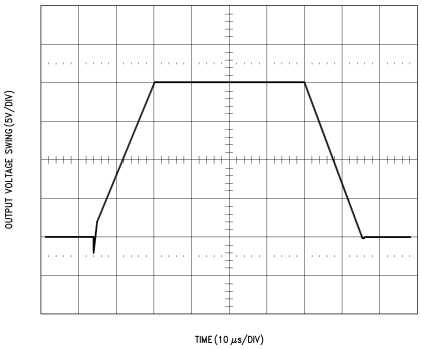



**Figure 24. Large Signal Inverting**

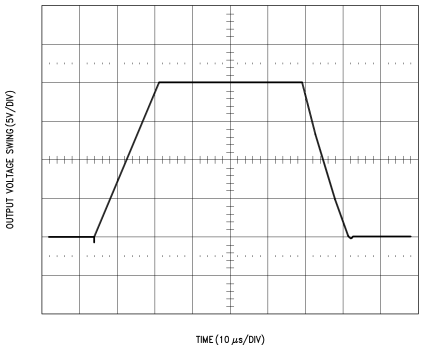



**Figure 25. Large Signal Non-Inverting**

# 7 Detailed Description

## 7.1 Overview

The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming ensures very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

## 7.2 Functional Block Diagram

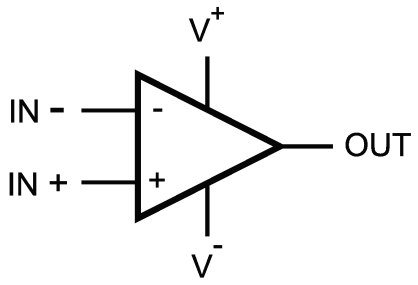



**Figure 26. Each Amplifier**

## 7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp $V_{OUT}$ is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

## 7.4 Device Functional Modes

### 7.4.1 Input and Output Stage

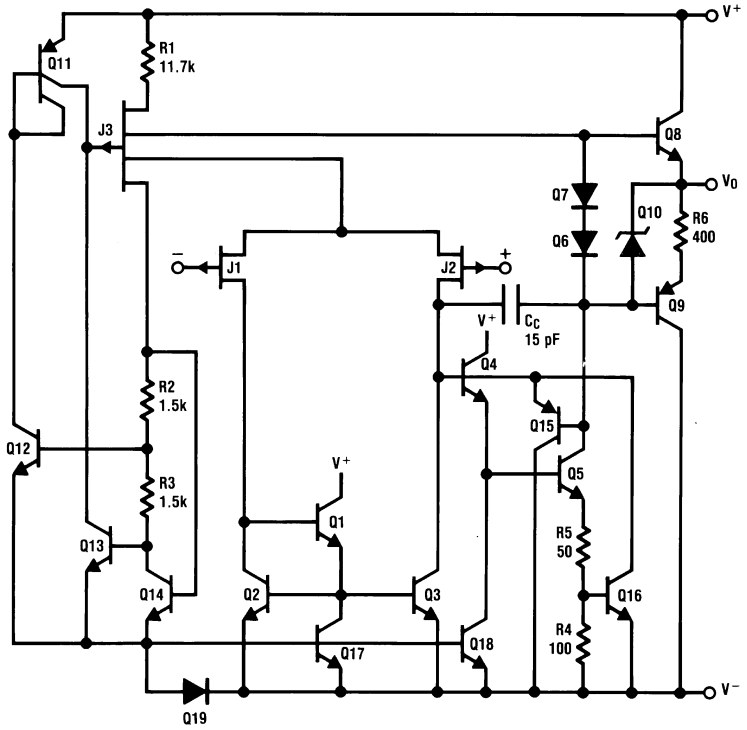



**Figure 27. 1/2 Dual LF442**

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LF442 uses a combination of careful layout design and internal trimming to ensure very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

## 8.2 Typical Applications

1. Battery Powered Strip Chart Preamplifier
2. "No FET" Low Power V to F Converter
3. High Efficiency Crystal Oven Controller
4. Conventional Log Amplifier
5. Unconvential Log Amplifier

### 8.2.1 Battery Powered Strip Chart Preamplifier

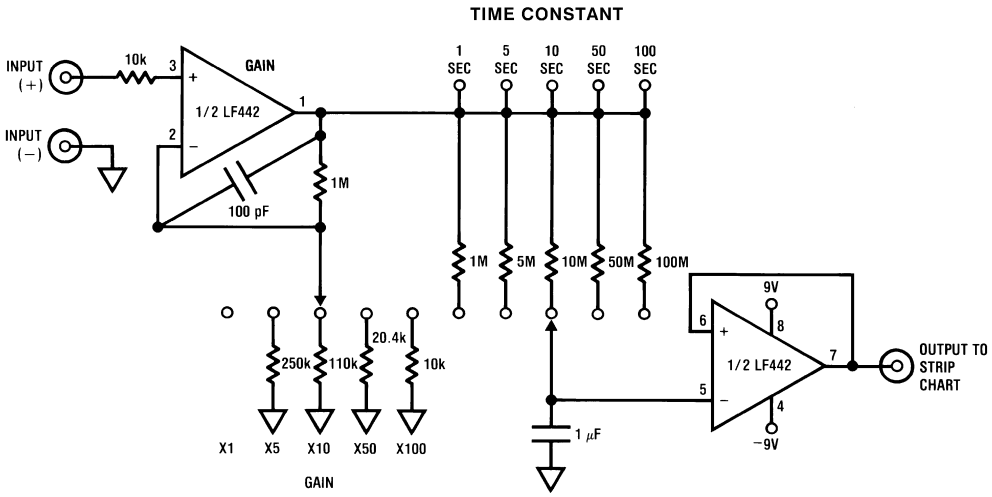



**Figure 28. Battery Powered Strip Chart Preamplifier**

#### *8.2.1.1 Design Requirements*

Runs from 9V batteries (±9V supplies).

Fully settable gain and time constant.

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems.

## Typical Applications (continued)

### 8.2.1.2 Detailed Design Procedure

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

### 8.2.1.3 Application Curves

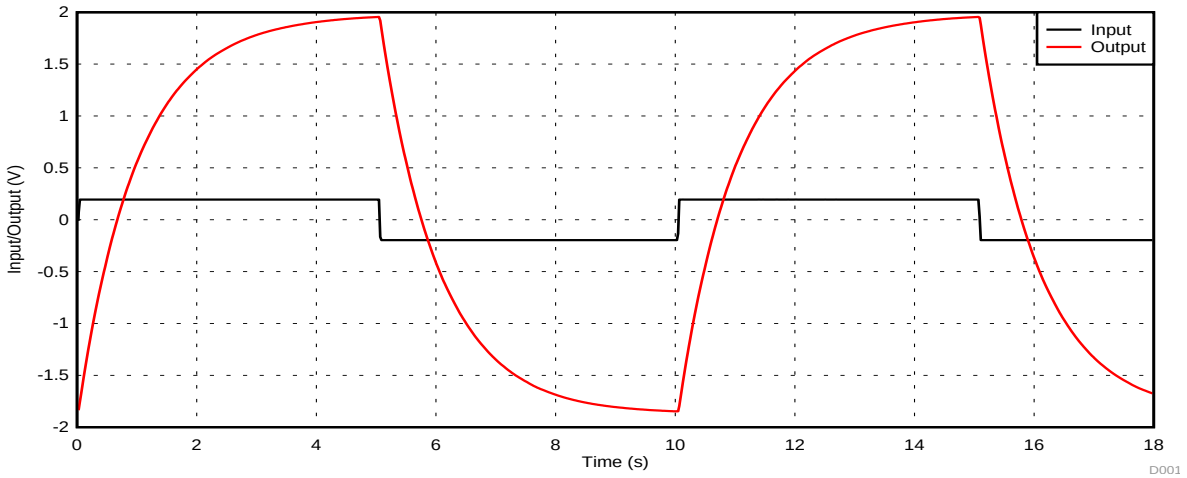



**Figure 29. Input and Output Waveforms, Gain = 10, Time Constant = 1 Second**

## Typical Applications (continued)

### 8.2.2 "No FET" Low Power V to F Converter

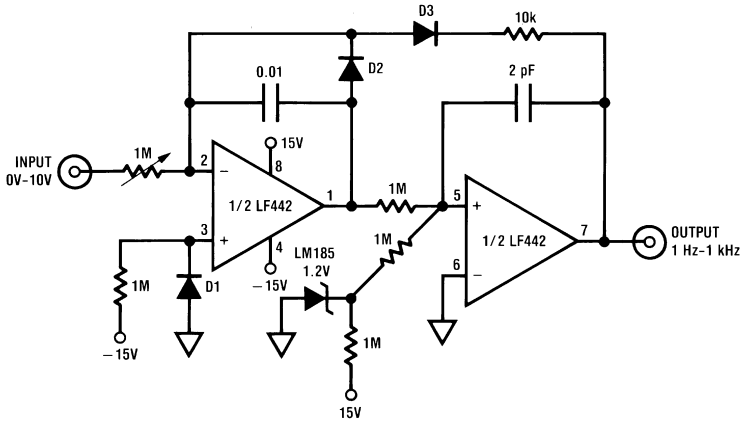



**Figure 30. "No FET" Low Power V to F Converter**

#### *8.2.2.1 Design Requirements*

1. Trim 1M pot for 1 kHz full-scale output.
2. 15 mW power drain.
3. No integrator reset FET required.
4. Mount D1 and D2 in close proximity.
5. 1% linearity to 1 kHz.

#### *8.2.2.2 Detailed Design Procedure*

See Section 8.2.1.2.

#### *8.2.2.3 Application Curves*

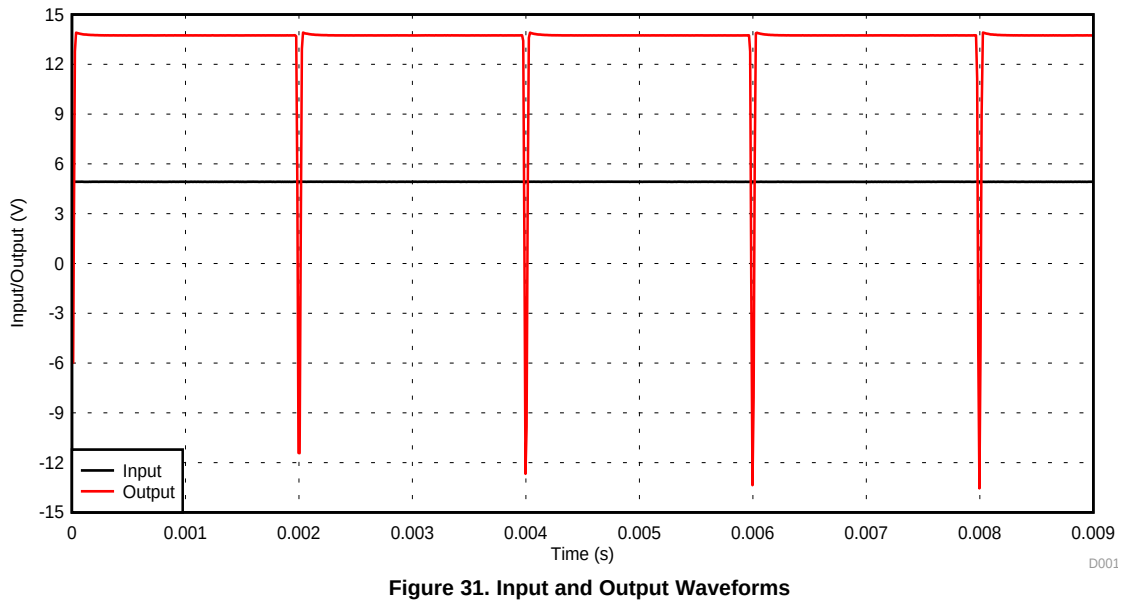



**Figure 31. Input and Output Waveforms**

## Typical Applications (continued)

### 8.2.3 High Efficiency Crystal Oven Controller

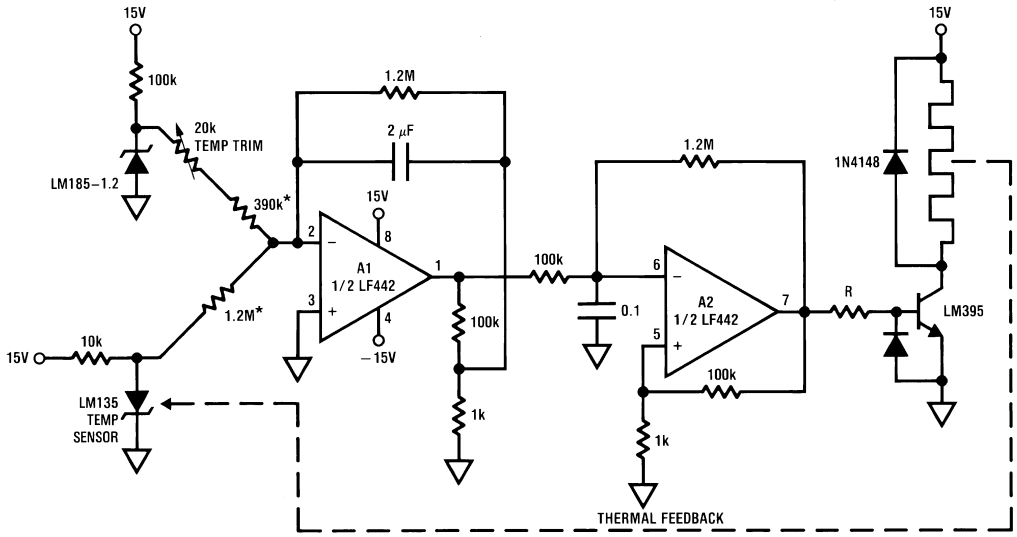



**Figure 32. High Efficiency Crystal Oven Controller**

#### *8.2.3.1 Design Requirements*

1. $T_{control}$= 75°C
2. A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature.
3. A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop.
4. Switched mode operation yields high efficiency.
5. 1% metal film resistor.

#### *8.2.3.2 Detailed Design Procedure*

See Section 8.2.1.2.

### 8.2.4 Conventional Log Amplifier

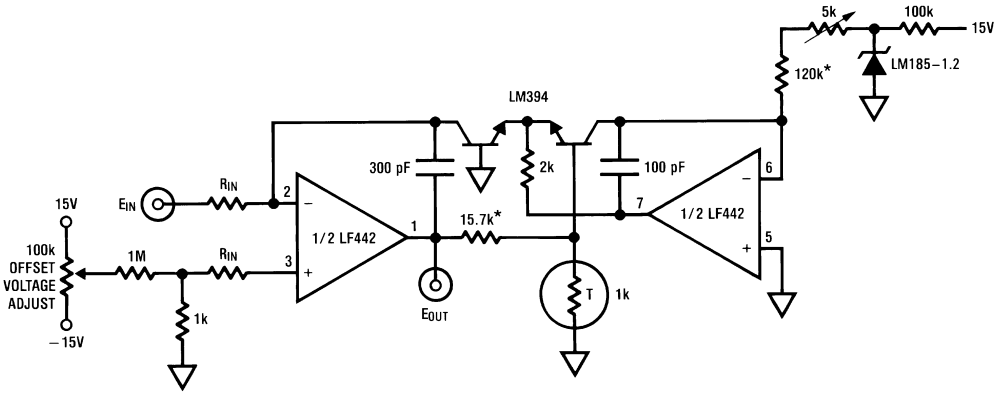



**Figure 33. Conventional Log Amplifier**

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

## Typical Applications (continued)

### 8.2.4.1 Design Requirements

1. $R_T$ = Tel Labs type Q81.
2. Trim 5k for 10 µA through the 5k–120k combination.
3. *1% film resistor

### 8.2.4.2 Detailed Design Procedure

See Section 8.2.1.2.

### 8.2.5 Unconventional Log Amplifier

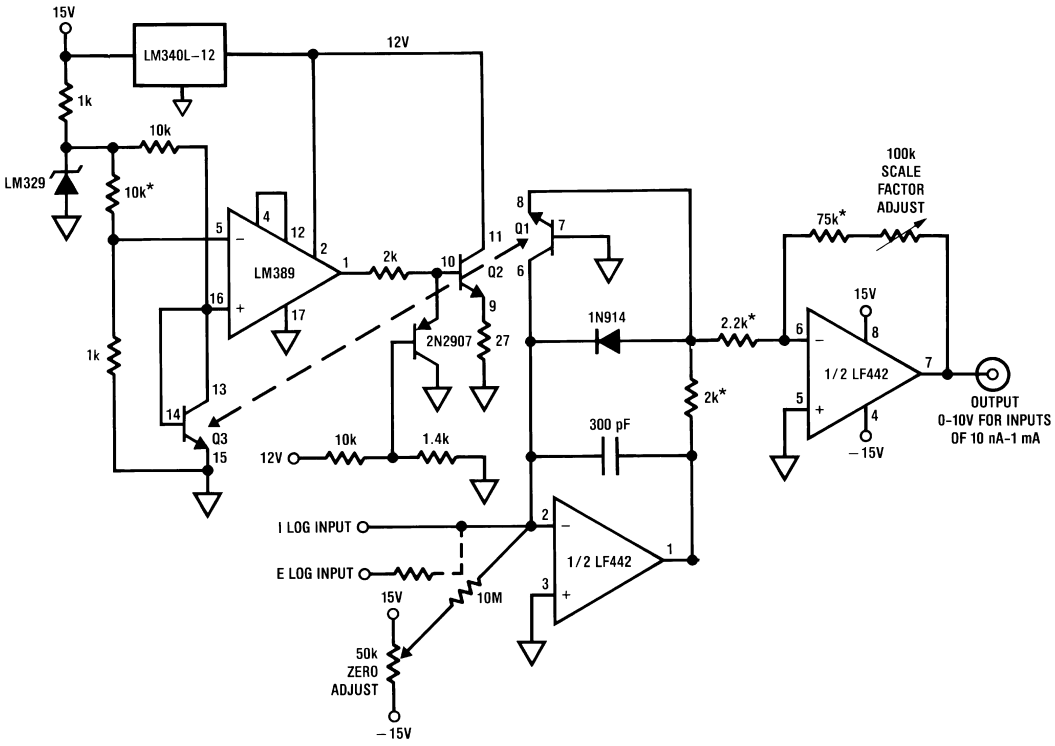



**Figure 34. Unconventional Log Amplifier**

### 8.2.5.1 Design Requirements

1. Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.
2. Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

### 8.2.5.2 Detailed Design Procedure

See Section 8.2.1.2.

# 9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5V.

# 10 Layout

## 10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

## 10.2 Layout Example

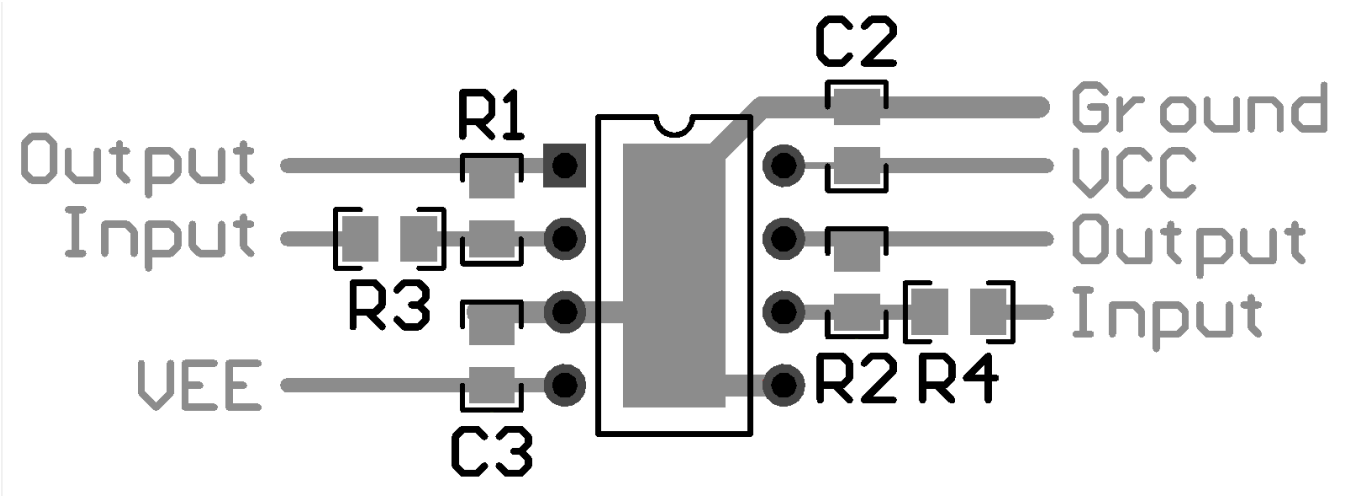



**Figure 35. LF442 Layout**

# 11 Device and Documentation Support

## 11.1 Trademarks

All trademarks are the property of their respective owners.

## 11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LF442ACN/NOPB | LIFEBUY | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | 0 to 70 | LF 442ACN | |
| LF442CN/NOPB | LIFEBUY | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | 0 to 70 | LF 442CN | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

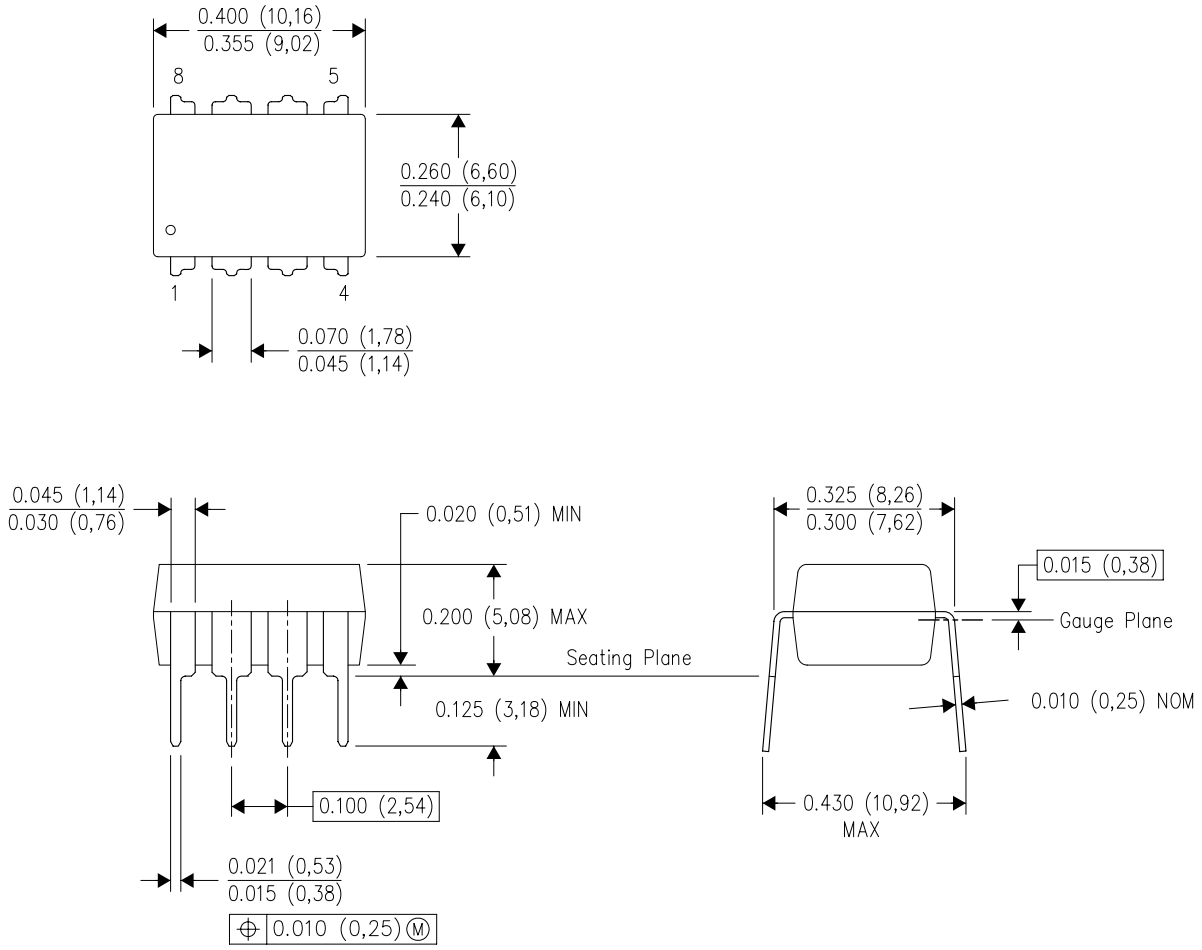
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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