LM2655

LM2655 2.5A High Efficiency Synchronous Switching Regulator

Literature Number: SNVS072C

National Semiconductor

April 2005

LM2655
2.5A High Efficiency Synchronous Switching Regulator

General Description

The LM2655 is a current-mode controlled PWM step-down switching regulator. It has the unique ability to operate in synchronous or asynchronous mode. This gives the designer flexibility to choose between the high efficiency of synchronous operation, or the low solution cost of asynchronous operation. Along with flexibility, the LM2655 offers high power density with the small footprint of a TSSOP-16 package.

High efficiency (>90%) is obtained through the use of an internal low ON-resistance (33mΩ) MOSFET, and an external N-Channel MOSFET. This feature, together with its low quiescent current, makes the LM2655 an ideal fit in portable applications.

Integrated in the LM2655 are all the power, control, and drive functions for asynchronous operation. In addition, a low-side driver output allows easy synchronous operation. The IC uses patented current sensing circuitry that eliminates the external current sensing resistor required by other current-mode DC-DC converters. A programmable soft-start feature limits start up current surges and provides a means of sequencing multiple power supplies.

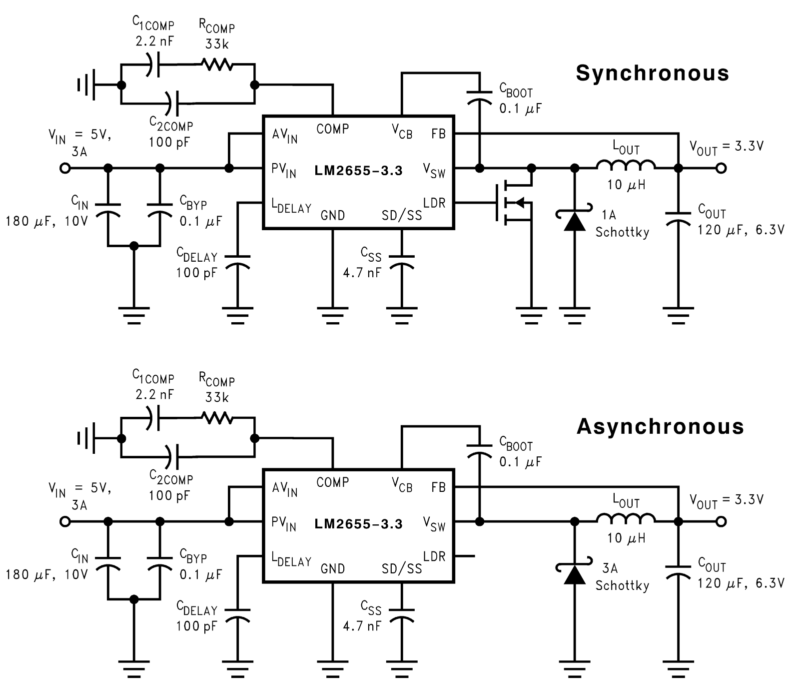
Features

- Ultra-high efficiency up to 96%
- 4V to 14V input voltage range
- Internal high-side MOSFET with low $R_{DS(ON)}$ = 0.033Ω
- 300 kHz fixed frequency internal oscillator
- Low-side drive for synchronous operation
- Guaranteed less than 12 µA shutdown current
- Patented current sensing for current mode control
- Programmable soft-start
- Input undervoltage lockout
- Output overvoltage shutdown protection
- Output undervoltage shutdown protection
- Thermal Shutdown
- 16-pin TSSOP package

Applications

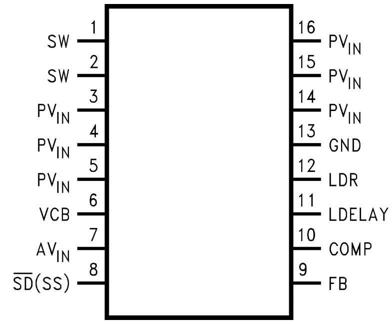
- Hard disk drives
- Internet appliances
- TFT monitors
- Computer peripherals
- Battery powered devices

Typical Application



Connection Diagram

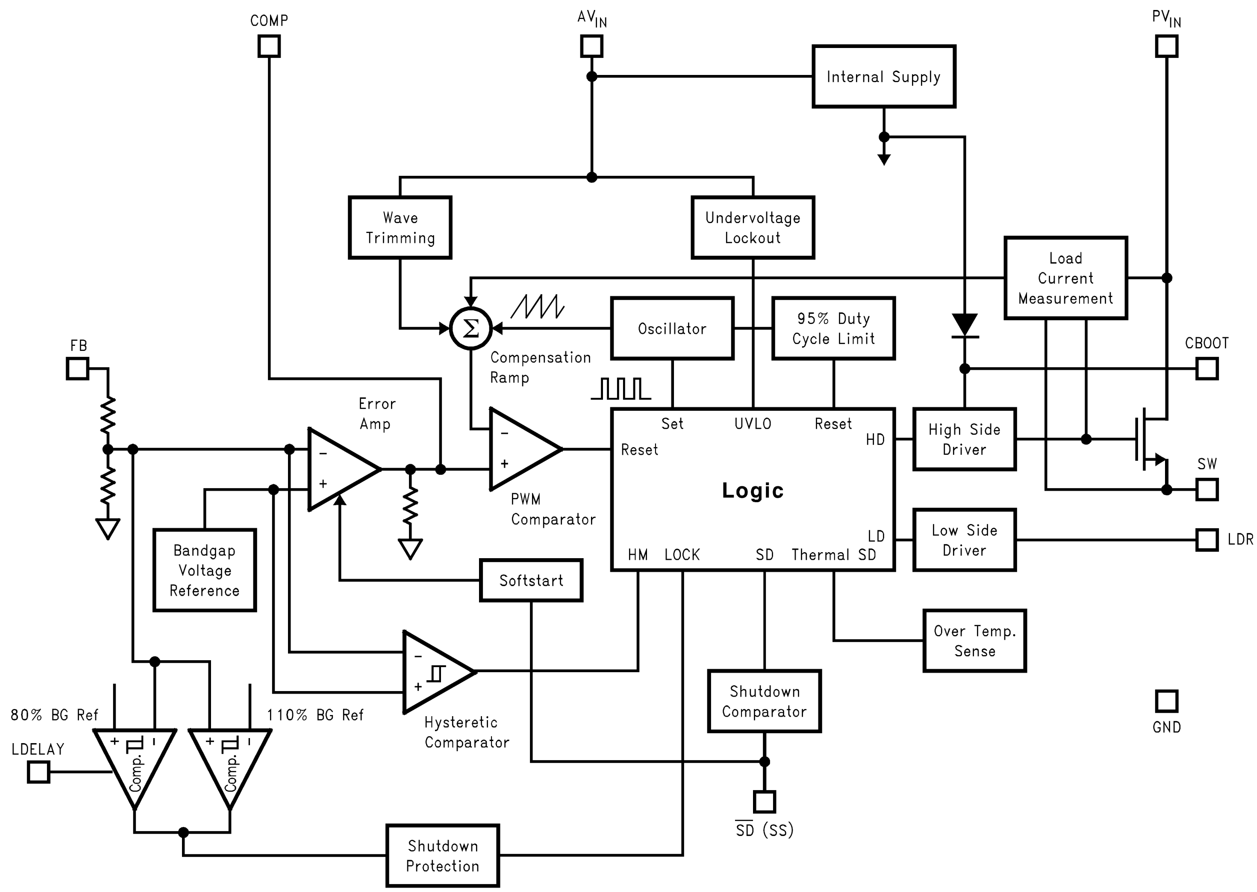
16-Lead TSSOP (MTC)



10128403

Top View
Order Number LM2655MTC-ADJ
See NS Package Number MTC16

Block Diagram



10128404

Pin Description

Pin	Name	Function
1-2	SW	Switched-node connection, which is connected to the source of the internal high-side MOSFET.
3-5	PV_{IN}	Main power supply input pin. Connected to the drain of the internal high-side MOSFET.
6	V_{CB}	Bootstrap capacitor connection for high-side gate drive.
7	AV_{IN}	Input voltage for control and drive circuits.
8	$\overline{SD}$(SS)	Shutdown and Soft-start control pin. Pulling this pin below 0.3V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result.
9	FB	Output voltage feedback input. Connected to the output voltage.
10	COMP	Compensation network connection. Connected to the output of the voltage error amplifier.
11	L_{DELAY}	A capacitor between this pin to ground sets the delay from when the output voltage reaches 80% of its nominal to when the undervoltage latch protection is enabled.
12	LDR	Low-side FET gate drive pin.
13	GND	Power ground.
14-16	PV_{IN}	Main power supply input pin. Connected to the drain of the internal high-side MOSFET.

Ordering Information

Supplied as 1000 units Tape and Reel	Supplied as 3000 units, Tape and Reel
LM2655MTC-3.3	LM2655MTCX-3.3
LM2655MTC-ADJ	LM2655MTCX-ADJ

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (PV_{IN})	3.8V ≤ V_{IN} ≤ 14V
Supply Voltage (AV_{IN})	4.0V ≤ V_{IN} ≤ 14V
Feedback Pin Voltage	-0.4V ≤ V_{FB} ≤ 5V
V_{CB} Voltage, (Note 7)	7V
C_{SS} Voltage	2.5V
Comp Voltage	2.5V
L_{DELAY} Voltage	2.5V
LDR Voltage	5V
V_{SW}, (Note 8)	14V
Power Dissipation (T_A =25˚C), (Note 2)	
TSSOP-16 Package θ_{JA}	140˚C/W
Power Dissapation	893mW
Lead Temperature	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
ESD Susceptibility(Note 3)	
Human Body Model(Note 4)	1kV
Machine Model	200V

Operating Ratings (Note 1)

Storage Temperature Range	–65˚C ≤ T_J ≤ +150˚C
Junction Temperature Range	–40˚C ≤ T_J ≤ +125˚C

LM2655-3.3 Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
V_{OUT}	Output Voltage	I_{LOAD} = 1.5 A	3.3	 3.235/**3.185** 3.392/**3.416**	V V(min) V(max)
V_{OUT}	Output Voltage Line Regulation	V_{IN} = 5V to 14V I_{LOAD} = 1.5 A	0.5	**0.7**	% %(max)
	Output Voltage Load Regulation	I_{LOAD} = 100 mA to 2.5A V_{IN} =10V	0.6	**1.7**	% %(max)
V_{INUV}	V_{IN} Undervoltage Lockout Threshold Voltage	Rising Edge	3.8	**3.95**	V V(max)
V_{UV_HYST}	Hysteresis for the Input Undervoltage Lockout		210		mV
I_{CL}(Note 9)	Average Output Current Limit	V_{IN} = 5V V_{OUT} = 3.3V	3.3		

LM2655-ADJ Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
V_{FB}	Feedback Voltage	I_{LOAD} = 1.5 A	1.238	 1.208/**1.181** 1.260/**1.267**	V V(min) V(max)
V_{OUT}	Output Voltage Line Regulation	V_{IN} = 5V to 14V I_{LOAD} = 1.5 A	0.5	**0.7**	% %(max)
	Output Voltage Load Regulation	I_{LOAD} = 100 mA to 2.5A V_{IN} =10V	0.6	**1.7**	% %(max)
V_{INUV}	V_{IN} Undervoltage Lockout Threshold Voltage	Rising Edge	3.8	**3.95**	V V(max)
V_{UV_HYST}	Hysteresis for the Input Undervoltage Lockout		210		mV
I_{CL}(Note 9)	Average Output Current Limit	V_{IN} = 5V V_{OUT} = 3.3V	3.3		A

All Output Voltage Versions Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 5)	Units
I_Q	Quiescent Current	Shutdown Pin Floating (Device On) Device Not Switching	1.7	**3**	mA mA(max)
I_{QSD}	Quiescent Current in Shutdown Mode	Shutdown Pin Pulled Low	7	12/**20**	µA µA(max)
$R_{DS(ON)}$	Switch ON Resistance	I_{SWITCH} = 1.5A	33	**80**	mΩ mΩ(max)
$R_{SW(ON)}$	Switch On Resistance (MOSFET ON Resistance + Bonding Wire Resistance)	I_{SWITCH} = 1.5A	72		mΩ
I_L	Switch Leakage Current		5		nA
V_{BOOT}	Bootstrap Regulator Voltage	I_{BOOT} = 1 mA C_{BOOT}=tbd	6.7	**6.4** **7.0**	V V(min) V(max)
G_M	Error Amplifier Transconductance		1250		µmho
A_V	Error Amplifier Voltage Gain		100		
I_{EA_SOURCE}	Error Amplifier Source Current	V_{IN} = 4V, V_{FB} = .9*V_{OUT}, V_{COMP} = 2V	40	32/**10**	µA µA(min)
I_{EA_SINK}	Error Amplifier Sink Current	V_{IN} = 4V, V_{FB} = 1.1*V_{OUT}, V_{COMP} = 2V	80	53/**30**	µA µA(min)
V_{EAH}	Error Amplifier Output Swing Upper Limit	V_{IN} = 4V, V_{FB} = .9*V_{OUT}, V_{COMP} = 2V	2.70	2.50/**2.40**	V V(min)
V_{EAL}	Error Amplifier Output Swing Lower Limit	V_{IN} = 4V, V_{FB} = .9*V_{OUT}, V_{COMP} = 2V	1.25	1.35/**1.50**	V V(max)
F_{OSC}	Oscillator Frequency	Measured at Switch Pin V_{IN} = 4V	300	280/**255** 330/**345**	kHz kHz(min) kHz(max)
D_{MAX}	Maximum Duty Cycle	V_{IN} = 4V	95	**92**	% %(min)
I_{SS}	Soft-Start Current	Voltage at the SS Pin = 1.4V	11	**14**	µA µA(max)
V_{OUTUV}	V_{OUT} Undervoltage Lockout Threshold Voltage		81	**76** **84**	$\%V_{OUT}$ $\%V_{OUT}$(min) $\%V_{OUT}$(max)
	Hysteresis for V_{OUTUV}		5		$\%V_{OUT}$
V_{OUTOV}	V_{OUT} Overvoltage Lockout Threshold Voltage		108	**106** **114**	$\%V_{OUT}$ $\%V_{OUT}$(min) $\%V_{OUT}$(max)
	Hysteresis for V_{OUTOV}		5		$\%V_{OUT}$
$I_{LDELAY\_\_SOURCE}$	LDELAY Pin Source Current		5		µA
$I_{SHUTDOWN}$	Shutdown Pin Current	Shutdown Pin Pulled Low	2.2	3.7/**4.0**	µA µA(max)
$V_{SHUTDOWN}$	Shutdown Pin Threshold Voltage	Rising Edge	0.6	**0.25** **0.9**	V V(min) V(max)
T_{SD}	Thermal Shutdown Temperature		165		˚C

All Output Voltage Versions Electrical Characteristics (Continued)

Specifications with standard typeface are for T_J = 25˚C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 5)	Units
T_{SD_HYST}	Thermal Shutdown Hysteresis Temperature		25		˚C

Low-side Driver (LDR) Parameters

Specifications with standard typeface are for T_J = 25˚C, and those in **boldface type** apply over full **Operating Temperature Range**. V_{IN} = 10V unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
V_{OH}	Logic High Level	V_{IN} = 10V	6.8	**6.6**	V V(min)
		V_{IN} = 6.0V	6	**5.8**	V V(min)
V_{OL}	Logic Low Level		0	**0.05**	V V(max)
I_{SINK}	LDR Sink Current	LDR Voltage = 1V	500		mA
I_{SOURCE}	LDR Source Current	LDR Voltage = 2V	180		mA
T_{RR}	Rise Time	C_{GS}=1000pF	18		ns
T_F	Fall Time	C_{GS}=1000pF	7		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 893 mW rating results from using 150˚C, 25˚C, and 140˚C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 140˚C/W represents the worst-case condition of no heat sinking of the 16-pin TSSOP package. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation must be derated by 7.14 mW per ˚C above 25˚C ambient. The LM2655 actively limits its junction temperatures to about 165˚C.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 4: ESD susceptibility using the human body model is 500V for V_{CB}, V_{SW}, LDR, and L_{DELAY}.

Note 5: Typical numbers are at 25˚C and represent the most likely norm.

Note 6: All limits guaranteed at room temperature (standard typeface) and at **temperature extremes (bold typeface)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Measured with respect to V_{SW}.

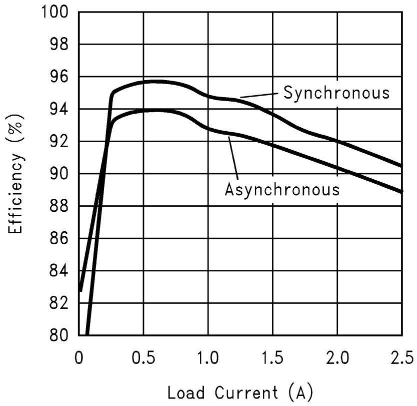
Note 8: Measured while switching in closed loop with Vin = 15V.

Note 9: Average output current limit obtained using typical application circuit. This figure is dependant on the the inductor used.

Note 10: Bond wire resistance accounts for approximately 40mΩ of $R_{SW(ON)}$.

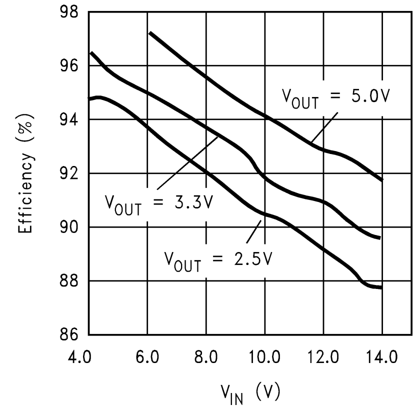
Typical Performance Characteristics

Efficiency vs Load Current (V_{IN} = 5V, V_{OUT} = 3.3V)



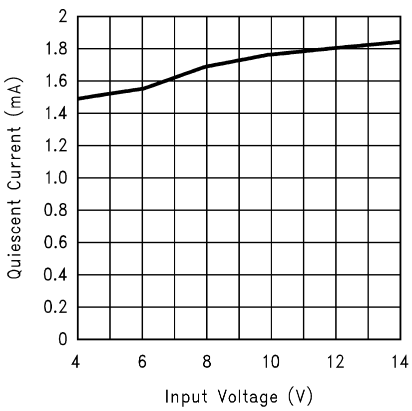
10128405

Efficiency vs V_{IN} (I_{LOAD} = 0.5A) (Synchronous)



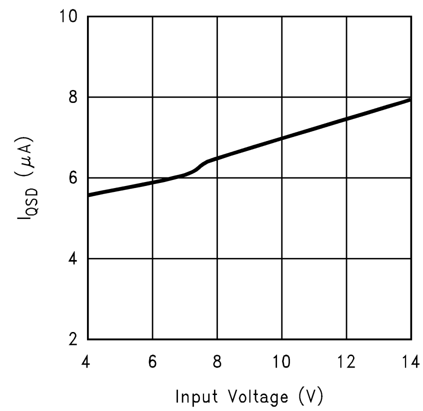
10128406

I_Q vs V_{IN}



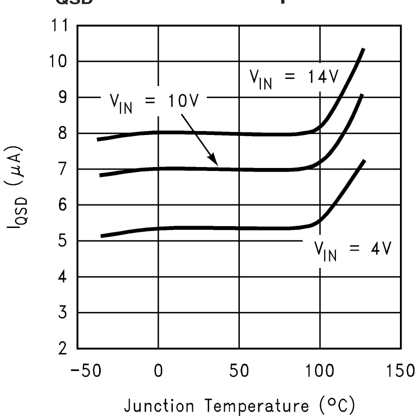
10128407

I_{QSD} vs V_{IN}



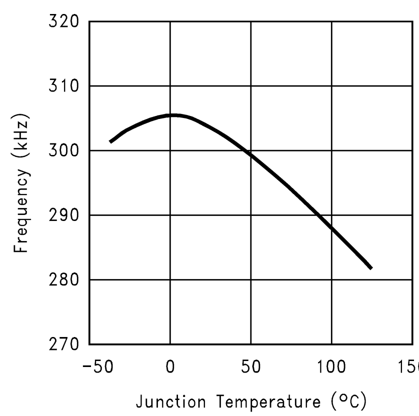
10128408

I_{QSD} vs Junction Temperature



10128409

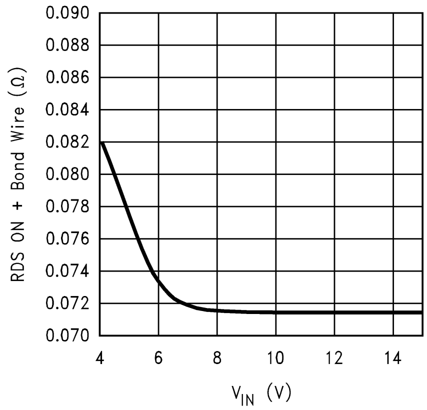
Frequency vs Junction Temperature



10128410

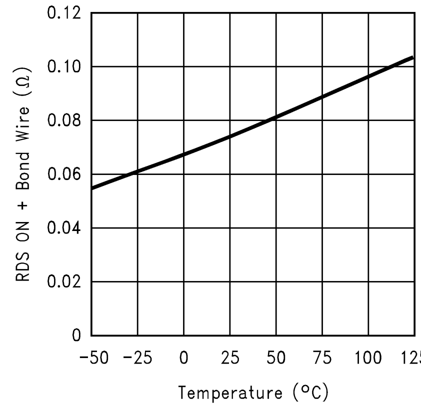
Typical Performance Characteristics (Continued)

$R_{SW(ON)}$ + Bond Wire Resistance vs Input Voltage (Note 10) **(I_{LOAD} = 1.5A)**



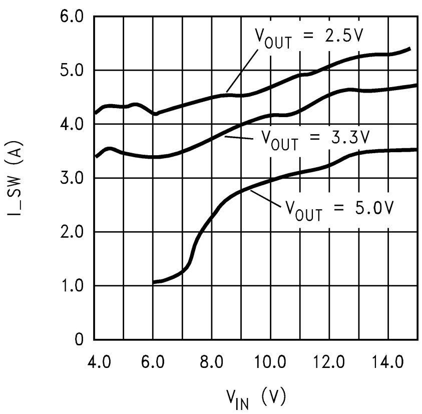
10128411

$R_{SW(ON)}$ + Bond Wire Resistance vs Junction Temperature (Note 10) **(I_{LOAD} = 1.5A, V_{IN} = 5V)**



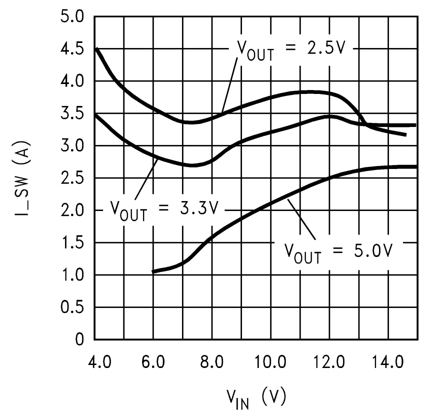
10128412

Current Limit vs Input Voltage (Synchronous)



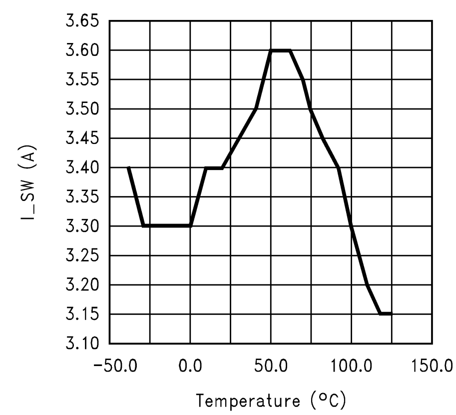
10128413

Current Limit vs Input Voltage (Asynchronous)



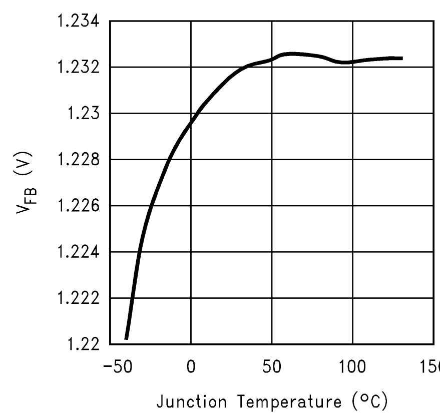
10128414

Current Limit vs Junction Temperature (V_{IN} = 5V, V_{OUT} = 3.3V)



10128415

Reference Voltage vs Junction Temperature



10128416

Operation

The LM2655 is a constant frequency (300kHz), current-mode PWM switcher that can be operated synchronously or asynchronously.

SYNCHRONOUS OPERATION

A converter is said to be in synchronous operation when a MOSFET is used in place of the catch diode. In the case of the buck converter, this MOSFET is known as the low-side MOSFET (the MOSFET connected between the input source and the low-side MOSFET is the high-side MOSFET). Converters in synchronous operation exhibit higher efficiencies compared to asynchronous operation because the I^2R losses are reduced with the use of a MOSFET . Operation of the LM2655 in synchronous mode is identical to its operation in asynchronous mode, except that internal logic drives the low-side MOSFET. At the beginning of a switching cycle, the high-side MOSFET is on and current from the input source flows through the inductor and to the load. The current from the high-side MOSFET is sensed and compared with the output of the error amplifier (COMP pin). When the sensed current reaches the COMP pin voltage level, the high-side switch is turned off. After a 30ns delay (deadtime), the low-side driver goes high and turns the low-side MOSFET on. The current now flows through the low-side MOSFET, through the inductor and on to the load. A 30ns delay is necessary to insure that the MOSFETs are never on at the same time. During the 30ns deadtime, the current is forced to flow through the low-side MOSFET's body diode. It is recommended that a low forward drop schottky diode be placed in parallel to the low-side MOSFET so that current will be more efficiently conducted during this 30ns deadtime. This Schottky diode should be placed within 5mm of the switch pin so that current limit is not effected (see External Schottky Diode section). At the end of the switching cycle, the low-side switch is turned off and after another 30ns delay, the cycle is repeated.

Current through the high-side MOSFET is sensed by patented circuitry that does not require an external sense resistor. As a result, system cost and size are reduced, efficiency is increased, and noise immunity of the sensed current is improved. A feedforward from the input voltage is added to reduce the variation of the current limit over the input voltage range.

ASYNCHRONOUS OPERATION

A unique feature of the LM2655 is that it can be operated in either synchronous or asynchronous mode. When operating in asynchronous mode, a small amount of efficiency is sacrificed for a less expensive solution. Any diode may be used, but it is recommended that a low forward drop schottky diode be use to maximize efficiency. When operating the LM2655 in asynchronous mode, the LDR pin should be terminated with a large resistor (>1 MegΩ), or left floating. Operation in asynchronous mode is similar to that of synchronous mode, except the internal low-side MOSFET logic is not used. At the beginning of a switching cycle, the high-side MOSFET is on and current from the input source flows through the inductor and to the load. The current from the high-side MOSFET is sensed and compared with the output of the error amplifier (COMP pin). When the sensed current reaches the COMP pin voltage level, the high-side switch is turned off. At this instant, the load current is commutated through the catch diode. The current now flows through the diode and the inductor and on to the load. At the end of the switching cycle, the high-side switch is turned on and the cycle is repeated.

PROTECTIONS

The peak current in the system is monitored by cycle-by-cycle current limit circuitry. This circuitry will turn the high-side MOSFET off whenever the current through the high-side MOSFET reaches a preset limit (see plots). A second level current limit is accomplished by the undervoltage protection: if the load pulls the output voltage down below 80% of its nominal value, the undervoltage latch protection will wait for a period of time (set by the capacitor at the LDELAY pin, see LDELAY CAPACITOR section for more information). If the output voltage is still below 80% of its nominal after the waiting period, the latch protection will be enabled. In the latch protection mode, the low-side MOSFET is on and the high-side MOSFET is off. The latch protection will also be enabled immediately whenever the output voltage exceeds the overvoltage threshold (110% of its nominal). Both protections are disabled during start-up.(See SOFT-START CAPACITOR section and LDELAY CAPACITOR section for more information.) Toggling the input supply voltage or the shutdown pin can reset the device from the latched protection mode.

Design Procedure

This section presents guidelines for selecting external components.

INPUT CAPACITOR

A low ESR aluminum, tantalum, ceramic, or any other type of capacitor is needed between the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals $2V_{OUT}$. For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge current tested by the manufacturer to prevent damage by the inrush current. It is also recommended to put a small ceramic capacitor (0.1 µF) between the input pin and ground pin to reduce high frequency noise.

INDUCTOR

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages:

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300\ kHz}$$

A higher value of ripple current reduces inductance, but increases the conductance loss, core loss, current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple require-

Design Procedure (Continued)

ment. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

OUTPUT CAPACITOR

The selection of C_{OUT} is primarily determined by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE}\left(ESR + \frac{1}{8F_S C_{OUT}}\right)$$

The ESR term usually plays the dominant role in determining the voltage ripple. A low ESR aluminum electrolytic or tantalum capacitor (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below –25˚C since its ESR rises dramatically at cold temperature. A tantalum capacitor has a much better ESR specification at cold temperature and is preferred for low temperature applications.

The output voltage ripple in constant frequency mode has to be less than the sleep mode voltage hysteresis to avoid entering the sleep mode at full load:

$$V_{RIPPLE} < 20mV * V_{OUT} / V_{FB}$$

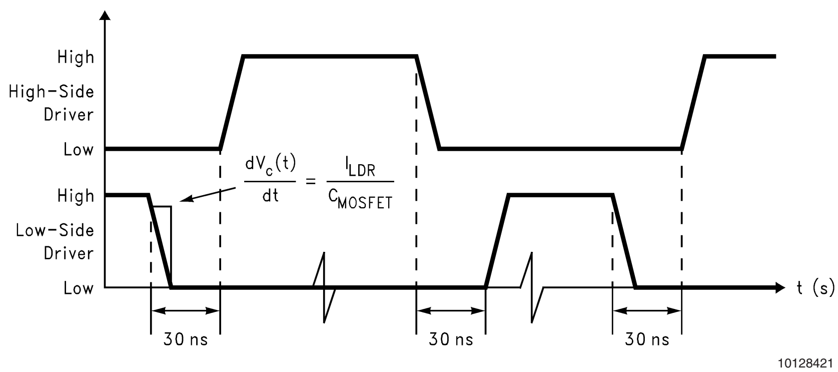


FIGURE 1. Low-side/high-side driver timing diagram.

TABLE 1. MOSFET Manufacturers

Manufacturer	Model Number	Package Type	www Address	Phone	Fax
Fairchild Semiconductor	FDC653N	SuperSOT-6	www.fairchildsemi.com	888-522-5372	207-761-6020
General Semiconductor	GF4420	SO-8	www.gensemi.com	631-847-3000	631-847-3236
International Rectifier	IRF7807	SO-8	www.irf.com	310-322-3331	310-322-3332
Vishay Siliconix	Si4812DY	SO-8	www.vishay.com	800-554-5565	408-567-8995
	Si4874DY	SO-8			
Zetex	ZXM64N03X	SO-8	www.zetex.com	(44) 161-622-4422	(44) 161-622-4420

LOW-SIDE MOSFET SELECTION

When operating in synchronous mode, special attention should be given to the selection of the low-side MOSFET. Besides choosing a MOSFET with minimal size and on resistance, it is critical that the MOSFET meet certain rise and fall time specifications. A 30ns deadtime between the low-side and high-side MOSFET switching transitions is programmed into the LM2655, as shown in *Figure 1*. The prevent shoot-through current, the low-side MOSFET must turn off before the high-side MOSFET turns on. Hence, the low-side MOSFET has 30ns to turn off from the time the low-side driver goes low. The fall time of the low-side MOSFET is governed by the equation:

$I_C = C_{IN} * dV_C/dt$.

where I_C is the LDR sink current capability, C_{IN} is the equivalent capacitance seen at the LDR pin, and V_C is the gate-to-source voltage of the MOSFET. I_C is limited by the low-side driver of the LM2655, but C_{IN} is fixed by the MOSFET. Therefore, it is important that the chosen MOSFET has a suitable C_{IN} so that the LM2655 will be able to turn it off

Design Procedure (Continued)

within 30ns. An input capacitance of less than 1000pF is recommended. Several suitable MOSFETs are shown in *Table 1*.

EXTERNAL SCHOTTKY DIODE (Syncronous)

A Schottky diode is recommended to prevent the intrinsic body diode of the low-side MOSFET from conducting during the deadtime in PWM operation. If the body diode turns on, there is extra power dissipation in the body diode because of the reverse-recovery current and higher forward voltage drop. In addition, the high-side MOSFET has more switching loss because the diode reverse-recovery current adds to the high-side MOSFET turn-on current. These losses degrade the efficiency by 1-2%. The improved efficiency and noise immunity with the Schottky diode become more obvious with increasing input voltage and load current.

It is important to place the diode very close to the switch pin of the LM2655. Extra parasitic impedance due to the trace between the switch pin and the cathode of the diode will cause the current limit to decrease. The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. Since it is on for a short period of time, the diode's average current rating need only be 30% of the maximum output current.

EXTERNAL SCHOTTKY DIODE (Asyncronous)

In asyncronous mode, the output current commutates throught the schottky diode when the high-side MOSFET is turned off. Using a schottky diode with low forward voltage drop will minimize the effeciency loss in the diode. However, to achieve the greatest efficiency, the LM2655 should be operated in syncronous mode using a low-side MOSFET. Since the Schottky diode conducts for the entire second half of the duty cycle in asyncronous mode, it should be rated higher than the full load current.

BOOST CAPACITOR

The boost capacitor provides the extra votage needed to turn the high-side, n-channel MOSFET on. A 0.1 µF ceramic capacitor is recommended for the boost capacitor. The typical voltage across the boost capacitor is 6.7V.

SOFT-START CAPACITOR

A soft-start capacitor is used to provide the soft-start feature. When the input voltage is first applied, or when the $\overline{SD}$(SS) pin is allowed to go high, the soft-start capacitor is charged by a current source (approximately 2 µA). When the $\overline{SD}$(SS) pin voltage reaches 0.6V (shutdown threshold), the internal regulator circuitry starts to operate. The current charging the soft-start capacitor increases from 2 µA to approximately 10 µA. With the $\overline{SD}$(SS) pin voltage between 0.6V and 1.3V, the level of the current limit is zero, which means the output voltage is still zero. When the $\overline{SD}$(SS) pin voltage increases beyond 1.3V, the current limit starts to increase. The switch duty cycle, which is controlled by the level of the current limit, starts with narrow pulses and gradually gets wider. At the same time, the output voltage of the converter increases towards the nominal value, which brings down the output voltage of the error amplifier. When the output of the error amplifier is less than the current limit voltage, it takes over the control of the duty cycle. The converter enters the normal current-mode PWM operation. The $\overline{SD}$(SS) pin voltage is eventually charged up to about 2V.

The soft-start time can be estimated as:

$$T_{SS} = C_{SS} * 0.6V/2\ \mu A + C_{SS} * (2V-0.6V)/10\ \mu A$$

During start-up, the internal circuit is monitoring the soft-start voltage. When the softstart voltage reaches 2V, the undervoltage and overvoltage protections are enabled.

If the output voltage doesn't rise above 80% of the normal value before the soft-start reaches 2V, undervoltage protection shut down the device. You can avoid this by either increasing the value of the soft-start capacitor, or using a LDELAY capacitor.

LDELAY CAPACITOR

The LDELAY capacitor (CDELAY) provides a means to control undervoltage latch protection. By changing CDELAY, the user can adjust the time delay between the output voltage dropping below 80% of its nominal value and the part shutting off due to undervoltage latch protection. The LDELAY circuit consists of a 5 µA current source in series with a user defined capacitor, CDELAY. The 5 µA current source is turned on whenever the output voltage is below 80% of its nominal value, otherwise this current source is off. With the output voltage below 80% of its nominal value, the 5 µA current source begins to charge CDELAY, as shown in *Figure 2*. If the potential across CDELAY reaches 2V, undervoltage latch protection will be enabled and the part will shutdown. If the output voltage recovers to above 80% of its nominal value before the potential across CDELAY reaches 2V, undervoltage latch protection will remain disabled. Hence, CDELAY sets a time delay by the following equation:

$$T_{DELAY}\ (ms) = C_{DELAY}\ (nF) * 2V/5A$$

Undervoltage latch protection can be disabled by tying the LDELAY pin to the ground.

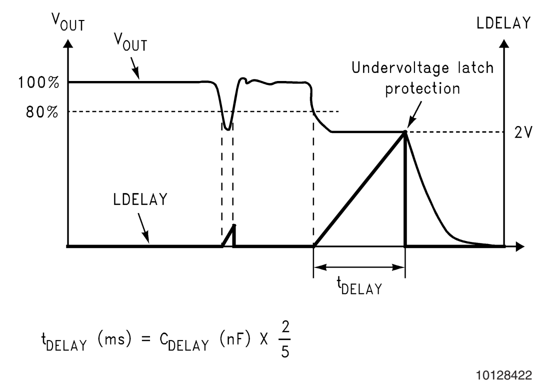


FIGURE 2. Undervoltage latch protection.

COMPENSATION COMPONENTS

In the control to output transfer function, the first pole F_{p1} can be estimated as $1/(2\pi R_{OUT}C_{OUT})$; The ESR zero F_{z1} of the output capacitor is $1/(2\pi ESRC_{OUT})$; Also, there is a high frequency pole F_{p2} in the range of 45kHz to 150kHz:

$$F_{p2} = F_s/(\pi n(1-D))$$

where $D = V_{OUT}/V_{IN}$, $n = 1+0.348L/(V_{IN}-V_{OUT})$ (L is in µHs and V_{IN} and V_{OUT} in volts).

The total loop gain G is approximately $1000/I_{OUT}$ where I_{OUT} is in amperes.

A Gm amplifier is used inside the LM2655. The output resistor R_o of the Gm amplifier is about 80kΩ. C_{c1} and R_C together with R_o give a lag compensation to roll off the gain:

$$F_{pc1} = 1/(2\pi C_{c1}(R_o+R_c)),\ F_{zc1} = 1/2\pi C_{c1}R_c.$$

Design Procedure (Continued)

In some applications, the ESR zero F_{z1} can not be cancelled by F_{p2}. Then, C_{c2} is needed to introduce F_{pc2} to cancel the ESR zero, $F_{p2} = 1/(2\pi C_{c2} R_o \| R_c)$.

The rule of thumb is to have more than 45˚ phase margin at the crossover frequency (G=1).

If C_{OUT} is higher than 68µF, C_{c1} = 2.2nF, and R_c = 15KΩ are good choices for most applications. If the ESR zero is too low to be cancelled by F_{p2}, add C_{c2}.

If the transient response to a step load is important, choose R_C to be higher than 10kΩ.

Application Circuits

PROGRAMMABLE OUTPUT VOLTAGE

Using the adjustable output version of the LM2655 as shown in *Figure 3*, output voltages between 1.24V and 13V can be achieved. Use the following formula to select the appropriate resistor values:

$$R_{FB1} = R_{FB2} * (V_{OUT} - V_{REF}) / V_{REF}$$

where V_{REF} = 1.238V.

Select resistors between 10kΩ and 100kΩ. (1% or higher accuracy metal film resistors for R_{FB1} and R_{FB2}.)

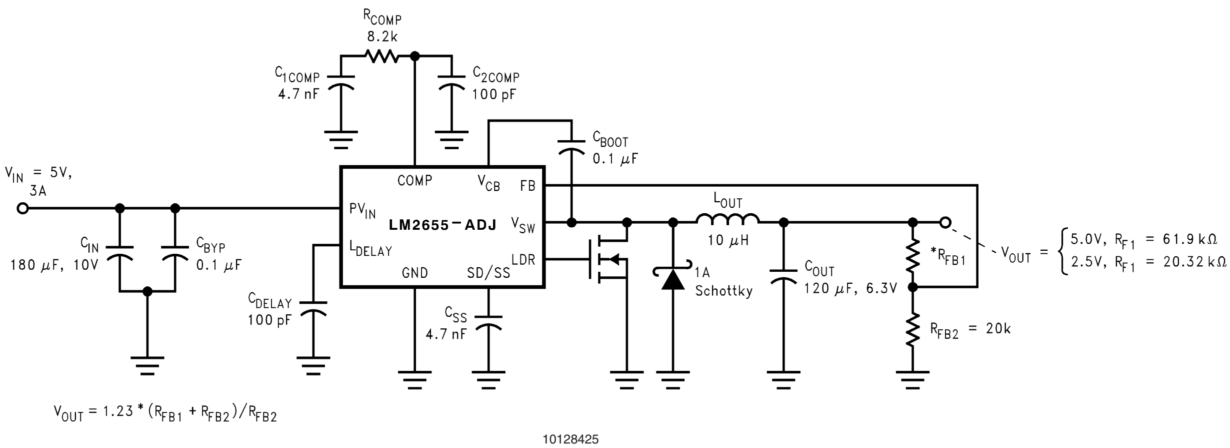


FIGURE 3. Programmable output voltage.

EXTENDING INPUT VOLTAGE RANGE

Figure 4 shows a way to configure the LM2655 so that input voltages of less than 4V can be converted. This circuit makes use of the separate analog and power V_{IN} pins. All the supervisory circuits of the LM2655 are powered through the AV_{IN} pin, while the source voltage that is to be converted is input to the PV_{IN} pins. The internal circuitry of the LM2655 has an operating range of 4V < V_{CC} < 14V, so a voltage within this range must be applied to AV_{IN}. This source may be low power because it only needs to supply 5mA. An input capacitor should be connected across this source, and a small bypass capacitor should be placed physically close to the AV_{IN} pin to ground. With all the internal circuitry being powered by a separate source, the only requirement of the voltage at PV_{IN} is that it be slightly higher (~500mV) than the desired output voltage. The source connected to PV_{IN} will also need an input capacitor and bypass capacitor, but the input capacitor must be selected following the guidelines explained in the INPUT CAPACITOR section.

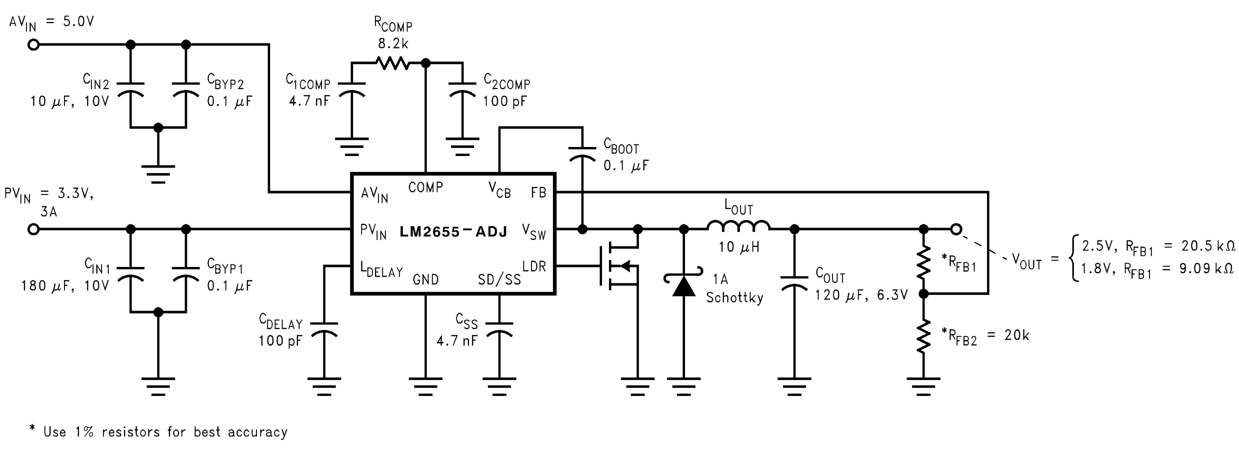


FIGURE 4. Extended input voltage range.

Application Circuits (Continued)

OBTAINING OUTPUT VOLTAGES OF LESS THAN 1.25V

Some applications require output voltages less than 1.25V. The circuit shown in *Figure 5* will allow the LM2655 to do such a conversion. By referencing the two feedback resistors to V_{ADJ} (V_{ADJ} > 1.24V), V_{OUT} can be adjusted from 0V to V_{ADJ} by the equation:

$$V_{OUT} = (V_{REF}-V_{ADJ})*(R_{FB1}+R_{FB2})/R_{FB2} + V_{ADJ}$$

where V_{REF} = 1.24V. V_{ADJ} can be any voltage higher than V_{REF} (1.24V). In *Figure 5*, V_{ADJ} is produced by an LMV431 adjustable reference following the equation:

$$V_{ADJ} = 1.24*(R_{ADJ1}/R_{ADJ2} + 1).$$

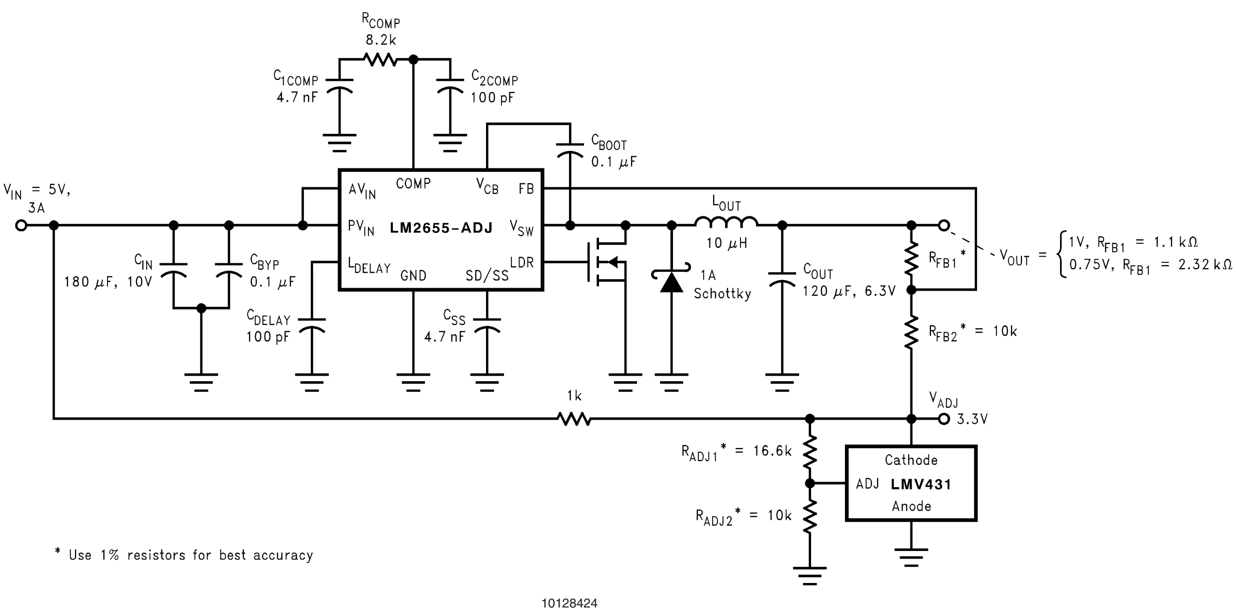
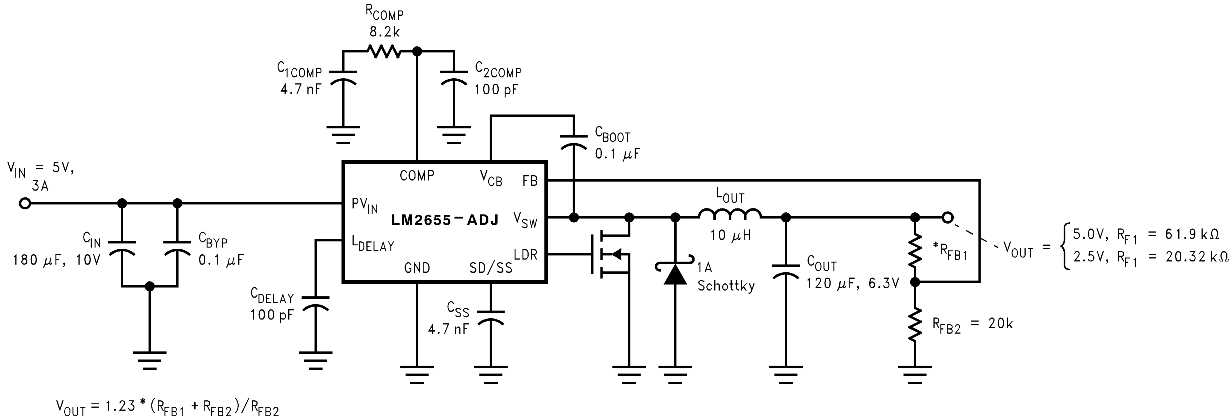


FIGURE 5. Obtaining output voltages of less than 1.25V

Pcb Layout Considerations

Layout is critical to reduce noise and ensure specified performance. The important guidelines are listed as follows:

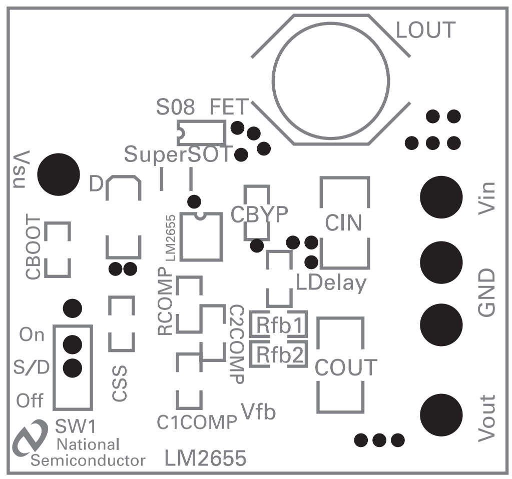
1. Minimize the parasitic inductance in the loop of input capacitors and the internal MOSFETs by connecting the input capacitors to V_{IN} and PGND pins with short and wide traces. The high frequency ceramic bypass capacitor, in particular, should be placed as close to and no more than 5mm from the V_{IN} pin. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes that may result in noise problems.
2. Minimize the trace from the center of the output resistor divider to the FB pin and keep it away from noise sources to avoid noise pick up. For applications that require tight regulation at the output, a dedicated sense trace (separated from the power trace) is recommended to connect the top of the resistor divider to the output.
3. If the Schottky diode D is used, minimize the traces connecting D to SW and PGND pins. Use short and wide traces.
4. If the low-side MOSFET is used, minimize the trace connecting the LDR pin to the gate of the MOSFET, and the traces to SW and PGND pins. Use short and wide traces for the power traces going from the MOSFET to SW and PGND pins.



10128425

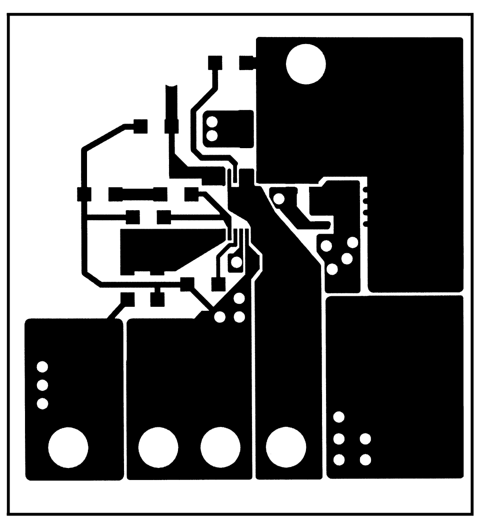
Schematic for the Typical Board Layout

Typical PC Board Layout: (2X Size)



10128426

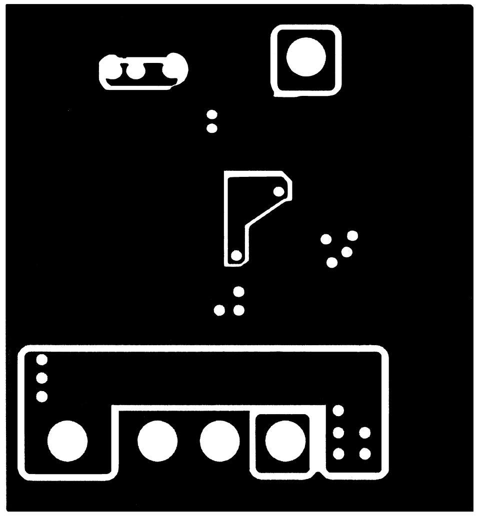
Component Placement Guide



10128427

Component Side PC Board Layout

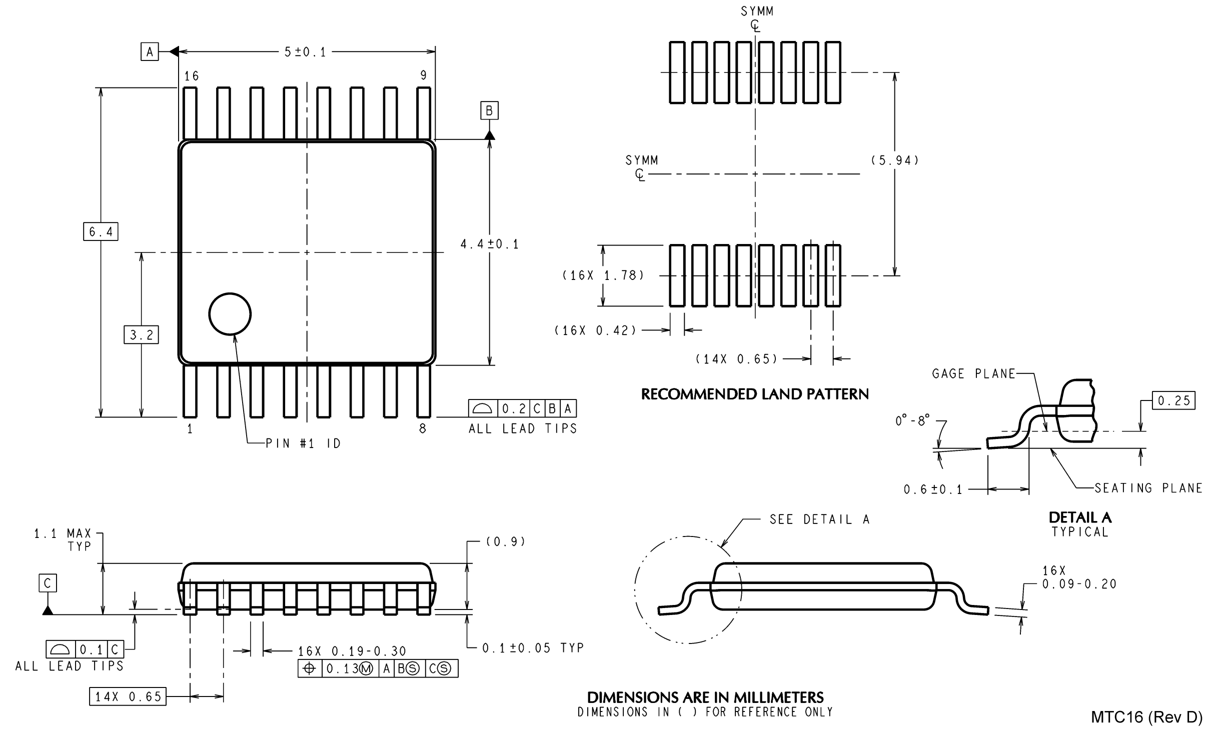
Typical PC Board Layout: (2X Size) (Continued)



10128428

Solder Side PC Board Layout

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead TSSOP (MTC)
NS Package Number MTC16
Order Number LM2655MTC-ADJ
LM2655MTCX-ADJ
LM2655MTC-3.3
LM2655MTCX-3.3
See Ordering Information Table For Order Quantities

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265