LM2725/LM2726 High Speed Synchronous MOSFET Drivers

Check for Samples: LM2725, LM2726

FEATURES

- **High Peak Output Current**
- **Adaptive Shoot-Through Protection**
- **36V SW Pin Absolute Maximum Voltage**
- **Input Under-Voltage-Lock-Out**
- **Typical 20ns Internal Delay**
- **Plastic 8-pin SOIC Package**

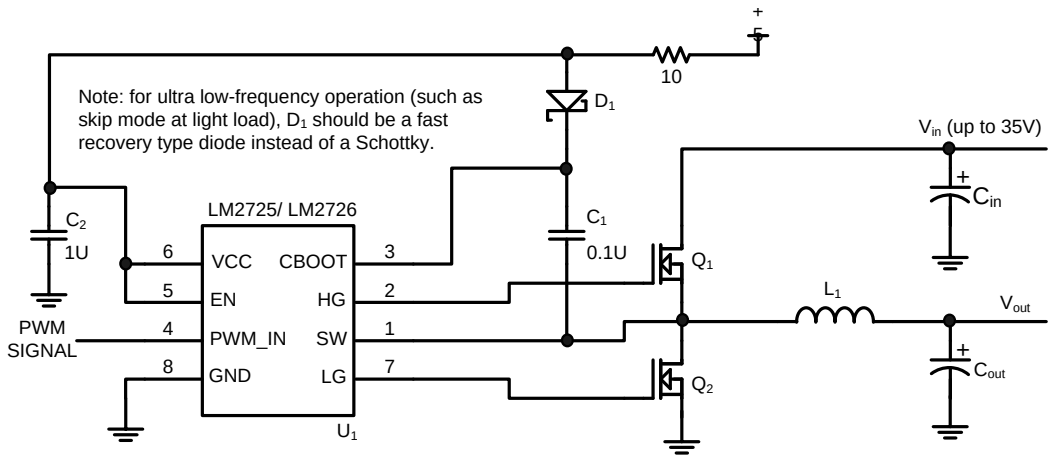
APPLICATIONS

- **High Current DC/DC Power Supplies**
- **High Input Voltage Switching Regulators**
- **Microprocessors**

DESCRIPTION

The LM2725/LM2726 is a family of dual MOSFET drivers that drive both the top MOSFET and bottom MOSFET in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in shoot-through protection circuitry prevents the top and bottom FETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2725 is about 1.2A and that of the LM2726 is about 3A. In an SOIC-8 package, each driver is able to handle 50mA average current. When EN signal is asserted the input UVLO (Under Voltage Lock Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. The top gate bias voltage needed by the top MOSFET can be obtained through an external bootstrap structure. Minimum input pulse width is as low as 55ns.

Typical Application



Connection Diagram

8-Lead Small Outline Package

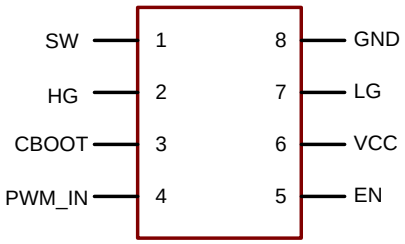
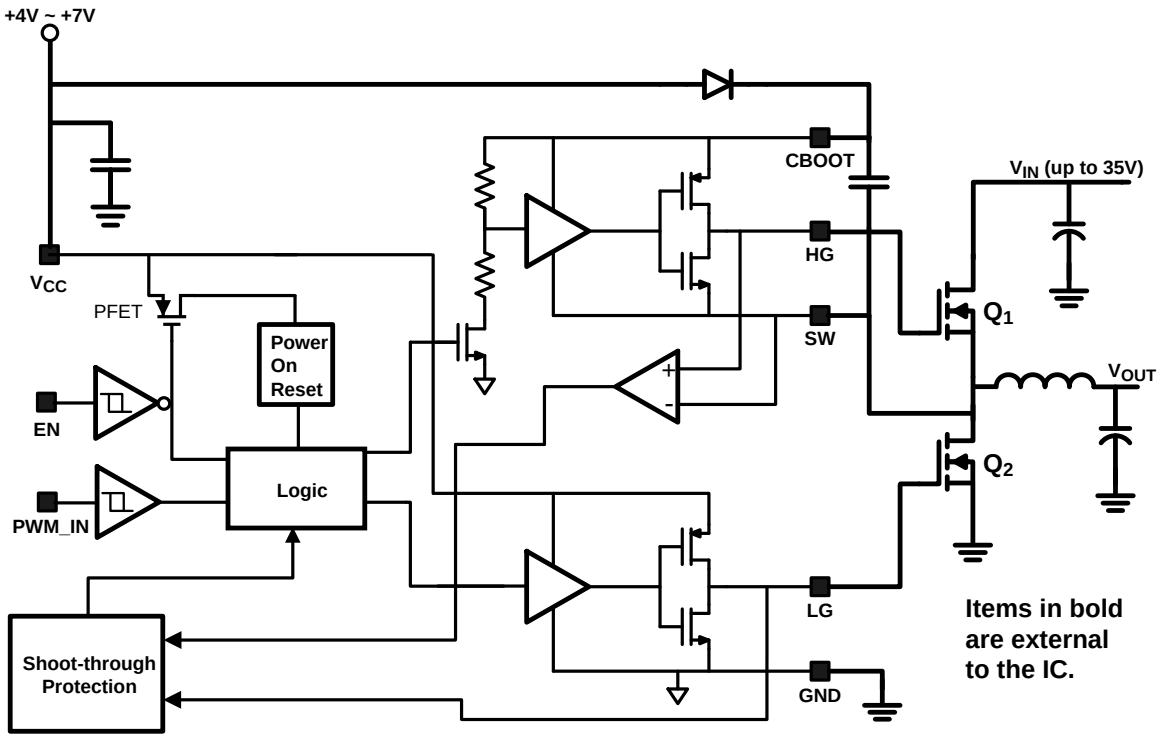


Figure 1. Top View

PIN DESCRIPTIONS

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs.
2	HG	Top gate drive output.
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver.
4	PWM_IN	Accepts a 5V-logic control signal.
5	EN	Chip Enable. Active HIGH. Must be asserted during power up and down.
6	VCC	Connect to +5V supply.
7	LG	Bottom gate drive output.
8	GND	Ground.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

ORDER NUMBER	PACKAGE TYPE	STATUS
LM2726M	SOIC	NRND
LM2726M/NOPB		NRND

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Absolute Maximum Ratings (1)(2)

VCC	7.5V
CBOOT	42V
CBOOT to SW	8V
SW to PGND	36V
Junction Temperature	+150°C
Power Dissipation (3)	720mW
Storage Temperature	−65° to 150°C
ESD Susceptibility Human Body Model (4)	1 kV
Soldering Time, Temperature	10sec., 300°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The gaurnteed specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for LM2725/LM2726 is 172°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 0.7W.
(4) ESD machine model susceptibility is 100V.

Operating Ratings (1)

VCC	4V to 7V
Junction Temperature Range	0° to 125°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The gaurnteed specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.

Electrical Characteristics
LM2725

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		180	**250**	µA
I_{q_sd}	Shutdown Quiescent Current	EN = 0V, PWM_IN = 0V		0.5	**15**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		1.2		A
	Pull-Up Rds_on	I_{CBOOT} = I_{HG} = 0.7A		2.4		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−1.0		A
	Pull-down Rds_on	I_{SW} = I_{HG} = 0.7A		1.4		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			10		ns
t_3	Pull-Up Dead Time	Timing Diagram		23		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN Falling Edge		21		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		1.2		A
	Pull-up Rds_on	I_{VCC} = I_{LG} = 0.7A		2.6		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		−2		A
	Pull-down Rds_on	I_{GND} = I_{LG} = 0.7A		0.65		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		18		ns
t_2	Fall Time			6		ns
t_7	Pull-up Dead Time	Timing Diagram		28		ns
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		15		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V		3.0		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			2.5		V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.5		V
V_{IH_EN}	EN Pin High Input		**2.4**			V
V_{IL_EN}	EN Pin Low Input				**0.8**	V
I_{leak_EN}	EN Pin Leakage Current	EN = VCC = 5V	**−2**		**2**	µA
		VCC = 5V, EN = 0V	**−2**		**2**	
t_{on_min}	Minimum Positive Input Pulse Width (1)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (2)			55		

(1) If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.
(2) If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Electrical Characteristics LM2725 (continued)

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.8**	

Electrical Characteristics LM2726

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		185	**250**	µA
I_{q_sd}	Shutdown Quiescent Current	EN = 0V, PWM_IN = 0V		0.5	**15**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		3.0		A
	Pull-Up Rds_on	I_{CBOOT} = I_{HG} = 1.0A		1.2		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	I_{SW} = I_{HG} = 1.0A		0.5		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			12		ns
t_3	Pull-Up Dead Time	Timing Diagram		19		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN from Falling Edge		27		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-up Rds_on	I_{VCC} = I_{LG} = 1.0A		1.1		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	I_{GND} = I_{LG} = 1.0A		0.6		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time			14		ns
t_7	Pull-up Dead Time	Timing Diagram		12		ns
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		13		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V		2.8		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			2.5		V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.3		V
V_{IH_EN}	EN Pin High Input		**2.4**			V
V_{IL_EN}	EN Pin Low Input				**0.25**	V
I_{leak_EN}	EN Pin Leakage Current	EN = VCC = 5V	**−2**		**2**	µA
		VCC = 5V, EN = 0V	**−2**		**2**	

Electrical Characteristics
LM2726 (continued)

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{on_min}	Minimum Positive Input Pulse Width (1)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (2)			55		
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.25**	

(1) If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.
(2) If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

TEST CIRCUIT DIAGRAMS

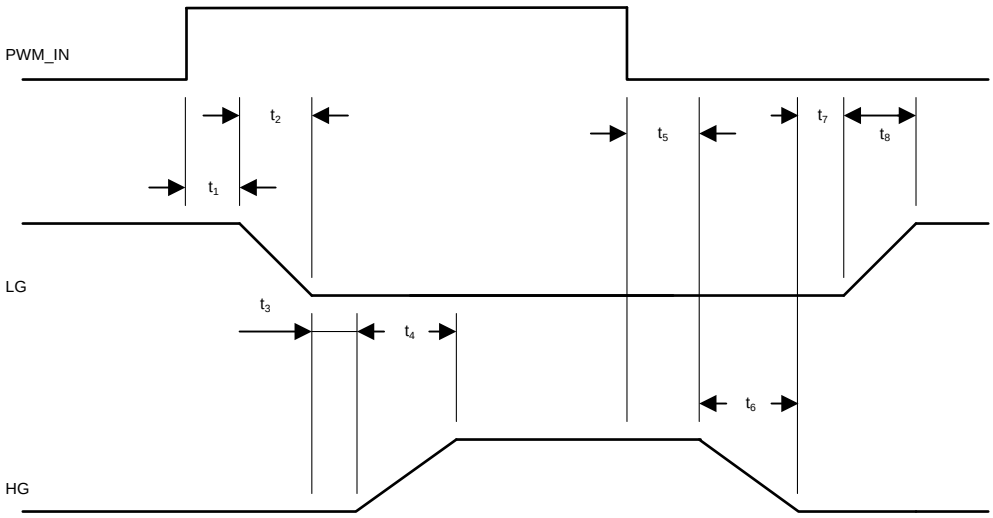


Figure 2. Timing Diagram

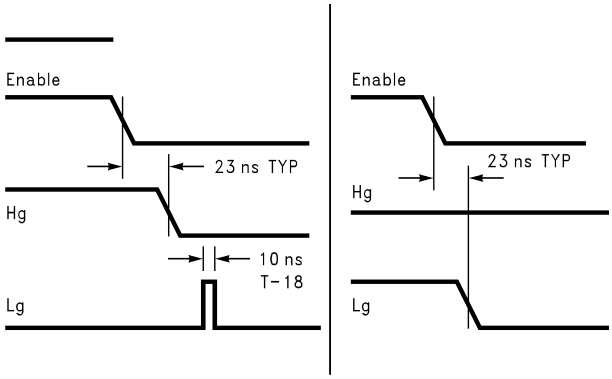


Figure 3. Enable Pin Shutdown

Test Circuits

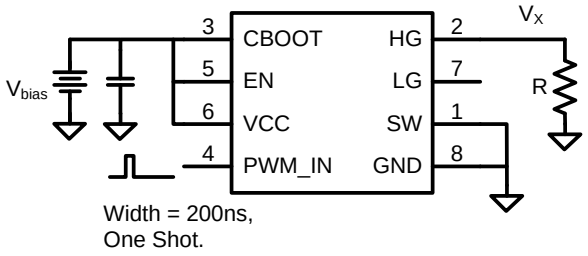


Figure 4. Test Circuit 1

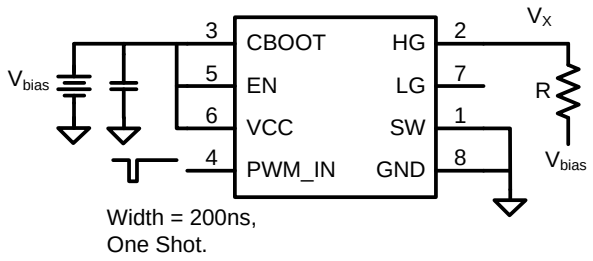


Figure 5. Test Circuit 2

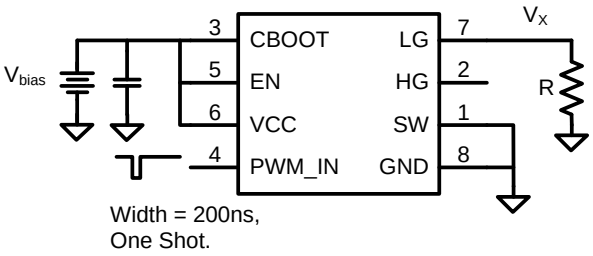


Figure 6. Test Circuit 3

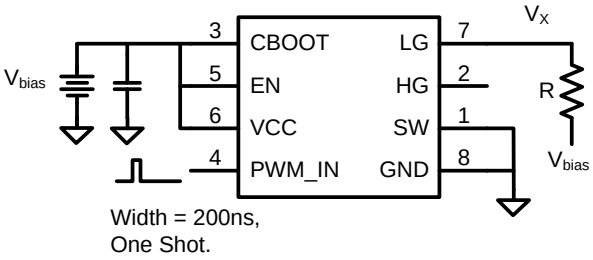


Figure 7. Test Circuit 4

$$I_{pull\_up} = \frac{V_x}{R} \quad (1)$$

$$I_{pull\_down} = \frac{V_{bias} - V_x}{R} \quad (2)$$

$$R_{ds\_pull\_up} = \frac{V_{bias} - V_x}{V_x} \cdot R \quad (3)$$

$$R_{ds\_pull\_down} = \frac{V_x}{V_{bias} - V_x} \cdot R \quad (4)$$

Typical Waveforms

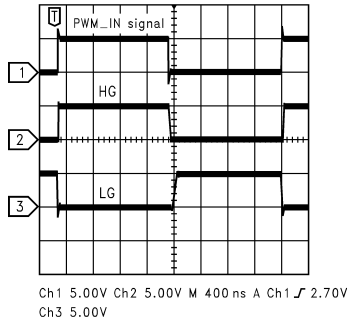


Figure 8. Switching Waveforms of Test Circuit

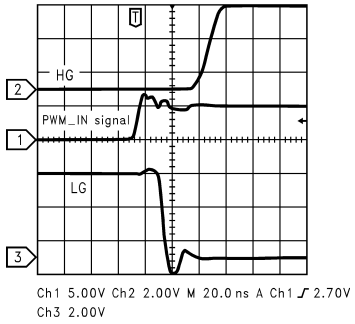


Figure 9. When Input Goes High

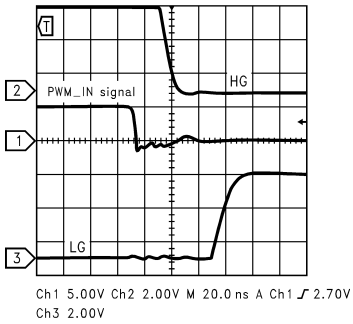


Figure 10. When Input Goes Low

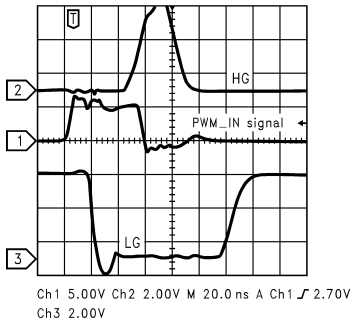


Figure 11. Minimum Positive Pulse

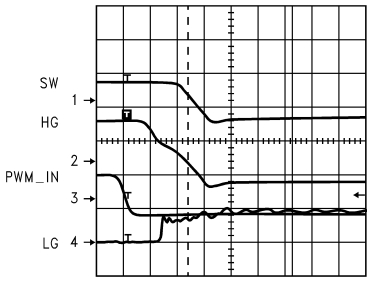


Figure 12. Turn-Off

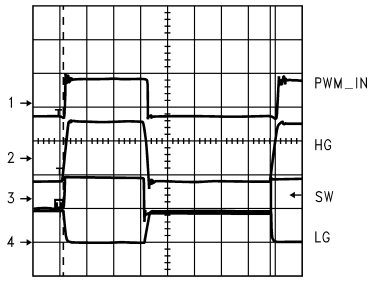


Figure 13. Normal Operation at 250kHz

Functional Description

The LM2725/2726 drivers were designed to be used in systems supporting low-power states, such as notebook computers' Suspend-To-RAM (STR), etc. A typical application scenario would be powering up and powering down the driver while having EN asserted, i.e. at logic high level. During a low-power state of the whole system when the load is not powered, the EN input can be pulled to logic low level to shutdown the driver thus reducing its power.

The EN pin functions as a "Chip Enable." When it is asserted high, the chip is fully powered on and fully functional. When the EN pin is low, the power is disconnected from the internal POR (Power-On-Reset) and the bandgap reference blocks by a P-FET. This is done to lower the quiescent current Iq from 180µA typical in normal operation to 0.5µA typical in shutdown mode. The HG and LG drivers are still powered to maintain the external NFETs.

The POR circuit also performs the UVLO (Under Voltage Lockout) function and, therefore, the POR must be powered on during the driver powering up and down. This means that the EN pin must be allowed to transition high or low with the VCC rail. Having the EN pin low during startup prevents the POR circuit from biasing up, which can potentially cause an unpredicted state in the HG output.

The HG high-side driver circuit includes a latch. A signal from the POR block resets the latch, turning HG output off. Without the POR signal, this latch may be indeterminate in its initial state upon powering up. The slew rate of CB-SW voltage may affect the latch's initial state, as well as normal leakage paths through the transistors controlling the latch.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2726MX/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		2726 M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

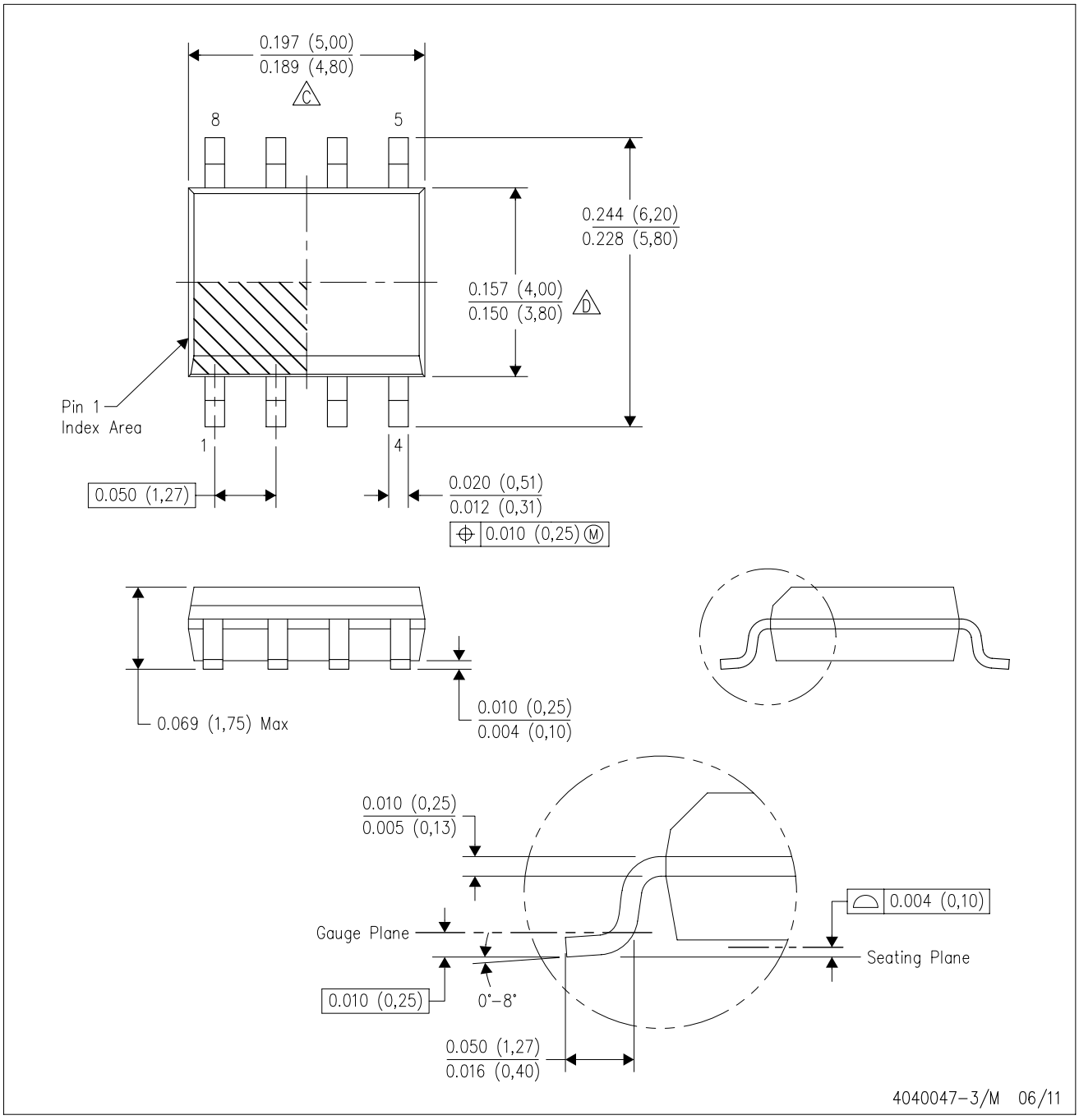
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265