

LM2753 High-Power Switched-Capacitor Voltage Converter and Flash LED Driver

1 Features

- Input Voltage Range: 3 V to 5.5 V
- Regulated 5-V Output
- 250-mA Output Current With a 3.6-V Input
- 400-mA Pulsed Output Current (up to 500-ms Duration)
- 60- μ A (Typical) Quiescent Current
- Pulse-Frequency Modulation (PFM) Regulation
- Inductor-Less Solution: Requires Only Three Small Capacitors
- < 1- μ A Typical Shutdown Current
- 10-pin WSON Package (No Pullback):
 - 3 mm \times 3 mm \times 0.8 mm

2 Applications

- Cell-Phone Camera Flash
- Digital Still Cameras
- Fire-Alarm Notification
- Emergency Strobe Lighting
- Intruder Alert Notification
- Barcode Scanners
- Handheld Data Terminals
- General-Purpose Regulated Voltage Output, High-Current Supply

3 Description

The LM2753 is capable of driving a flash LED with a pulsed current of 400 mA at an input voltage of 3.6 V. A switched-capacitor doubler, the LM2753 provides a regulated 5-V output (V_{OUT}) over an input supply range of 3 V to 5.5 V. The switched output, I_{OUT} , takes less than 10 ns to turn on and provide maximum current to a flash LED. Flash LED current is set via a ballast resistor. Continuous illumination current (torch mode) is programmed by connecting a resistor between I_{OUT} and V_{OUT} . This device uses only three small, low-cost ceramic capacitors.

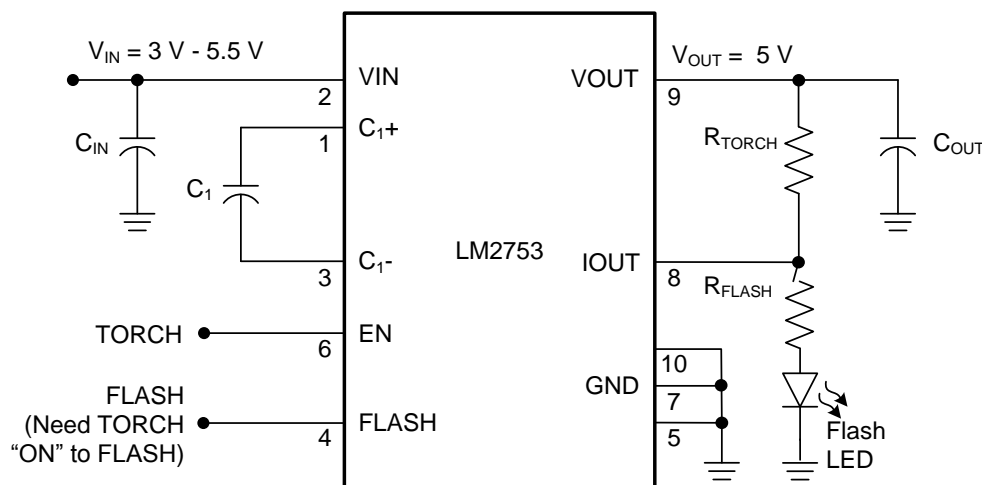
The LM2753 device uses pulse frequency modulation (PFM) regulation. Typical operating frequency is 725 kHz. Under no-load conditions, the LM2753 operates on only 60 μ A. If the output is connected to ground, the charge pump stays in the gain of 1, which helps limit the input current to 300 mA (typical).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2753	WSON (10)	3.00 mm \times 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

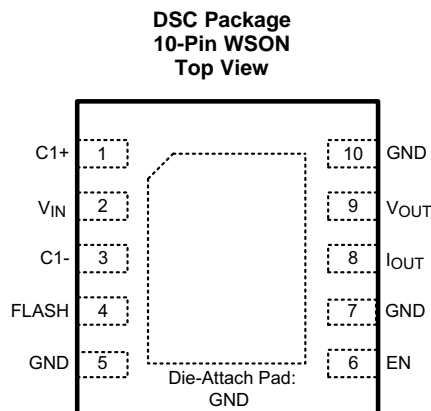
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2016) to Revision F	Page
• Added several <i>Applications</i>	1

Changes from Revision D (May 2013) to Revision E	Page
• Added <i>Device Information</i> and <i>Pin Configuration and Functions</i> sections, <i>ESD Ratings</i> , <i>Feature Description</i> , <i>Device Functional Modes</i> , <i>Application and Implementation</i> , <i>Power Supply Recommendations</i> , <i>Layout</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections	1
• Changed $R_{\theta JA}$ from "55°C/W" to "52.5°C/W"; add additional thermal values	4

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Semiconductor data Sheet to TI format.....	11

5 Pin Configuration and Functions



Pin Descriptions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	C ₁₊	O	Flying capacitor connection
2	V _{IN}	I	Input voltage connection. Input voltage range: 3 V to 5.5 V
3	C ₁₋	O	Flying capacitor connection
4	FLASH	I	Flash logic input pin. Logic HIGH = flash output on, logic low = flash output off. there is an internal pulldown of 300 kΩ between FLASH and GND.
5	GND	—	Connect to ground
6	EN	I	Enable pin. Logic HIGH = enable, Logic LOW = shutdown. There is an internal pulldown of 300 kΩ between EN and GND
7	GND	—	Connect to ground
8	IOUT	O	Flash output. ON/OFF control via FLASH pin
9	VOUT	O	5-V regulated output
10	GND	—	Connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
V _{IN} pin: voltage to GND	-0.3	6	V
EN, FLASH pins: voltage to GND	-0.3	(V _{IN} + 0.3) w/ 6 V maximum	V
Continuous power dissipation ⁽³⁾	Internally limited		
Junction temperature, T _{J-MAX-ABS}		150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 120°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}).

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Machine model	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage	3	5.5	V
EN, FLASH input voltage	0	V _{IN}	V
Junction temperature, T _J	-40	120	°C
Ambient temperature, T _A ⁽²⁾	-40	85	°C

- (1) All voltages are with respect to the potential at the GND pin.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 120°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM2753	UNIT
		DSC (WSON)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	52.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	63.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	27.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	27.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	7.3	°C/W

- (1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Unless otherwise noted, specifications apply to the *Simplified Schematic* with $T_A = 25^\circ\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{(EN)} = V_{IN}$, $V_{(FLASH)} = \text{GND}$, $C_1 = 1\ \mu\text{F}$, $C_{IN} = C_{OUT} = 10\ \mu\text{F}$.^{(1) (2)}

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} Output voltage	$3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} \leq 100\text{ mA}$		5		V
	$3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} \leq 100\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	4.75 (-5%)		5.25 (5%)	
I_{VOUT} Continuous load current	$3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $V_{OUT} = 5\text{ V}$ (typical)		200		mA
I_{OUT} Pulsed flash current	$V_{(FLASH)} = 1.8\text{ V}$, $T_{PULSE} = 500\text{ ms}$ $V_{IOUT-MAX} = 4.1\text{ V}$ (typical)		400		mA
I_Q Quiescent current	$I_{OUT} = 0\text{ mA}$, $3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		60		μA
	$I_{OUT} = 0\text{ mA}$, $3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$			80	
I_{SD} Shutdown supply current	$V_{(EN)} = 0\text{ V}$ $3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.1	1	μA
	$V_{(EN)} = 0\text{ V}$, $3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ $T_A = 85^\circ\text{C}$		0.2		
R_{OUT} Output impedance	$V_{IN} = 3.2\text{ V}$		5.3		Ω
f_{SW} Switching frequency	$3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		725		kHz
	$3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	475		950	
V_{IH} Logic input high	Input pins: EN, FLASH, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	1.2		V_{IN}	V
V_{IL} Logic input low	Input pins: EN, FLASH, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0		0.3	V
I_{IH} Logic input high current	$V_{(EN)} = V_{(FLASH)} = 3\text{ V}$		10		μA
I_{IL} Logic input low current	$V_{(EN)} = V_{(FLASH)} = 0\text{ V}$		10		nA
t_{ON} Turnon time ⁽³⁾			640		μs
t_{FLASH} Flash turnon time ⁽⁴⁾	$V_{(FLASH)} = 3.6\text{ V}$		10		ns

- (1) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not specified, but represent the most likely norm.
- (2) C_{IN} , C_{OUT} , and C_1 : Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
- (3) Turnon time is measured from when the EN signal is pulled high until the output voltage on V_{OUT} crosses 90% of its final value.
- (4) Flash turnon time is measured from when the FLASH signal is pulled high until the voltage on I_{OUT} crosses 90% of its final programmed value.

6.6 Typical Characteristics

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{(FLASH)} = \text{GND}$, $V_{(EN)} = V_{IN}$, $C_{IN} = C_{OUT} = 10\ \mu\text{F}$, $C_1 = 1\ \mu\text{F}$.

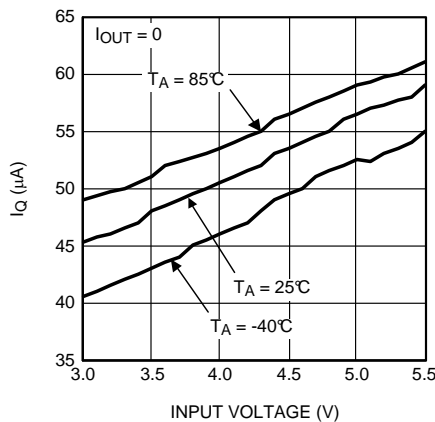


Figure 1. Quiescent Current vs Input Voltage

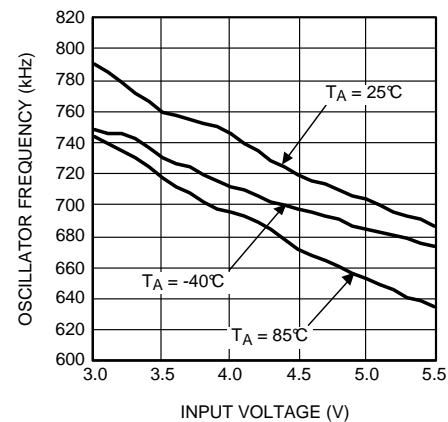


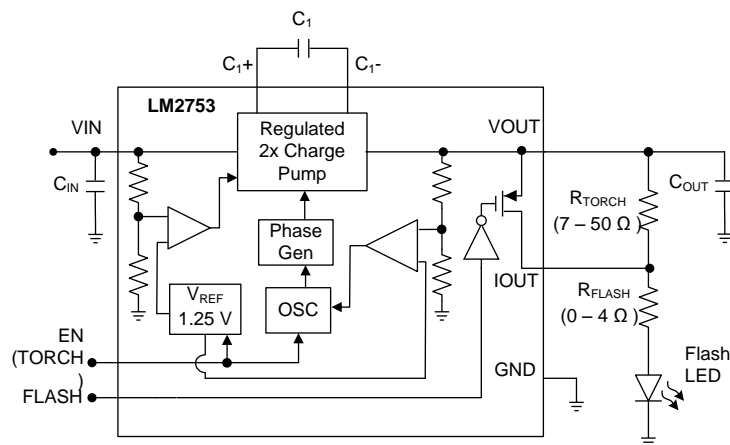
Figure 2. Oscillator Frequency vs Input Voltage

7 Detailed Description

7.1 Overview

The LM2753 is a switched-capacitor doubler with a regulated 5-V output. It is capable of continuously supplying up to 200 mA at 5 V to a load connected to V_{OUT} . This device uses pulse frequency modulation (PWM) and a multi-level switch array to regulate and maintain the output voltage. For higher load currents, such as during flash operation, the output voltage is allowed to droop to supply the necessary current. Although there is no current limit on this device, the device automatically defaults to a gain of 1 when the output is brought below the input voltage. This configuration limits the input current to about 300 mA (typical). The operating range for the LM2753 is over the extended Li-Ion battery range from 2.7 V to 5.5 V.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Soft Start

Soft start is engaged when the device is taken out of shutdown mode ($EN = \text{logic HIGH}$) or when voltage is supplied simultaneously to the V_{IN} and EN pins. During soft start, the voltage on V_{OUT} ramps up in proportion to the rate that the reference voltage is being ramped up. The output voltage is programmed to rise from 0 V to 5 V in 640 μs (typical).

7.3.2 Flash LED Selection

The LM2753 provides a 5-V (typical) fixed voltage to drive a flash LED with a continuous current up to 200 mA (typical). At LED currents above 200 mA (typical), the output of the device is allowed to droop to deliver the desired current to the flash LED. This droop limits the maximum forward voltage and in turn the maximum current that can be supplied to a given LED. Choose LEDs so that the LED forward voltage at the desired maximum LED current does not exceed the output voltage of the LM2753 when loaded down with that same current. TI suggests that the selected LEDs be binned due to the relatively high forward voltage tolerance of flash LEDs. The typical and maximum diode forward voltage depends highly on the manufacturer and their technology. [Table 1](#) lists several suggested manufacturers.

Feature Description (continued)

Table 1. Flash LED Selection

MANUFACTURER	CONTACT
Agilent	www.agilent.com/semiconductors
Citizen	www.c-e.co.jp/e/
Lumileds	www.lumileds.com
Nichia	www.nichia.com
Osram	www.osram-os.com
Panasonic	www.panasonic.co.jp/semicon/
Seoul Semiconductor	en.seoulsemicon.co.kr

7.3.3 PFM Regulation

The LM2753 achieves its tightly regulated output voltage with pulse-frequency modulated (PFM) regulation. PFM simply means the part only pumps when charge must be delivered to the output in order to keep the output voltage in regulation. When the output voltage is above the target regulation voltage the part idles, consuming minimal supply current with C_1 is connected between V_{IN} and GND and V_{IN} is disconnected from V_{OUT} . In this state, the load current is supplied solely by the charge stored on the output capacitor. As this capacitor discharges and the output voltage falls below the target regulation voltage, the charge pump activates, and charge is delivered to the output. This charge supplies the load current and boosts the voltage on the output capacitor.

The primary benefit of PFM regulation is when output currents are light and the device is predominantly in the low-supply-current idle state. Net supply current is minimal because the part only occasionally needs to recharge the output capacitor by activating the charge pump. With PFM regulation, input and output ripple frequencies vary significantly and are dependent on output current, input voltage, and to a lesser degree, other factors such as temperature, internal switch characteristics, and capacitor characteristics (voltage tolerance, temperature variation).

7.3.4 Output Voltage Ripple

The voltage ripple on the output of the LM2753 is highly dependent on the application conditions. The output capacitance, input voltage, and output current each play a significant part in determining the output voltage ripple. Due to the complexity of the LM2753 operation, providing equations or models to approximate the magnitude of the ripple cannot be easily accomplished. However, the following general statements can be made.

The output capacitor has a significant effect on output voltage ripple magnitude. Ripple magnitude is typically linearly proportional to the output capacitance present. The equivalent series resistance (ESR) of the output capacitor also contributes to the output voltage ripple, as there is effectively an AC-voltage drop across the ESR due to current switching in and out of the capacitor. To keep the voltage ripple small, TI recommends a low-ESR ceramic capacitor on the output. Placing multiple capacitors in parallel can reduce ripple significantly, by both increasing capacitance and reducing ESR. When capacitors are in parallel the ESR of the capacitors are in parallel as well, resulting in a net ESR according to the properties of parallel resistance. Two identical capacitors in parallel have twice the capacitance and half the ESR as compared to a single capacitor if the same type. On a similar note, if a large-value, high-ESR capacitor (tantalum, for example) is to be used as the primary output capacitor, the net ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with this primary output capacitor.

7.3.5 IOOUT Pin

An internal FET is connected between the VOUT pin and the IOOUT pin of the LM2753 device. When a logic high signal is placed on the FLASH input pin, the internal FET turns on and connects I_{OUT} to V_{OUT} in less than 10 ns (typical). If the IOOUT pin is not going to be used, the FLASH input pin can be tied to GND, and the IOOUT pin can be left unconnected.

In the typical application circuit there is one resistor between VOUT and IOOUT and another resistor between IOOUT and the flash LED. When a LOW logic signal is placed on the FLASH input pin, the internal FET opens and current flows from V_{OUT} through both resistors and through the flash LED. When a logic HIGH signal is applied to the Flash input pin the internal FET closes, shorting out the resistor between VOUT and IOOUT, and current flows through the second resistor and the Flash LED.

Follow these steps to set the desired current levels for the flash LED:

7.3.5.1 Setting Flash Current

1. Determine the forward voltage of the LED at the desired flash current.
2. Find the voltage difference between I_{OUT} and the LED forward voltage.
3. Divide the voltage difference by the desired flash current to obtain the needed flash LED ballast resistance

7.3.5.2 Setting Torch Current

1. First determine required flash ballast.
2. Determine the forward voltage of the LED at the desired continuous torch current.
3. Find the voltage difference between V_{OUT} and the LED forward voltage.
4. Divide the voltage difference by the desired torch current to obtain the total resistance needed.
5. Subtract the flash ballast resistance from this total resistance to find the required torch resistance between V_{OUT} and I_{OUT}
6. Find the voltage difference between I_{OUT} and the LED forward voltage.
7. Divide the voltage difference by the desired flash current to obtain the needed flash LED ballast resistance

7.3.6 PWM Brightness Control Procedures

The brightness of a flash LED connected to V_{OUT} can be linearly varied from zero up to the maximum programmed current level by applying a PWM signal to the EN pin of the LM2753 device. The following procedures describe how to program the LED drive current and adjust the output current level using a PWM signal.

1. To select the maximum desired current level, refer to the [IOUT Pin](#) section and follow the steps detailed in [Setting Flash Current](#) and [Setting Torch Current](#).
2. Brightness control for torch mode can be implemented by pulsing a signal at the EN pin, while flash is connected to a logic LOW signal. Also, brightness control can also be implemented for flash mode by pulsing a signal on the FLASH pin while the part is already enabled (EN = logic HIGH). LED brightness is proportional to the duty cycle (D) of the PWM signal. For linear brightness control over the full duty cycle adjustment range, the PWM frequency (f) should be limited during torch mode to accommodate the turn-on time ($T_{ON} = 640 \mu s$) of the device. Also, the PWM frequency must be limited during flash mode to accommodate the turnon time ($T_{FLASH} = 10 ns$) of the I_{OUT} output FET.

$$D \times (1/f) > T_{ON,FLASH}$$

$$f_{MAX} = D_{MIN} \div T_{ON,FLASH}$$

If the PWM frequency is much less than 100 Hz, flicker may be seen in the LEDs. For the LM2753, zero duty cycle turns off the LED and a 50% duty cycle results in an average I_{OUT} being half of the programmed LED current. For example, if the output is programmed for a maximum of 100 mA through the flash LED, a 50% duty cycle results in an average I_{LED} of 50 mA.

7.3.7 Multi-Level Switch Array

In order to supply high load currents across the entire V_{IN} operating range, especially at lower V_{IN} , switches in the charge pump are normally designed to have low ON resistance. However, at high input voltages and low load currents, this low resistance results in high output voltage ripple due to the output capacitor being charged too quickly. To solve this problem, while still being able to deliver the needed output current, the LM2753 has a switch array with multiple switches connected in parallel.

The number of switches used in parallel depends on the input voltage applied to the LM2753. At lower input voltages all paralleled switches are used, and as the input voltage rises, switches are removed from the parallel configuration. The highest switch resistance is achieved as the input voltage reaches the maximum operating voltage, which helps with voltage management.

7.3.8 Thermal Protection

When the junction temperature exceeds 140°C (typical), the LM2753 internal thermal protection circuitry disables the part. This feature protects the device from damage due to excessive power dissipation. The device recovers and operates normally when the junction temperature falls below 125°C (typical). It is important to have good thermal conduction with a proper layout to reduce thermal resistance.

7.3.9 Power Efficiency

Charge-pump efficiency is derived in [Equation 1](#) and [Equation 2](#) (supply current and other losses are neglected for simplicity):

$$I_{IN} = G \times I_{OUT}$$

where

- G represents the charge pump gain (1)

$$E = (V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN}) = V_{OUT} \div (G \times V_{IN})$$

where

- G represents the charge pump gain (2)

Efficiency is at its highest as $G \times V_{IN}$ approaches V_{OUT} . Refer to the efficiency graph in [Typical Characteristics](#) for the detailed efficiency data.

7.4 Device Functional Modes

7.4.1 Enable Mode

The enable logic pin (EN) disables the part and reduces the quiescent current to 0.1 μ A (typical). The LM2753 has an active-high EN pin (LOW = shutdown, HIGH = operating). The LM2753 EN pin can be driven with a low-voltage CMOS logic signal (1.5-V logic, 1.8-V logic, etc.). There is an internal 300-k Ω pulldown resistor between the EN and GND pins of the LM2753.

7.4.2 Flash Mode

The flash logic pin (FLASH) controls the internal FET connected between the VOUT and IOUT pins on the LM2753. The LM2753 has an active-HIGH FLASH pin (LOW = shut down, HIGH = operating). A logic HIGH signal must be present on the EN pin before a logic HIGH signal is placed on the FLASH input pin. The EN and FLASH input pins can be connected together and controlled with the same logic signal. The turnon time for I_{OUT} in this configuration will be limited by the turn-on time of the device. The turn-on time for the internal FET is typically 10 ns when the device is already on (EN signal HIGH, V_{OUT} at 5 V). The LM2753 FLASH pin can be driven with a low-voltage CMOS logic signal (1.5-V logic, 1.8-V logic, etc.). There is an internal 300-k Ω pulldown resistor between the FLASH and GND pins of the LM2753.

8 Application and Implementation

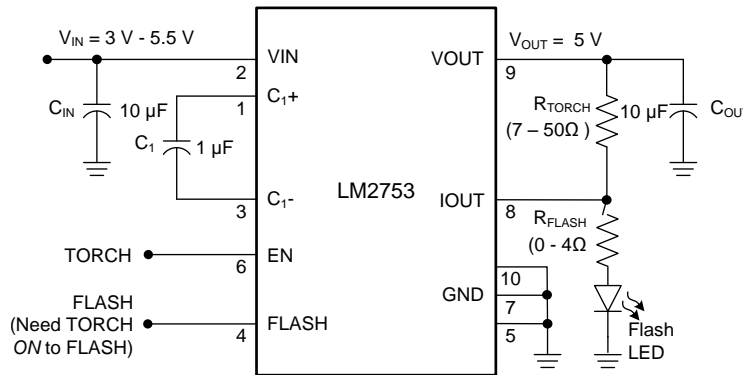
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2753 can be used to drive a flash LED with a pulsed current of up to 400 mA or a continuous current of up to 200 mA over a wide input voltage range. As well as powering flash LEDs, the LM2753 device is suitable for driving other devices with power requirements up to 200 mA. White LEDs can also be connected to this device to back light a cellular phone keypad and display. The LED brightness can be controlled by applying a PWM signal to the enable pin (EN) during torch mode, or to the FLASH pin during flash mode (see [PWM Brightness Control Procedures](#)).

8.2 Typical Application



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Figure 3. LM2753 Typical Application

8.2.1 Design Requirements

For typical switched-capacitor applications, use the parameters listed in [Table 2](#).

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	3 V
Typical output voltage	5 V
Output current	250 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitors

The LM2753 requires three external capacitors for proper operation. TI recommends surface-mount multi-layer ceramic capacitors. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR) ($\leq 15 \text{ m}\Omega$ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are generally not recommended for use with the LM2753 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2753. These capacitors have tight capacitance tolerance (as good as $\pm 10\%$), hold their value over temperature (X7R: $\pm 15\%$ over -55°C to $+125^\circ\text{C}$; X5R: $\pm 15\%$ over -55°C to $+85^\circ\text{C}$), and typically have little voltage coefficient when compared to other types of capacitors. However, selecting a capacitor with a voltage rating much higher than the voltage it will be subjected to ensures that the capacitance stays closer to the nominal value of the capacitor. Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2753. Capacitors with these temperature characteristics typically have wide capacitance tolerance ($+80\%$, -20%), vary significantly over temperature (Y5V: 22% , -82% over -30°C to $+85^\circ\text{C}$ range; Z5U: 22% , -56% over 10°C to 85°C range), and have poor voltage coefficients. Under some conditions, a nominal $1\text{-}\mu\text{F}$ Y5V or Z5U capacitor could have a capacitance of only $0.1 \mu\text{F}$. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2753. [Table 3](#) lists suggested capacitor suppliers for the typical application circuit.

Table 3. Ceramic Capacitor Manufacturers

MANUFACTURER	CONTACT
TDK	www.component.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

8.2.2.2 Power Dissipation

The power dissipation ($P_{\text{DISSIPATION}}$) and junction temperature (T_J) can be approximated with [Equation 3](#) and [Equation 4](#). P_{IN} is the product of the input current and input voltage, P_{OUT} is the power consumed by the load connected to the output, T_A is the ambient temperature, and $R_{\theta\text{JA}}$ is the junction-to-ambient thermal resistance for the 10-pin WSON package.

$$P_{\text{DISSIPATION}} = P_{\text{IN}} - P_{\text{OUT}} = (V_{\text{IN}} \times I_{\text{IN}}) - (V_{\text{VOUT}} \times I_{\text{OUT}})$$

where

- V_{IN} is the input voltage to the LM2753
- V_{VOUT} is the voltage at the output of the device
- I_{OUT} is the total current supplied to the load(s) connected to both V_{OUT} and I_{OUT} (3)

$$T_J = T_A + (P_{\text{DISSIPATION}} \times R_{\theta\text{JA}}) \quad (4)$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM2753 may be operated outside the ambient temperature rating, so long as the junction temperature of the device does not exceed the maximum operating rating of 120°C . The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 120°C .

8.2.3 Application Curves

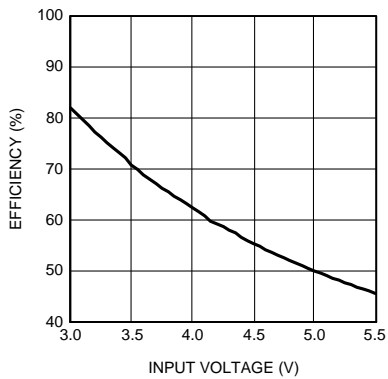
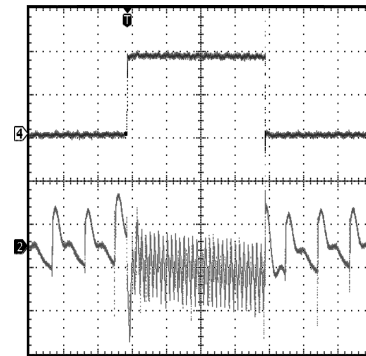
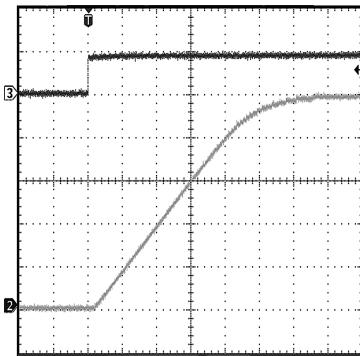


Figure 4. Efficiency vs Input Voltage



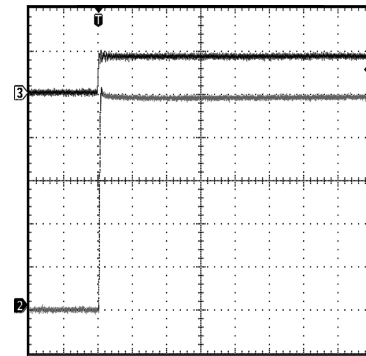
Top: I_{OUT} ; Scale: 100 mA/div
 Bottom: V_{OUT} ; Scale: 50 mV/div, AC Coupled
 Time scale: 40 μ s/div
 Load = 10 mA to 20 mA Step
 $V_{IN} = 3.6$ V

Figure 5. Load Step Response



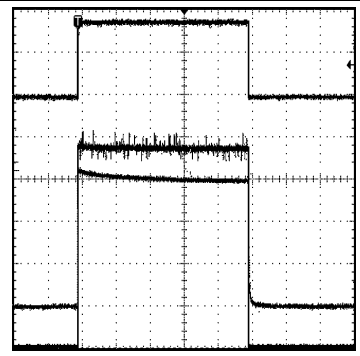
Top: V_{EN} ; Scale: 2V/div
 Bottom: V_{OUT} ; Scale: 1V/div
 Time scale: 1000 μ s/div
 $V_{IN} = 3.6$ V
 Load = 100 mA

Figure 6. Start-Up Behavior



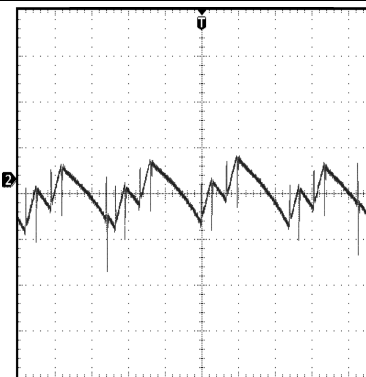
Top: V_{FLASH} ; Scale: 2V/div
 Bottom: V_{IOUT} ; Scale: 1V/div
 Time scale: 400 ns/div
 $V_{IN} = 3.6$ V
 No Load

Figure 7. Flash Enable Behavior



Top: V_{FLASH} ; Scale: 1V/div
 Bottom: V_{IOUT} ; Scale: 1V/div
 Time scale: 100 ms/div
 $V_{IN} = 3.6$ V
 Load = 10 mA to 400 mA Step

Figure 8. Flash Pulse Response



V_{OUT} ; Scale: 50mV/Div, AC Coupled
 Time scale: 2 μ s/div
 $V_{IN} = 3.6$ V
 Load = 200 mA

Figure 9. Output Voltage Ripple

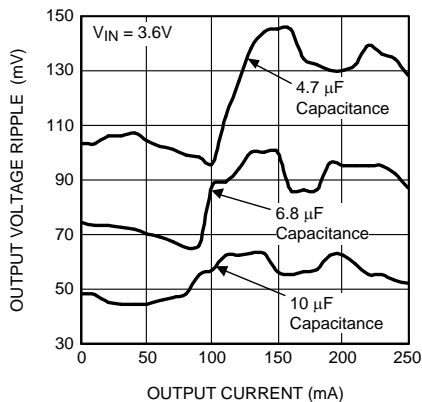
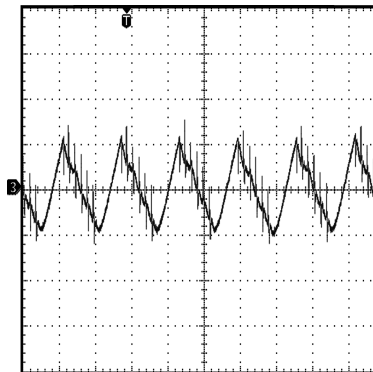


Figure 10. Output Voltage Ripple vs Output Current



V_{IN}: Scale: 50mV/Div, AC Coupled
Time scale: 4 μs/div

V_{IN} = 3.6 V
Load = 200 mA

Figure 11. Input Voltage Ripple

9 Power Supply Recommendations

The LM2753 is designed to operate from an input voltage supply range from 3 V to 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2753 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

Place the output capacitor as close as possible to the output voltage and GND pins.

- VIN input voltage pin must be bypassed to ground with a low-ESR bypass capacitor. Place the capacitor as close as possible to the VIN pin.
- Place the charge pump flying capacitor close to the flying capacitor pins.

10.2 Layout Example

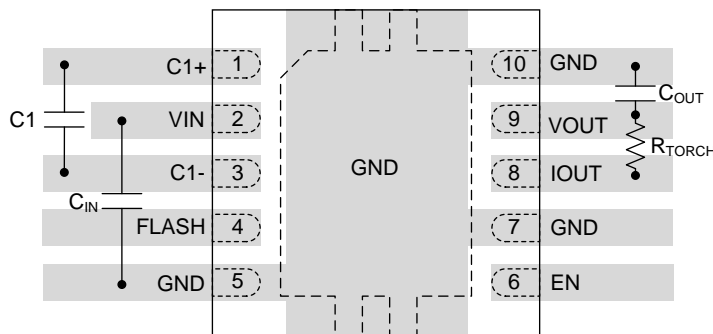


Figure 12. LM2753 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

[AN-1187 Leadless Leadframe Package \(LLP\)](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2753SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D004B	Samples
LM2753SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D004B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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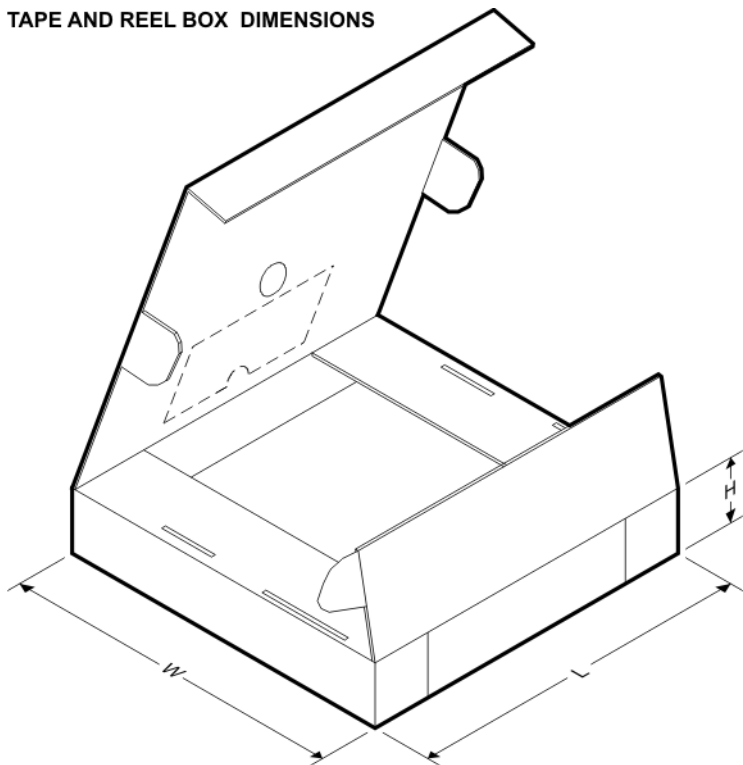
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2753SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2753SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2753SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM2753SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

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