LM3743 High-Performance Synchronous Buck Controller with Comprehensive Fault Protection Features

Check for Samples: LM3743

FEATURES

- **Input Voltage From 3.0V to 5.5V**
- **Output Voltage Adjustable Down to 0.8V**
- **Reference Accuracy: ±1.75%, over Full Temperature and Input Voltage Range**
- **High-Side and Low-Side N-Channel MOSFETs**
- **Switching Frequency Options of 1 MHz or 300 kHz**
- **Comprehensive Fault Protection Features:**
  - **High-Side Current Limit**
  - **Low-Side Current Limit**
  - **Output Under-Voltage Protection**
- **Hiccup Mode Protection Eliminates Thermal Runaway During Fault Conditions**
- **Externally Programmable Soft-Start with Tracking Capability**
- **Pre-Bias Start-Up Capability**
- **VSSOP-10 Package**

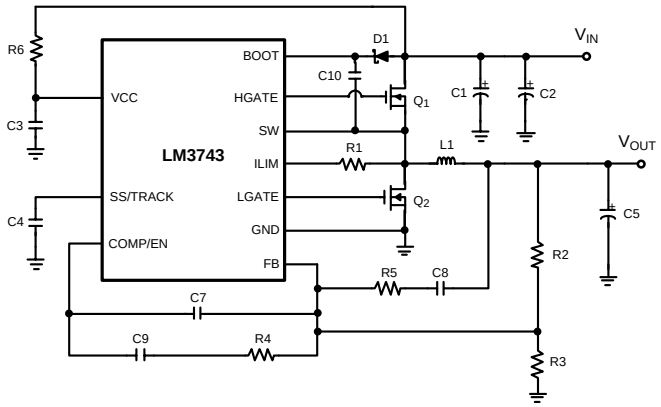
APPLICATIONS

- **Rack-Mount Servers**
- **Telecom Base Stations**
- **Routers**
- **Printers/Scanners**
- **Multi-Media Set-Top Boxes**
- **FPGAs, ASICs, and DSPs**

DESCRIPTION

The LM3743 is a DC-DC voltage mode PWM buck controller featuring synchronous rectification at 300 kHz or 1 MHz. It can deliver current as high as 20A and step down from an input voltage between 3V and 5.5V down to a minimum output voltage of 0.8V, with a ±1.75% internal reference accuracy. The LM3743 provides a set of comprehensive fault protection features such as high-side current limit, output under-voltage protection, and low-side current limit. When any of these fault protection features are engaged, it enters a hiccup protection mode which is suitable for high reliability systems such as rack mounted servers and telecom base station subsystems. The LM3743 also employs a proprietary monolithic glitch free pre-bias start-up method suited for FPGA and ASIC logic devices. An external programmable soft-start allows for tracking and timing flexibility. The driver features 1.6Ω of pull-up resistance and 1Ω of pull-down drive resistance for high power density and very efficient power processing.

Typical Application



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Connection Diagram

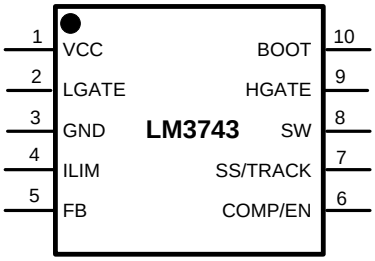

Figure 1. 10-Lead Plastic VSSOP (Top View)
See Package Number DGS

PIN DESCRIPTIONS

VCC (Pin 1)	Supply rail for the controller section of the IC. A minimum capacitance of 1 µF, preferably a multi-layer ceramic capacitor type (MLCC), must be connected as close as possible to the V_{CC} and GND pin and a 1 to 4.99Ω resistance must be connected in series from the supply rail to the Vcc pin. See V_{CC} Filtering in the Design Consideration section for further details.
LGATE (Pin 2)	Gate drive for the low-side N-channel MOSFET. This signal is interlocked with HGATE to avoid a shoot-through problem.
GND (Pin 3)	Power ground (PGND) and signal ground (SGND). Connect the bottom feedback resistor between this pin and the feedback pin.
ILIM (Pin 4)	Low side current limit threshold setting pin. This pin sources a fixed 50 µA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side N-FET.
FB (Pin 5)	Feedback pin. This is the inverting input of the error amplifier used for sensing the output voltage and compensating the control loop.
COMP/EN (Pin 6)	Output of the error amplifier and enable pin. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the control loop. Forcing this pin to ground will shut down the IC.
SS/TRACK (Pin 7)	Soft-start and tracking pin. This pin is connected to the non-inverting input of the error amplifier during initial soft-start, or any time the voltage is below the reference. To track the rising ramp of another power supply's output, connect a resistor divider from the output of that supply to this pin as described in Application Information.
SW (Pin 8)	Switch pin. The lower rail of the high-side N-FET driver. Also used for the high side current limit sensing.
HGATE (Pin 9)	Gate drive for the high-side N-channel MOSFET. This signal is interlocked with LGATE to avoid a shoot-through problem.
BOOT (Pin 10)	Supply rail for the N-channel MOSFET high gate drive. The voltage should be at least one gate threshold above the regulator input voltage to properly turn on the high-side N-FET. See MOSFET GATE DRIVE in the Application Information section for more details on how to select MOSFETs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

V_{CC}		-0.3V to 6V
SW to GND		-0.3V to 6V
Boot to GND		-0.3V to 12V
Boot to SW		-0.3V to 6V
SS/TRACK, ILIM, COMP/EN,FB to GND		-0.3V to V_{CC}
Junction Temperature		150°C
Storage Temperature		−65°C to 150°C
Soldering Information	Lead Temperature (soldering, 10sec)	260°C
	Infrared or Convention (20sec)	235°C
ESD Rating[3]		+ / – 2 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device operates correctly. Operating Ratings do not imply specified performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD using the human body model which is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22–A114.

Operating Ratings

Supply Voltage Range, V_{CC}[1]	3.0V to 5.5V
Junction Temperature Range (T_J)	−40°C to +125°C

(1) Practical lower limit of V_{CC} depends on selection of the external MOSFET. See the MOSFET GATE DRIVE section under Application Information for further details.

Electrical Characteristics

V_{CC} = 3.3V, COMP/EN floating unless otherwise indicated in the conditions column. Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM PARAMETERS						
V_{FB}	FB pin voltage in regulation	3.0V ≤ V_{CC} ≤ 5.5V	**0.786**	0.8	**0.814**	V
V_{UVLO}	UVLO thresholds	Input voltage rising		2.84	**3.0**	V
		Input voltage falling	**2.45**	2.66		
I_{VCC}	Operating V_{CC} current	f_{SW} = 300 kHz, LM3743-300		1.5	**2.5**	mA
	Operating V_{CC} current	f_{SW} = 1 MHz, LM3743-1000		1.8	**3.0**	mA
	Shutdown V_{CC} current	COMP/EN = 0V		6	**50**	µA
$I_{SS/TRACK}$	SS/TRACK pin source current	$V_{SS/TRACK}$ = 0V	**8**	10.2	**12.5**	µA
I_{ILIM}	ILIM pin source current	V_{ILIM} = 0V	**42.5**	50	**57.5**	µA
V_{ILIM}	Current Limit Trip Level		**–25**	0	**25**	mV
$I_{COMP/EN}$	COMP/EN pin pull-up current	$V_{COMP/EN}$ = 0V		4		µA
$V_{HS-CLIM}$	High-side current limit threshold	Measured at V_{CC} pin with respect to SW		500		mV
ERROR AMPLIFER						
GBW	Error Amplifier Unity Gain Bandwidth			30		MHz
G	Error Amplifier DC Gain			90		dB
SR	Error Amplifier Slew Rate	$C_{COMPENSATION}$ = 2.2 nF, I_{EAO} = 1 mA		0.5		V/µs
I_{FB}	FB pin Bias Current			10	**200**	nA
I_{EAO}	EAO pin sourcing/sinking current capability	$V_{COMP/EN}$ = 1.5, V_{FB} = 0.75V		1.7		mA
		$V_{COMP/EN}$ = 1.5, V_{FB} = 0.85V		-1		
GATE DRIVE						
$I_{SHDN-BOOT}$	BOOT Pin Shutdown Current	V_{BOOT}-V_{SW} = 3.3V, $V_{COMP/EN}$ = 0V		25	**50**	µA

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Electrical Characteristics (continued)

V_{CC} = 3.3V, COMP/EN floating unless otherwise indicated in the conditions column. Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{HG-UP}	High Side MOSFET Driver Pull-up ON resistance	V_{BOOT}-V_{SW} = 3.3V, I_{HGATE} = 350mA (sourcing)		1.6		Ω
R_{HG-DN}	High Side MOSFET Driver Pull-down ON resistance	V_{BOOT}-V_{SW} = 3.3V, I_{HGATE} = 350mA (sinking)		1		Ω
R_{LG-UP}	Low Side MOSFET Driver Pull-up ON resistance	V_{CC} = 3.3V, I_{LGATE} = 350mA (sourcing)		1.6		Ω
R_{LG-DN}	Low Side MOSFET Driver Pull-down ON resistance	V_{CC} = 3.3V, I_{LGATE} = 350mA (sinking)		1		Ω
OSCILLATOR						
f_{SW}	Oscillator Frequency	3.0V ≤ V_{CC} ≤ 5.5V, LM3743-300	**255**	300	**345**	kHz
		3.0V ≤ V_{CC} ≤ 5.5V, LM3743-1000	**850**	1000	**1150**	
D_{MAX}	Max Duty Cycle	f_{SW} = 300 kHz, LM3743-300	**85**	91		%
		f_{SW} = 1 MHz, LM3743-1000	**69**	76		
V_{RAMP}	PWM Ramp Amplitude			1.0		V
LOGIC INPUTS AND OUTPUTS						
$V_{COMP/EN-HI}$	COMP/EN pin logic high trip-point			0.65	**0.9**	V
$V_{COMP/EN-LO}$	COMP/EN pin logic low trip-point		**0.1**	0.45		V
HICCUP MODE						
$N_{LSCYCLES}$	Low-side sensing cycles before hiccup mode			15		Cycles
$N_{LSRESET}$	Low-side sensing cycles reset without activating current limit			32		Cycles
V_{UVP}	Under Voltage Protection comparator threshold			400		mV
$t_{GLICH-UVP}$	Under Voltage Protection fault time before hiccup mode			7		µs
t_{HICCUP}	Hiccup timeout			5.5		ms
t_{SS}	Soft-start time coming out of hiccup mode			3.6		ms
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient Thermal Resistance			235		°C/W

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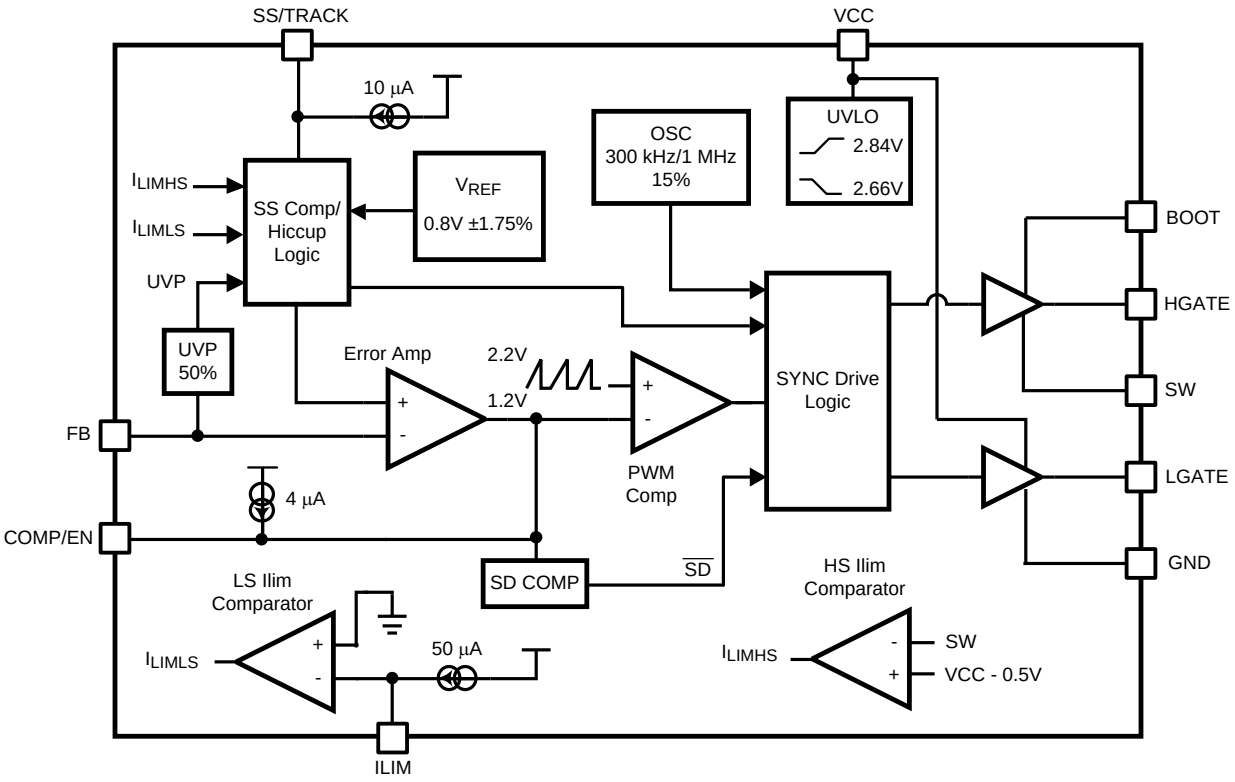
Block Diagram



Typical Performance Characteristics

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

D_{Max} vs Temperature f_{SW} = 1 MHZ

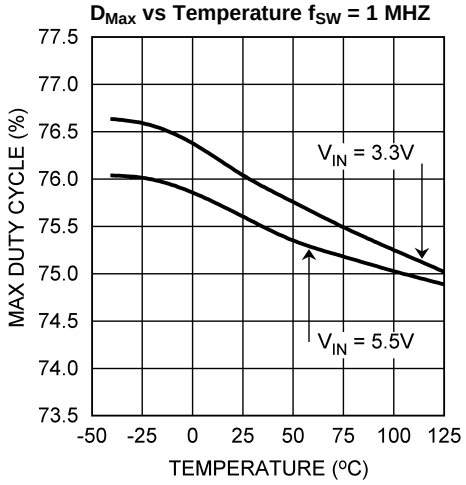


Figure 2.

D_{Max} vs Temperature f_{SW} = 300 kHz

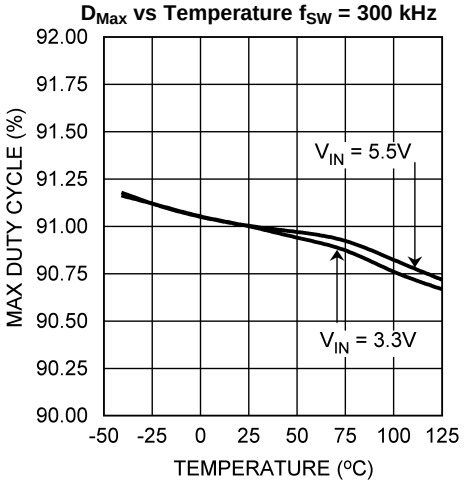


Figure 3.

FB vs Temperature f_{SW} = 1 MHZ

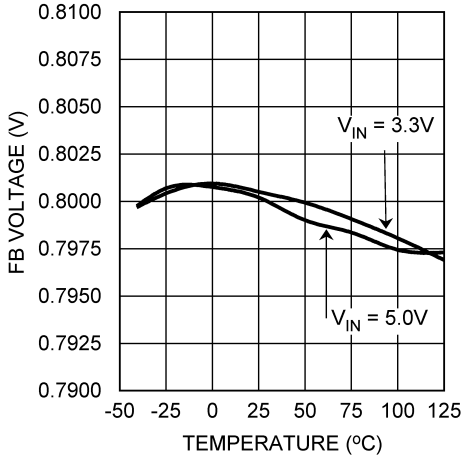


Figure 4.

FB vs Temperature f_{SW} = 300 kHz

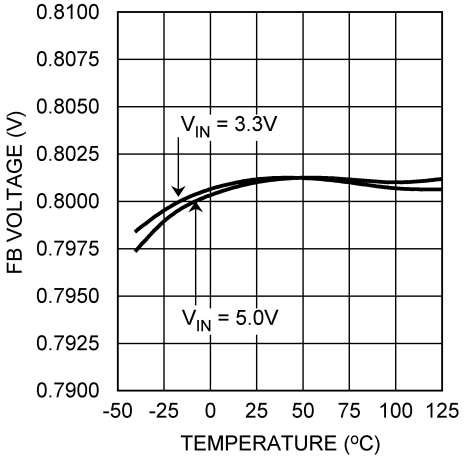


Figure 5.

Frequency vs Temperature f_{SW} = 1 MHz

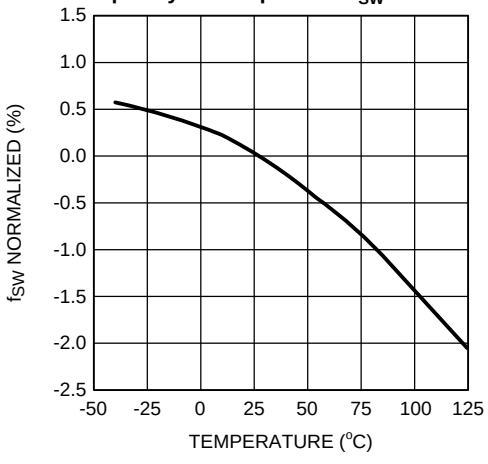


Figure 6.

Frequency vs Temperature f_{SW} = 300 kHz

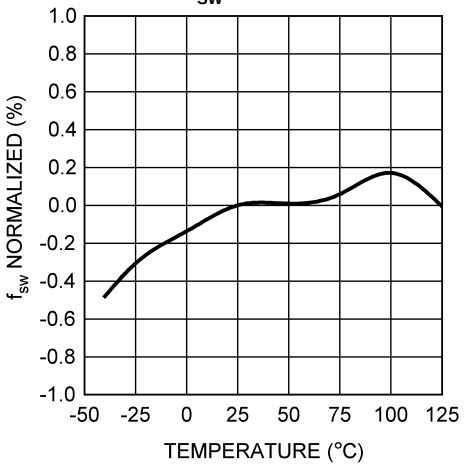


Figure 7.

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Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

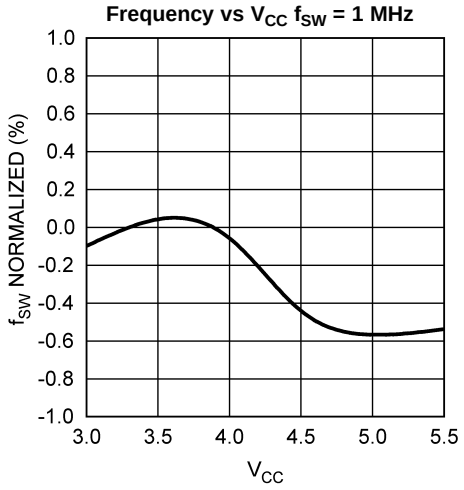

Figure 8.

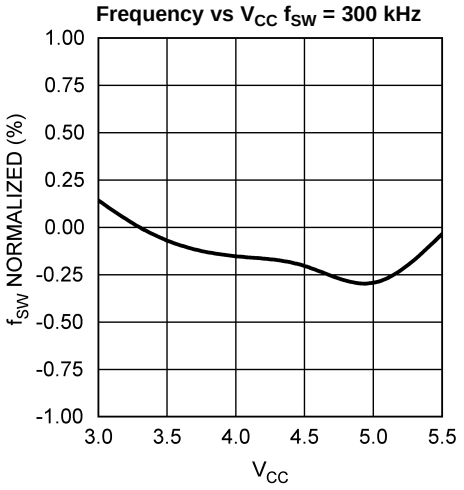

Figure 9.

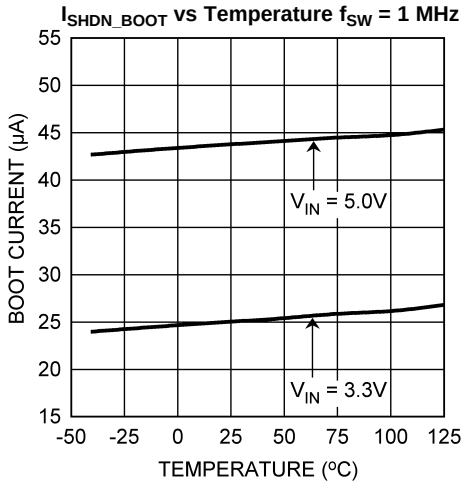

Figure 10.

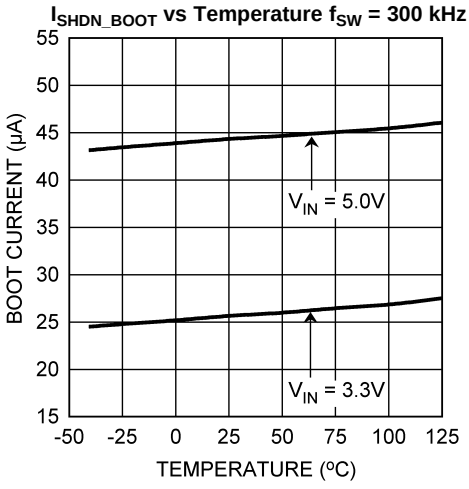

Figure 11.

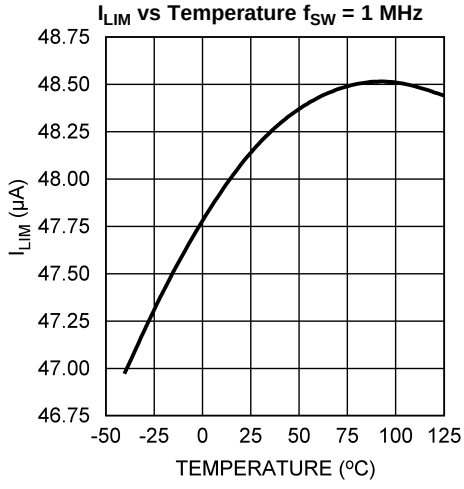

Figure 12.

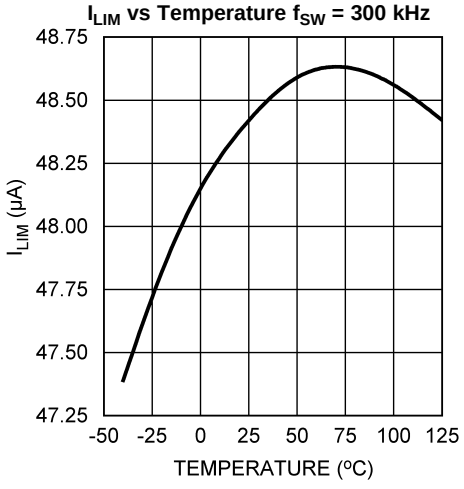

Figure 13.

Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

I_{VCC} vs Temperature f_{SW} = 1 MHz

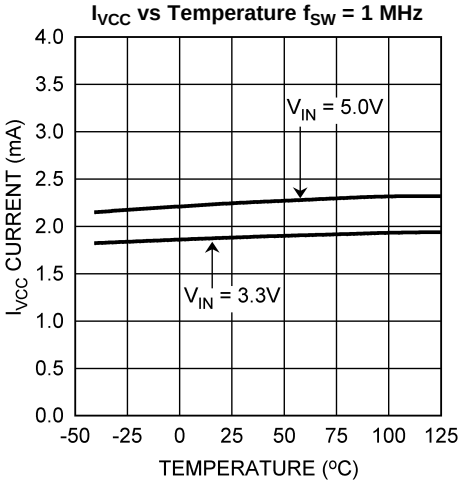

Figure 14.

I_{VCC} vs Temperature f_{SW} = 300 kHz

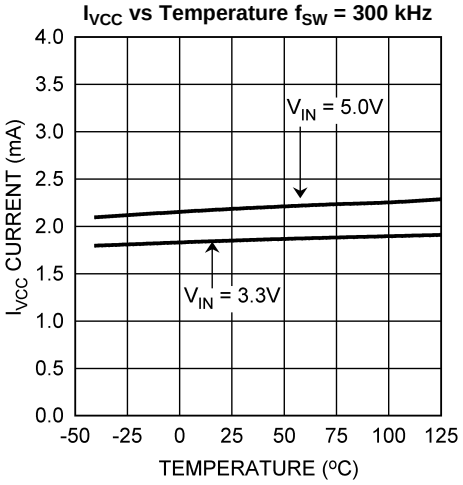

Figure 15.

Line Regulation V_{OUT} = 1.2V, I_{OUT} = 1A, f_{SW} = 300 kHz

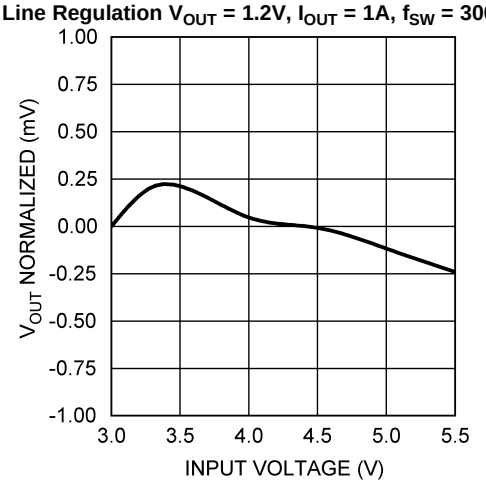

Figure 16.

Line Regulation V_{OUT} = 1.5V, I_{OUT} = 1A, f_{SW} = 1 MHz

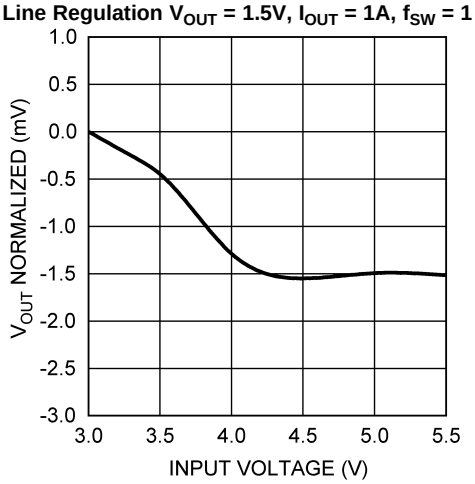

Figure 17.

Load Regulation V_{IN} = 3.3V, f_{SW} = 1 MHz

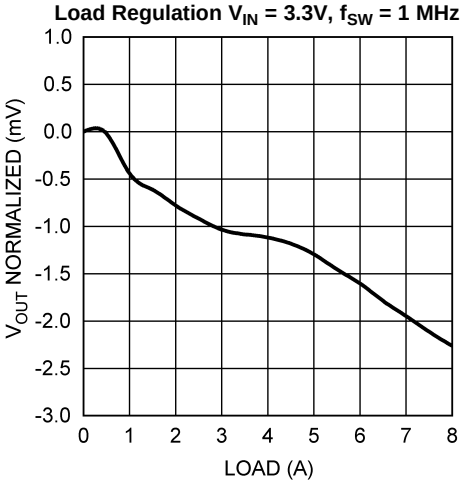

Figure 18.

Load Regulation V_{IN} = 3.3V, f_{SW} = 300 kHz

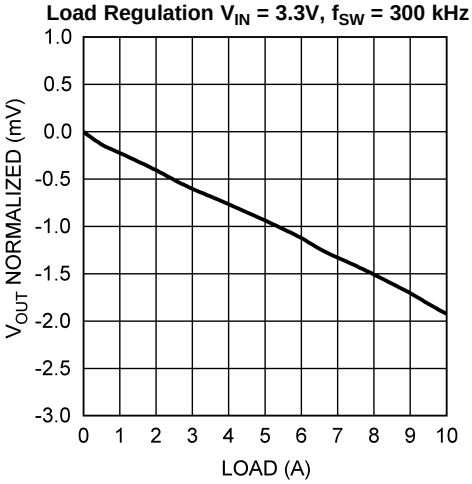

Figure 19.

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Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

Efficiency vs Load f_{SW} = 300 kHz, V_{IN} = 5.0V (Refer to Figure 56)

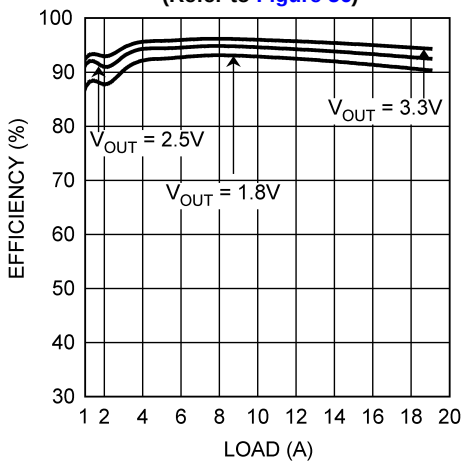

Figure 20.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 2.5V (Refer to Figure 56)

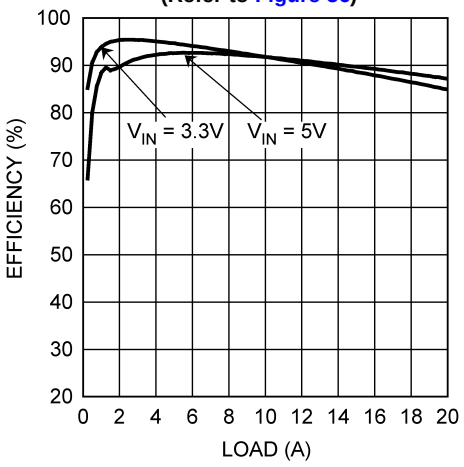

Figure 21.

Efficiency vs Load f_{SW} = 300 kHz, V_{IN} = 5.0V (Refer to Figure 56)

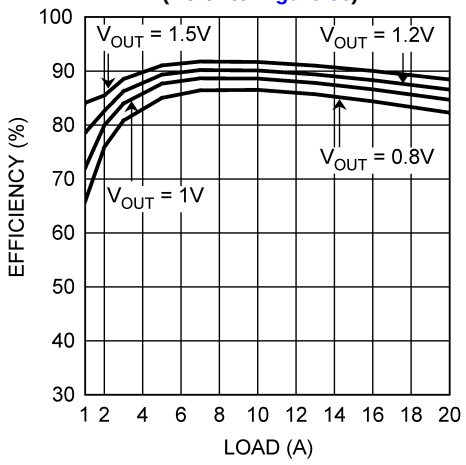

Figure 22.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.8V (Refer to Figure 56)

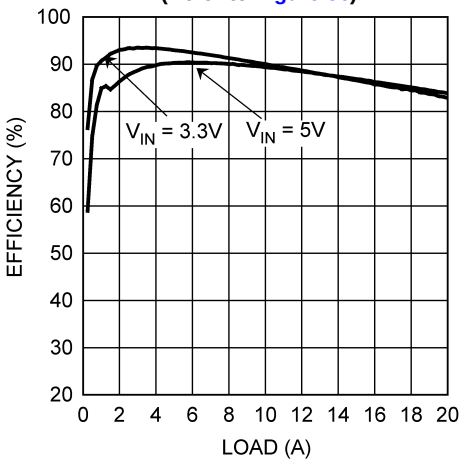

Figure 23.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 3.3V (Refer to Figure 56)

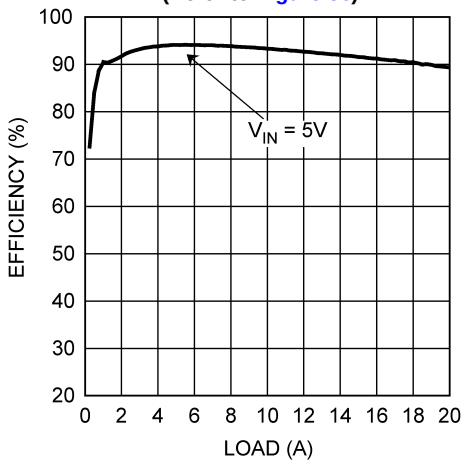

Figure 24.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.5V (Refer to Figure 56)

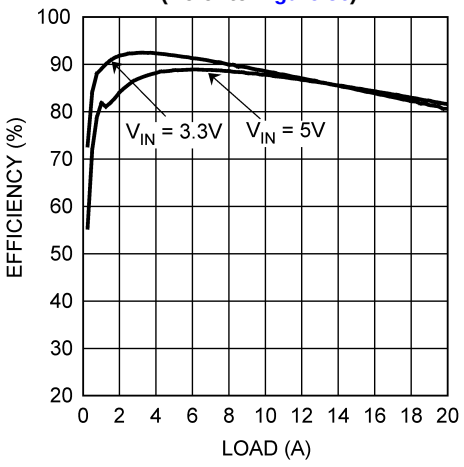

Figure 25.

Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.2V (Refer to Figure 56)

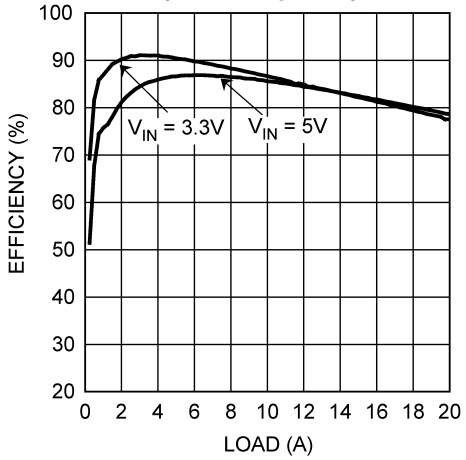

Figure 26.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.0V (Refer to Figure 56)

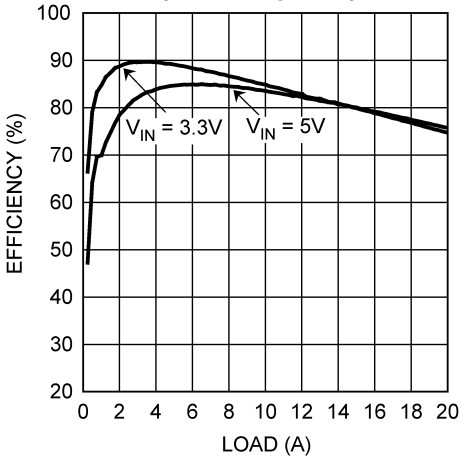

Figure 27.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 0.8V (Refer to Figure 56)

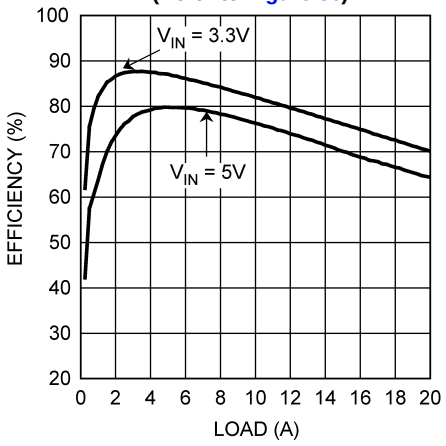

Figure 28.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 2.5V (Refer to AN-1450 (SNVA151) for BOM)

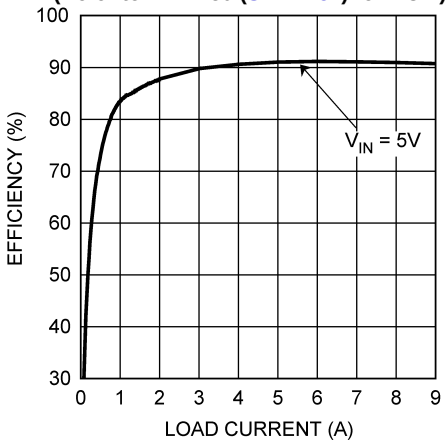

Figure 29.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 1.8V (Refer to AN-1450 (SNVA151) for BOM)

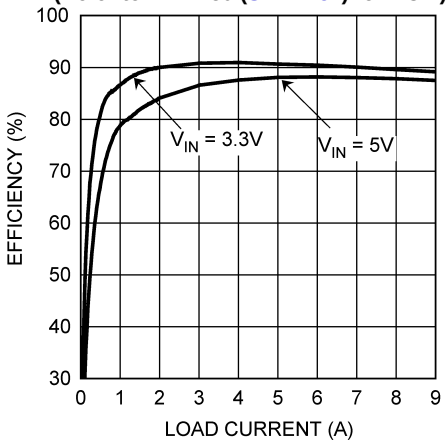

Figure 30.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 1.5V (Refer to AN-1450 (SNVA151) for BOM)

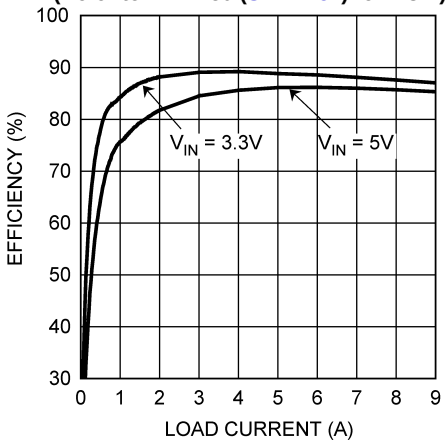

Figure 31.

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Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 1.2V (Refer to AN-1450 (SNVA151) for BOM)

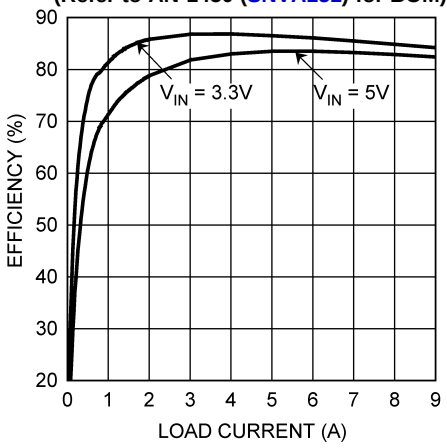

Figure 32.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 1.0V (Refer to AN-1450 (SNVA151) for BOM)

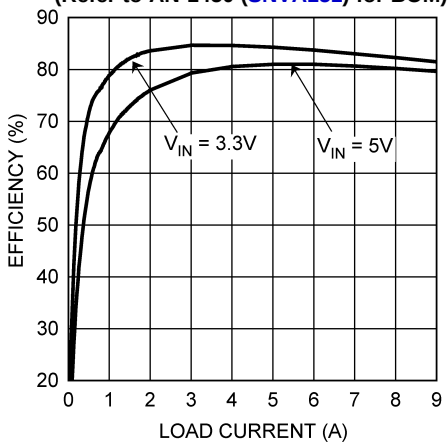

Figure 33.

Efficiency vs Load f_{SW} = 1 MHz, V_{OUT} = 0.8V (Refer to AN-1450 (SNVA151) for BOM)

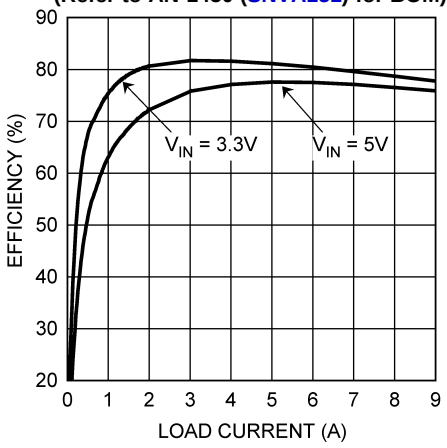

Figure 34.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 2.5V (Refer to AN-1450 (SNVA151) for BOM)

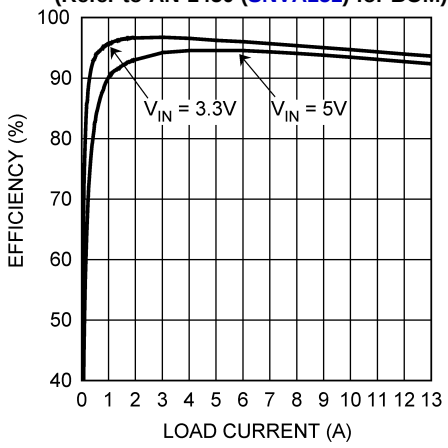

Figure 35.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.8V (Refer to AN-1450 (SNVA151) for BOM)

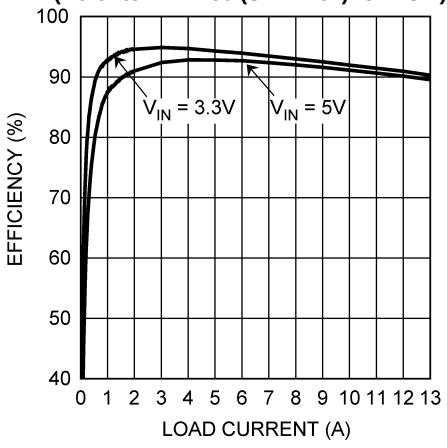

Figure 36.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.5V (Refer to AN-1450 (SNVA151) for BOM)

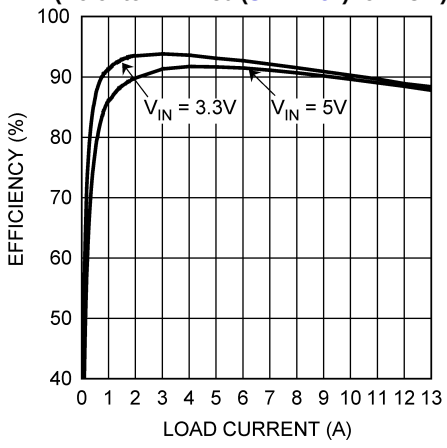

Figure 37.

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Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.2V (Refer to AN-1450 (SNVA151) for BOM)

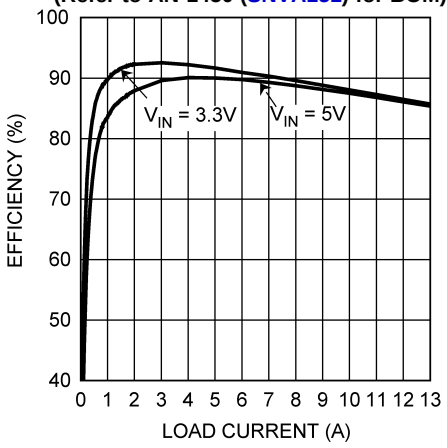

Figure 38.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 1.0V (Refer to AN-1450 (SNVA151) for BOM)

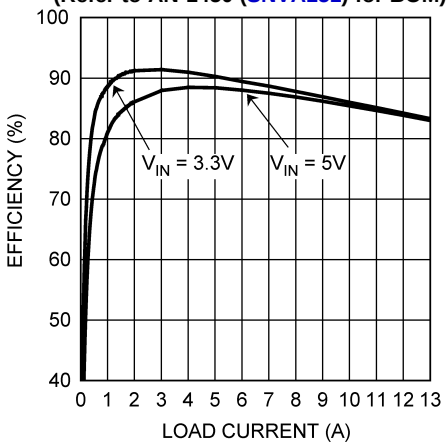

Figure 39.

Efficiency vs Load f_{SW} = 300 kHz, V_{OUT} = 0.8V (Refer to AN-1450 (SNVA151) for BOM)

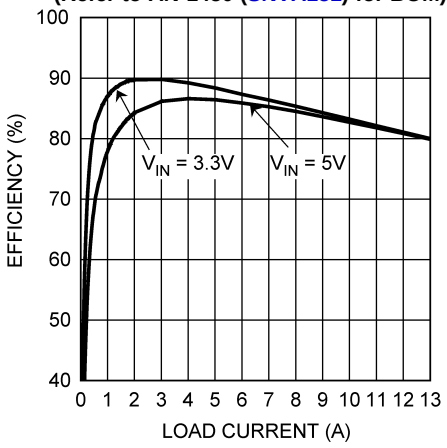

Figure 40.

Load Transient Response f_{SW} = 1 MHz, V_{IN} = 3.3V, I_{LOAD} = 100 mA to 3.5A (Refer to AN-1450 (SNVA151) for BOM)

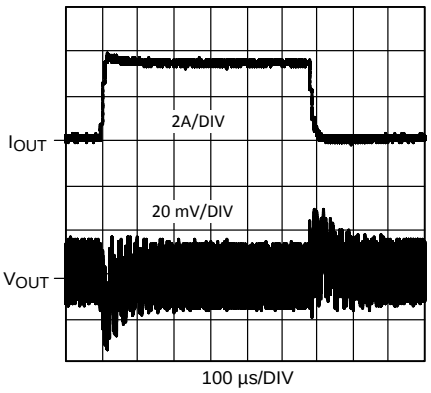

Figure 41.

Load Transient Response f_{SW} = 300 kHz, V_{IN} = 3.3V, I_{LOAD} = 100 mA to 3.5A (Refer to AN-1450 (SNVA151) for BOM)

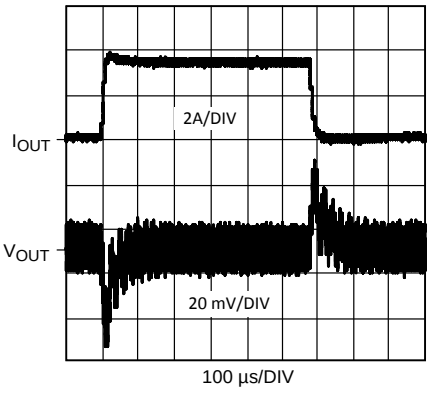

Figure 42.

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Typical Performance Characteristics (continued)

V_{IN} = 3.3, T_J = 25°C, I_{LOAD} = 1A unless otherwise specified.

Shutdown R_{LOAD} = 1Ω, V_{IN} = 5V

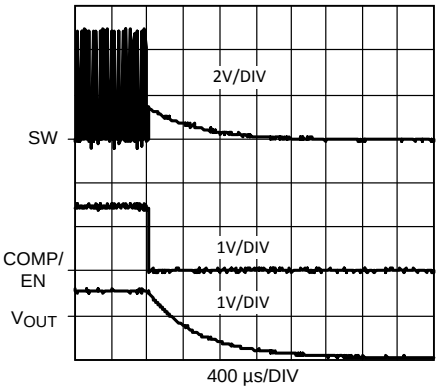

Figure 43.

Pre Bias Startup

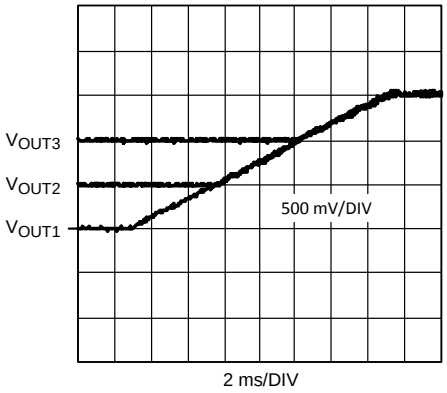

Figure 44.

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APPLICATION INFORMATION

THEORY OF OPERATION

The LM3743 is a voltage mode PWM buck controller featuring synchronous rectification at 300 kHz or 1 MHz. In steady state operation the LM3743 is always synchronous even at no load, thus simplifying the compensation design. The LM3743 ensures a smooth and controlled start-up to support pre-biased outputs. Two levels of current limit protection enhance the robustness of the power supply and requires no current sense resistor in the power path. The primary level of protection is the low side current limit and is achieved by sensing the voltage V_{DS} across the low side MOSFET. The second level of protection is the high side current limit, which protects power components from extremely high currents, caused by switch node short to ground.

NORMAL OPERATION

While in normal operation, the LM3743 IC controls the output voltage by controlling the duty cycle of the power FETs. The DC level of the output voltage is determined by a pair of feedback resistors using the following equation:

$$V_{OUT} = 0.8 \times \frac{R3 + R2}{R3} \quad (1)$$

(Designators refer to the Typical Application in the front page)

For synchronous buck regulators, the duty ratio D is approximately equal to:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

START UP

The LM3743 IC begins to operate when the COMP/EN pin is released from a clamped condition and the voltage at the V_{CC} pin has exceeded 2.84V. Once these two conditions have been met the internal 10µA current source begins to charge the soft-start capacitor connected at the SS/TRACK pin. During soft-start the voltage on the soft-start capacitor is connected internally to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the LM3743 reference voltage of 0.8V. At this point the reference voltage takes over at the non-inverting error amplifier input. The capacitance determines the length of the soft-start period, and can be approximated by:

$$C4 = (t_{SS} \times 10\ \mu A) / 0.8V \quad (3)$$

where

- t_{SS} is the desired soft-start time

In the event of either V_{CC} falling below UVLO or COMP/EN pin being pulled below 0.45V, the soft-start pin will discharge C4 to allow the output voltage to recover smoothly.

START UP WITH PRE-BIAS

A pre-bias output is a condition in which current from another source has charged up the output capacitor of the switching regulator before it has been turned on. The LM3743 features a proprietary glitch free monotonic pre-bias start-up method designed to ramp the output voltage from a pre-biased rail to the target nominal output voltage. The IC limits the on time of the low-side FET to 150 ns (typ) during soft-start, while allowing the high-side FET to adjust it's time according to soft-start voltage, V_{OUT}, and the internal voltage ramp. Any further commutation of the load current is carried by the body diode of the low-side FET or an external Schottky diode, if used. The low side current limit is active during soft-start while allowing the asynchronous switching. When soft-start is completed, the on-time of the low-side FET is allowed to increase in a controlled fashion up to the steady state duty cycle determined by the control loop. A plot of the LM3743 starting up into a pre-biased condition is shown in the Typical Performance Characteristics section.

Note that the pre-bias voltage must not be greater than the target output voltage of the LM3743, otherwise the LM3743 will pull the pre-bias supply down during steady state operation.

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TRACKING WITH EQUAL SOFT-START TIME

The LM3743 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS/TRACK pin. In this way, the output voltage slew rate of the LM3743 will be controlled by the master supply for loads that require precise sequencing. When the tracking function is used, no soft-start capacitor should be connected to the SS/TRACK pin. However in all other cases, a capacitor value (C4) of at least 560 pF should be connected between the soft-start pin and ground.

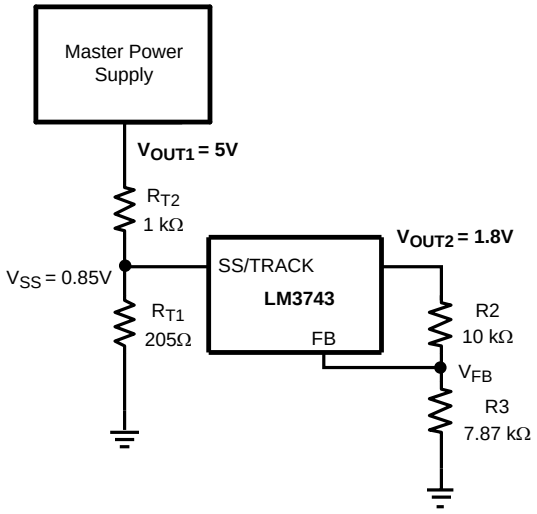

Figure 45. Tracking Circuit

One way to use the tracking feature is to design the tracking resistor divider so that the master supply's output voltage (V_{OUT1}) and the LM3743's output voltage (represented symbolically in Figure 45 as V_{OUT2}, therefore without explicitly showing the power components) both rise together and reach their target values at the same time. For this case, the equation governing the values of the tracking divider resistors R_{T1} and R_{T2} is:

$$R_{T1} = \frac{0.85}{V_{OUT1} - 0.85} \times R_{T2} \tag{4}$$

The top resistance R_{T2} must be set to 1 kΩ in order to limit current into the LM3743 during UVLO or shutdown. The final voltage of the SS/TRACK pin should be slightly higher than the feedback voltage of 0.8V, say about 0.85V as in the above equation. The 50 mV difference will ensure the LM3743 to reach regulation slightly before the master supply. If the master supply voltage was 5V and the LM3743 output voltage was 1.8V, for example, then the value of R_{T1} needed to give the two supplies identical soft-start times would be 205Ω. A timing diagram for the equal soft-start time case is shown in Figure 46.

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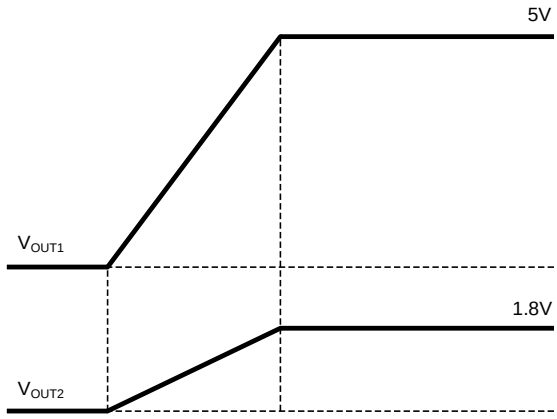

Figure 46. Tracking with Equal Soft-Start Time

TRACKING WITH EQUAL SLEW RATES

The tracking feature can alternatively be used not to make both rails reach regulation at the same time but rather to have similar rise rates (in terms of output dV/dt). In this case, the tracking resistors can be determined based on the following equation:

$$R_{T1} = \frac{0.80}{V_{OUT2} - 0.80} \times R_{T2} \quad (5)$$

For the example case of V_{OUT1} = 5V and V_{OUT2} = 1.8V, with R_{T2} set to 1 kΩ as before, R_{T1} is calculated from the above equation to be 887Ω. A timing diagram for the case of equal slew rates is shown in Figure 47.

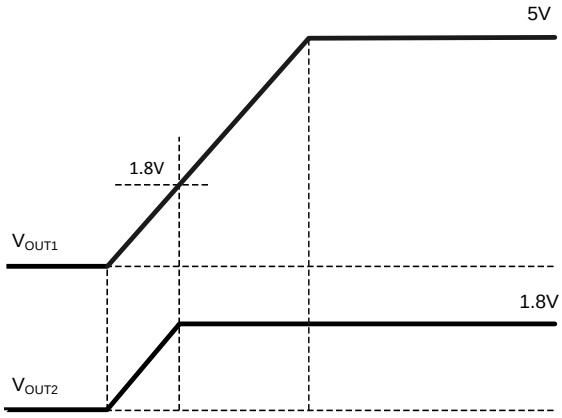

Figure 47. Tracking with Equal Slew Rate

TRACKING AND SHUTDOWN SEQUENCING

LM3743 is designed to track the output of a master power supply during start-up, but when the master supply powers down the output capacitor of the LM3743 will discharge cycle by cycle through the low-side FET. The off-time will reach 100% when the voltage at the track pin reaches zero volts. This condition will persist as long as the master output voltage is zero volts and the drivers of the LM3743 are still on. For example if the load is required to not be discharged, the drivers must be shut-off before the master powers down. This is achieved by shutting down the LM3743 or bring V_{CC} below UVLO falling threshold. In this case the load will not be discharged.

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SHUTDOWN

The LM3743 IC can be put into shutdown mode by bringing the voltage at the COMP/EN pin below 0.45V (typ). The quiescent current during shutdown is approximately 6 µA (typ). During shutdown both the high-side and low-side FETs are disabled. The soft-start capacitor is discharged through an internal FET so that the output voltage rises in a controlled fashion when the part is enabled again. When enabled a 4 µA pull-up current increases the charge of the compensation capacitors.

UNDER VOLTAGE LOCK-OUT (UVLO)

If V_{CC} drops below 2.66V (typ), the chip enters UVLO mode. UVLO consists of turning off the top and bottom FETs and remaining in that condition until V_{CC} rises above 2.84V (typ). As with shutdown, the soft-start capacitor is discharged through an internal FET, ensuring that the next start-up will be controlled by the soft-start circuitry.

MOSFET GATE DRIVE

The LM3743 has two gate drivers designed for driving N-channel MOSFETs in synchronous mode. Power for the high gate driver is supplied through the BOOT pin, while driving power for the low gate is provided through the V_{CC} pin. The BOOT voltage is supplied from a local charge pump structure which consists of a Schottky diode and 0.1 µF capacitor, shown in Figure 48. Since the bootstrap capacitor (C10) is connected to the SW node, the peak voltage impressed on the BOOT pin is the sum of the input voltage (V_{IN}) plus the voltage across the bootstrap capacitor (ignoring any forward drop across the bootstrap diode). The bootstrap capacitor is charged up by V_{IN} (called V_{BOOT_DC} here) whenever the upper MOSFET turns off.

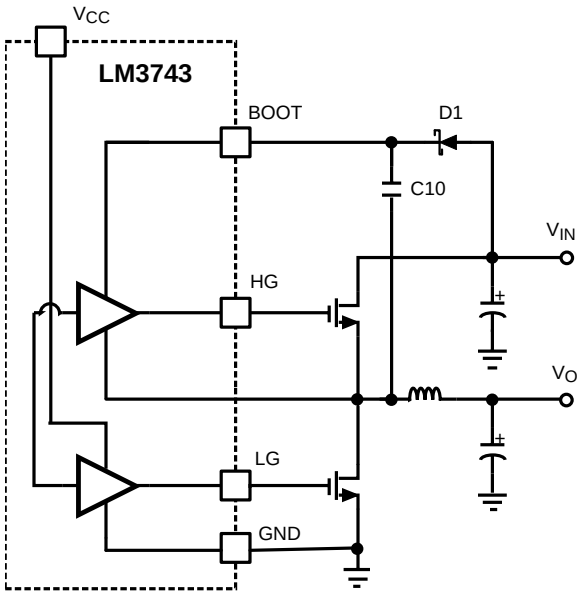

Figure 48. Charge Pump Circuit and Driver Circuitry

The output of the low-side driver swings between V_{CC} and ground, whereas the output of the high-side driver swings between V_{IN} + V_{BOOT_DC} and V_{IN}. To keep the high-side MOSFET fully on, the Gate pin voltage of the MOSFET must be higher than its instantaneous Source pin voltage by an amount equal to the 'Miller plateau'. It can be shown that this plateau is equal to the threshold voltage of the chosen MOSFET plus a small amount equal to I_{OUT}/g. Here I_{OUT} is the maximum load current of the application, and g is the transconductance of this MOSFET (typically about 100 for logic-level devices). That means we must choose V_{BOOT_DC} to at least exceed the Miller plateau level. This may therefore affect the choice of the threshold voltage of the external MOSFETs, and that in turn may depend on the chosen V_{IN} rail.

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So far in the discussion above, the forward drop across the bootstrap diode has been ignored. But since that does affect the output of the driver, it is a good idea to include this drop in the following examples. Looking at the Typical Application schematic, this means that the difference voltage V_{IN} - V_{D1}, which is the voltage the bootstrap capacitor charges up to, must always be greater than the maximum tolerance limit of the threshold voltage of the upper MOSFET. Here V_{D1} is the forward voltage drop across the bootstrap diode D1. This voltage drop may place restrictions on the type of MOSFET selected.

The capacitor C10 serves to maintain enough voltage between the top MOSFET gate and source to control the device even when the top MOSFET is on and its source has risen up to the input voltage level. The charge pump circuitry is fed from V_{IN}, which can operate over a range from 3.0V to 5.5V. Using this basic method the voltage applied to the high side gate V_{IN} - V_{D1}. This method works well when V_{IN} is 5V±10%, because the gate drives will get at least 4.0V of drive voltage during the worst case of V_{IN-MIN} = 4.5V and V_{D1-MAX} = 0.5V. Logic level MOSFETs generally specify their on-resistance at V_{GS} = 4.5V. When V_{CC} = 3.3V±10%, the gate drive at worst case could go as low as 2.5V. Logic level MOSFETs are not ensured to turn on, or may have much higher on-resistance at 2.5V. Sub-logic level MOSFETs, usually specified at V_{GS} = 2.5V, will work, but are more expensive and tend to have higher on-resistance.

LOW-SIDE CURRENT LIMIT

The main current limit of the LM3743 is realized by sensing the voltage drop across the low-side FET as the load current passes through it. The R_{DSON} of the MOSFET is a known value; hence the voltage across the MOSFET can be determined as:

$$V_{DS} = I_{OUT} \times R_{DSON} \quad (6)$$

The current flowing through the low-side MOSFET while it is on is the falling portion of the inductor current. The current limit threshold is determined by an external resistor, R1, connected between the switching node and the ILIM pin. A constant current (I_{ILIM}) of 50 µA typical is forced through R1, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has been reached. To obtain a more accurate value for R1 you must consider the operating values of R_{DSON} and I_{ILIM} at their operating temperatures in your application and the effect of slight parameter variations from part to part. R1 can be found by using the following equation using the R_{DSON} value of the low side MOSFET at it's expected hot temperature and the absolute minimum value expected over the full temperature range for the I_{ILIM} which is 42.5 µA:

$$R1 = R_{DSON-HOT} \times I_{CLIM} / I_{ILIM} \quad (7)$$

For example, a conservative 15A current limit (I_{CLIM}) in a 10A design with a $R_{DSON-HOT}$ of 10 mΩ would require a 3.83 kΩ resistor. The LM3743 enters current limit mode if the inductor current exceeds the set current limit threshold. The inductor current is first sampled 50 ns after the low-side MOSFET turns on. Note that in normal operation mode the high-side MOSFET always turns on at the beginning of a clock cycle. In current limit mode, by contrast, the high-side MOSFET on-pulse is skipped. This causes inductor current to fall. Unlike a normal operation switching cycle, however, in a current limit mode switching cycle the high-side MOSFET will turn on as soon as inductor current has fallen to the current limit threshold.

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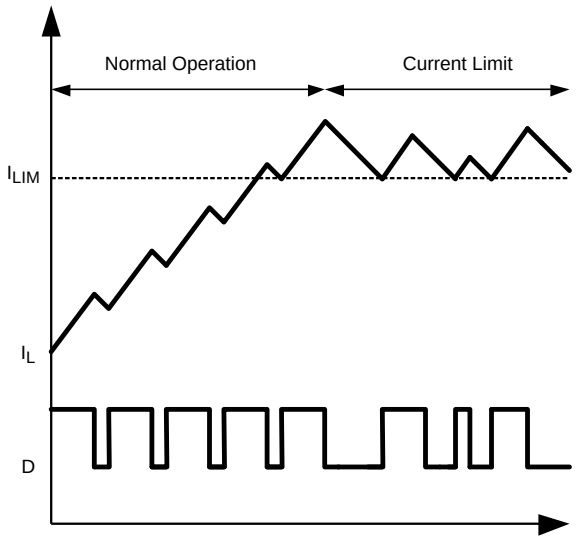

Figure 49. Current Limit Threshold

The low-side current sensing scheme can only limit the current during the converter off-time, when inductor current is falling. Therefore in a typical current limit plot the valleys are normally well defined, but the peaks are variable, according to the duty cycle, see Figure 49. The PWM error amplifier and comparator control the pulse of the high-side MOSFET, even during current limit mode, meaning that peak inductor current can exceed the current limit threshold. For example, during an output short-circuit to ground, and assuming that the output inductor does not saturate, the maximum peak inductor current during current limit mode can be calculated with the following equation:

$$I_{PK\text{-}CL} = I_{CLIM} + (T_{SW} - 200\ ns)\ \frac{V_{IN} - V_O}{L} \quad (8)$$

where

- T_{SW} is the inverse of switching frequency f_{SW}

The 200 ns term represents the minimum off-time of the duty cycle, which ensures enough time for correct operation of the current sensing circuitry.

In order to minimize the temperature effects of the peak inductor currents, the IC enters hiccup mode after 15 over current events, or a long current limit event that lasts 15 switching cycles (the counter is reset when 32 non-current limit cycles occur in between two current limit events). Hiccup mode will be discussed in further detail in the “Hiccup Mode and Internal Soft-Start” section.

HIGH-SIDE COARSE CURRENT LIMIT

The LM3743 employs a comparator to monitor the voltage across the high-side MOSFET when it is on. This provides protection for short circuits from switch node to ground or the case when the inductor is shorted, which the low side current limit cannot detect. A 200 ns blanking time period after the high-side FET turns on is used to prevent switching transient voltages from tripping the high-side current limit without cause. If the difference between V_{CC} pin and SW pin voltage exceeds 500 mV, the LM3743 will immediately enter hiccup mode (see HICCUP MODE AND INTERNAL SOFT-START section).

OUTPUT UNDER-VOLTAGE PROTECTION (UVP)

After the end of soft-start the output UVP comparator is activated. The threshold is 50% of the feedback voltage. Once the comparator indicates UVP for more than 7 µs typ. (glitch filter time), the IC goes into hiccup mode.

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HICCUP MODE AND INTERNAL SOFT-START

Hiccup protection mode is designed to protect the external components of the circuit (output inductor, FETs, and input voltage source) from thermal stress. During hiccup mode, the LM3743 disables both the high-side and low-side FETs and begins a cool down period of 5.5 ms. At the conclusion of this cool down period, the regulator performs an internal 3.6 ms soft-start. There are three distinct conditions under which the IC will enter the hiccup protection mode:

1. The low-side current sensing threshold has exceeded the current limit threshold for fifteen sampled cycles, see Figure 50. Each cycle is sampled at the start of each off time (t_{OFF}). The low-side current limit counter is reset when 32 consecutive non-current limit cycles occur in between two current limit events.
2. The high-side current limit comparator has sensed a differential voltage larger than 500 mV.
3. The voltage at the FB pin has fallen below 0.4V, and the UVP comparator has sensed this condition for 7 µs (during steady state operation).

The band gap reference, the external soft-start, and internal hiccup soft-start of 3.6 ms (typ) connect to the non-inverting input of the error amplifier through a multiplexer. The lowest voltage of the three connects directly to the non-inverting input. Hiccup mode will not discharge the external soft-start, only UVLO or shut-down will. When in hiccup mode the internal 5.5 ms timer is set, and the internal soft-start capacitor is discharged. After the 5.5 ms timeout, the internal 3.6 ms soft-start begins, see Figure 51. During soft-start, only low-side current limit and high side current limit can put the LM3743 into hiccup mode.

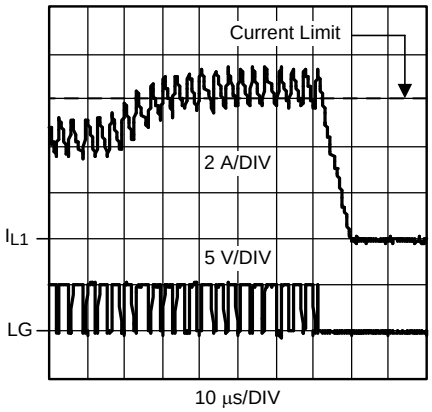

Figure 50. Entering Hiccup Mode

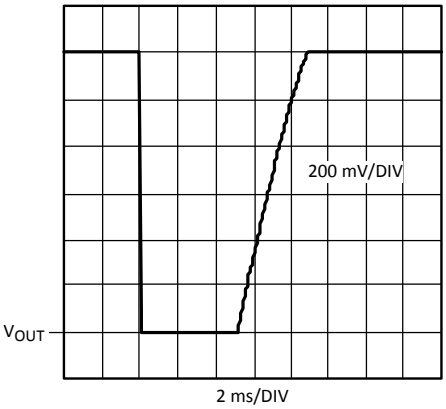

Figure 51. Hiccup Time-Out and Internal Soft-Start

For example, if the low-side current limit is 10A, then once in overload the low-side current limit controls the valley current and only allows an average amount of 10A plus the ripple current to pass through the inductor and FETs for 15 switching cycles. In such an amount of time, the temperature rise is very small. Once in hiccup mode, the average current through the high-side FET is:

$$I_{HSF\text{-}AVE} = (I_{CLIM} + \Delta I) \times [\, D(15 \text{ cycles} \times T_{SW}) \,] / 5.5 \text{ ms} = 71\text{mA} \quad (9)$$

With an arbitrary D = 60%, ripple current of 3A, and a 300 kHz switching frequency.

The average current through the low-side FET is:

$$I_{LSF\text{-}AVE} = (I_{CLIM} + \Delta I) \times [\, (1\text{–}D) \times (15 \text{ cycles} \times T_{SW}) \,] / 5.5 \text{ ms} = 47\text{mA} \quad (10)$$

And the average current through the inductor is:

$$I_{L\text{-}AVE} = (I_{CLIM} + \Delta I) \times [\, (15 \text{ cycles} \times T_{SW}) \,] / 5.5 \text{ ms} = 118\text{mA} \quad (11)$$

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DESIGN CONSIDERATIONS

The following is a design procedure for selecting all the components in the Typical Application circuit on the front page. This design converts 5V (V_{IN}) to 1.8V (V_{OUT}) at a maximum load of 10A with an efficiency of 90% and a switching frequency of 300 kHz. The same procedures can be followed to create many other designs with varying input voltages, output voltages, load currents, and switching frequency.

Switching Frequency

Selection of the operating switching frequency is based on trade-offs between size, cost, efficiency, and response time. For example, a lower frequency will require larger more expensive inductors and capacitors. While a higher switching frequency will generally reduce the size of these components, but will have a reduction in efficiency. Fast switching converters allow for higher loop gain bandwidths, which in turn have the ability to respond quickly to load and line transients. For the example application we have chosen a 300 kHz switching frequency because it will reduce the switching power losses and in turn allow for higher conduction losses considering the same power loss criteria, thus it is possible to sustain a higher load current.

Output Inductor

The output inductor is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}) also called the AC component of the inductor current. The DC current into the load is equal to the average current flowing in the inductor. The inductance is chosen by selecting between trade-offs in efficiency, size, and response time. The recommended percentage of AC component to DC current is 30% to 40%, this will provide the best trade-off between energy requirements and size, (read AN-1197 (SNVA038) for theoretical analysis). Another criteria is the ability to respond to large load transient responses; the smaller the output inductor, the more quickly the converter can respond. The equation for output inductor selection is:

$$L = \frac{V_{IN\text{-}MAX} - V_{OUT}}{\Delta I_{OUT} \times f_{SW}} \times D_{MIN} \tag{12}$$

$$L = \frac{5.5V - 1.8V}{0.3 \times 10A \times 300\ kHz} \times \frac{1.8V}{5.5V} \tag{13}$$

$$L = 1.34\ \mu H \tag{14}$$

Here we have plugged in the values for input voltage, output voltage, switching frequency, and 30% of the maximum load current. This yields an inductance of 1.34 µH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is (I_{OUT} + (0.5 x ΔI_{OUT})) = 11.5A, for a 10A design and a AC current of 3A.

The Coiltronics DR125–1R5 is 1.5 µH, is rated to 13.8A RMS current, and has a direct current resistance (DCR) of 3 mΩ. After selecting the Coiltronics DR125–1R5 for the output inductor, actual inductor current ripple must be re-calculated with the selected inductance value. This information is needed to determine the RMS current through the input and output capacitors. Re-arranging the equation used to select inductance yields the following:

$$\Delta I_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \times L_{ACTUAL}} \times D_{MIN} \tag{15}$$

$V_{IN(MAX)}$ is assumed to be 10% above the steady state input voltage, or 5.5V at V_{IN} = 5.0V. The re-calculated current ripple will then be 2.69A. This gives a peak inductor/switch current will be 11.35A.

Output Capacitor

The output capacitor in a switching regulator is selected on the basis of capacitance, equivalent series resistance (ESR), size, and cost. In this example the output current is 10A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. An important specification in switching converters is the output voltage ripple ΔV_{OUT}. At 300 kHz the impedance of most capacitors is very small compared to ESR, hence ESR becomes the main selection criteria. In this design the load requires a 2% ripple , which results in a ΔV_{OUT} of 36 $mV_{P\text{-}P}$. Thus the maximum ESR is then:

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$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (16)$$

ESR_{MAX} is 13 mΩ. Aluminum electrolytic (Al-E), tantalum (Ta), solid aluminum, organic, and niobium (Nb) capacitors are all popular in switching converters. In general, by the time enough capacitors have been paralleled to obtain the desired ESR, the bulk capacitance is more than enough to supply the load current during a transient from no-load to full load. The number and type of capacitors used depends mainly on their size and cost. One exception to this is multi-layer ceramic capacitors. MLCCs have very low ESR, but also low capacitance in comparison with other types. This makes them attractive for lower power designs. For higher power or for fast load transients the number of MLCCs needed often increases the size and cost to unacceptable levels. Because the load could transition quickly from 0 to 10A, more bulk capacitance is needed than the MLCCs can provide. One compromise is a solid electrolytic POSCAP from Sanyo or SP-caps from Panasonic. POSCAP and SPcaps often have large capacitances needed to supply currents for load transients, and low ESRs. The 6TPD470M by Sanyo has 470 µF, and a maximum ESR of 10 mΩ. Solid electrolytics have stable ESR relative to temperature, and capacitance change is relatively immune to bias voltage. Tantalums (Ta), niobium (Nb), and Al-E are good solutions for ambient operating temperatures above 0°C, however their ESR tends to increase quickly below 0°C ambient operating temperature, so these capacitor types are not recommended for this area of operation.

Input Capacitor

The input capacitors in a buck converter are subjected to high RMS current stress. Input capacitors are selected for their ability to withstand the heat generated by the RMS current and the ESR as specified by the manufacturer. Input RMS ripple current is approximately:

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)}$$

where

- duty cycle $D = V_{OUT}/V_{IN}$ (17)

The worst-case ripple for a buck converter occurs during full load and when the duty cycle (D) is 0.5.

When multiple capacitors of the same type and value are paralleled, the power dissipated by each input capacitor is:

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n}$$

where

- n is the number of paralleled capacitors
- ESR is the equivalent series resistance of each capacitor (18)

The equation above indicates that power loss in each capacitor decreases rapidly as the number of input capacitors increases. For this 5V to 1.8V design the duty cycle is 0.36. For a 10A maximum load the RMS current is 4.8A.

Connect one or two 22 µF MLCC as close as possible across the drain of the high-side MOSFET and the source of the low-side MOSFET, this will provide high frequency decoupling and satisfy the RMS stress. A bulk capacitor is recommended in parallel with the MLCC in order to prevent switching frequency noise from reflecting back into the input line, this capacitor should be no more than 1inch away from the MLCC capacitors.

MOSFETs

Selection of the power MOSFETs is governed by a trade-off between cost, size, and efficiency. One method is to determine the maximum cost that can be endured, and then select the most efficient device that fits that price. Using a spreadsheet to estimate the losses in the high-side and low-side MOSFETs is one way to determine relative efficiencies between different MOSFETs. Good correlation between the prediction and the bench result is not ensured.

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Losses in the high-side MOSFET can be broken down into conduction loss, gate charging loss, and switching loss. Conduction, or I^2R loss, is approximately:

For the high side FET:

$$P_C = D \ (I_{OUT}^2 \times R_{DSON\text{-}HI} \times 1.3) \quad (19)$$

For the low side FET:

$$P_C = (1 - D) \times (I_{OUT}^2 \times R_{DSON\text{-}LO} \times 1.3) \quad (20)$$

In the above equations the factor 1.3 accounts for the increase in MOSFET R_{DSON} due to heating. Alternatively, the 1.3 can be ignored and the R_{DSON} of the MOSFET estimated using the R_{DSON} vs. Temperature curves in the MOSFET manufacturer datasheet.

Gate charging loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{GC} = (V_{CC}) \times Q_G \times f_{SW} \quad (21)$$

V_{CC} is the driving voltage (see MOSFET GATE DRIVE section) and Q_G is the gate charge of the MOSFET. If multiple devices will be placed in parallel, their gate charges can simply be summed to form a cumulative Q_G.

Switching loss occurs during the brief transition period as the high-side MOSFET turns on and off, during which both current and voltage are present in the channel of the MOSFET. It can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}$$

where

- t_r and t_f are the rise and fall times of the MOSFET (22)

Switching loss occurs in the high-side MOSFET only.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 5.5V. The maximum drive voltage at the gate of the high-side MOSFET is 5.0V, and the maximum drive voltage for the low-side MOSFET is 5.5V. For designs between 5A and 10A, single MOSFETs in SO-8 provide a good trade-off between size, cost, and efficiency.

V_{CC} Filtering

To ensure smooth DC voltage for the chip supply a 1 µF (C3), X5R MLCC type or better must be placed as close as possible to the V_{CC} and GND pin. Together with a small 1 to 4.99Ω resistor placed between the input rail and the V_{CC} pin, a low pass filter is formed to filter out high frequency noise from injecting into the V_{CC} rail. Since V_{CC} is also the sense pin for the high-side current limit, the resistor should connect close to the drain of the high-side MOSFET to prevent IR drops due to trace resistance. A second design consideration is the low pass filter formed by C3 and R6 on the V_{CC} pin, a fast slew rate, large amplitude load transient may cause a larger voltage droop on C_{IN} than on V_{CC} pin. This may lead to a lower current at which high-side protection may occur. Thus increase the bulk input capacitor if the high-side current limit is engaging due to a dynamic load transient behavior as explained above.

Bootstrap Diode (D1)

The MBR0520 and BAT54 work well as a bootstrap diode in most designs. Schottky diodes are the preferred choice for the bootstrap circuit because of their low forward voltage drop. For circuits that will operate at high ambient temperature the Schottky diode datasheet must be read carefully to ensure that the reverse current leakage at high temperature does not increase enough to deplete the charge on the bootstrap capacitor while the high side FET is on. Some Schottky diodes increase their reverse leakage by as much as 1000 times at high temperatures. Fast rectifier and PN junction diodes maintain low reverse leakage even at high ambient temperature. These diode types have higher forward voltage drop but can still be used for high ambient temperature operation.

Control Loop Compensation

The LM3743 uses voltage-mode ('VM') PWM control to correct changes in output voltage due to line and load transients. VM requires careful small signal compensation of the control loop for achieving high bandwidth and good phase margin.

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The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output inductor, output capacitor, and load. The second part is the error amplifier, which for the LM3743 is a 30 MHz op-amp used in the classic inverting configuration. Figure 52 shows the regulator and control loop components.

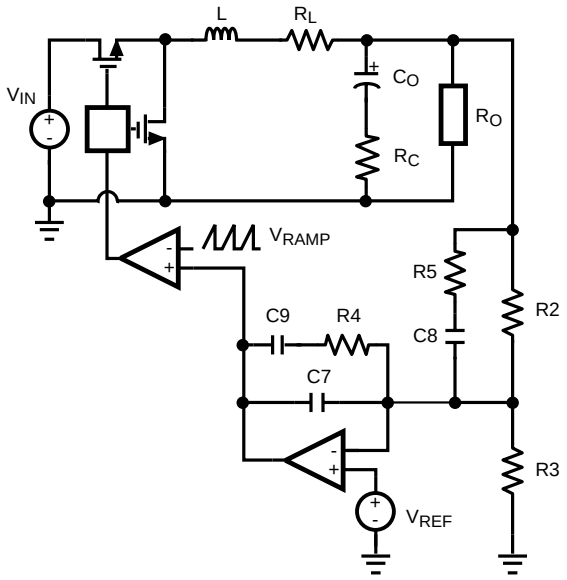

Figure 52. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to see. Software tools such as Excel, MathCAD, and Matlab are useful for showing how changes in compensation or the power stage affect system gain and phase.

The power stage modulator provides a DC gain A_{DC} that is equal to the input voltage divided by the peak-to-peak value of the PWM ramp. This ramp is $1.0V_{pk-pk}$ for the LM3743. The inductor and output capacitor create a double pole at frequency f_{DP}, and the capacitor ESR and capacitance create a single zero at frequency f_{ESR}. For this example, with V_{IN} = 5.0V, these quantities are:

$$A_{DC} = \frac{V_{IN}}{V_{RAMP}} = \frac{5.0}{1.0} = 5V/V \quad (23)$$

$$f_{DP} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_L}{LC_O(R_O + ESR)}} = 6\ kHz \quad (24)$$

$$f_{ESR} = \frac{1}{2\pi C_O ESR} = 33.9\ kHz \quad (25)$$

In the equation for f_{DP}, the variable R_L is the power stage resistance, and represents the inductor DCR plus the on resistance of the top power MOSFET. R_O is the output voltage divided by output current. The power stage transfer function G_{PS} is given by the following equation, and Figure 53 shows Bode plots of the phase and gain in this example.

$$G_{PS} = \frac{AV_{IN} \times R_O}{V_{RAMP}} \times \frac{sC_O R_C + 1}{as^2 + bs + c} \quad (26)$$

$$a = LC_O(R_O + R_C) \quad (27)$$

$$b = L + C_O(R_O R_L + R_O R_C + R_C R_L) \quad (28)$$

$$c = R_O + R_L \quad (29)$$

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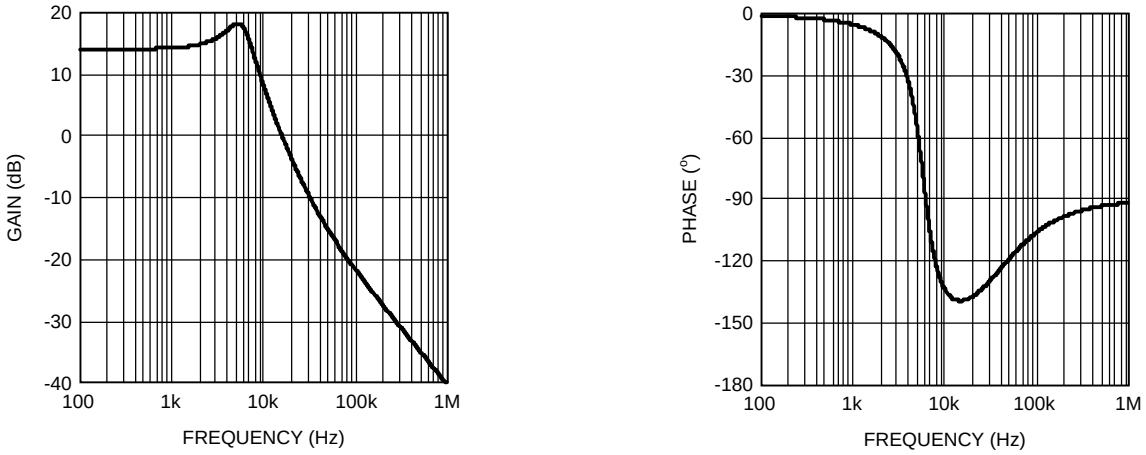

Figure 53. Power Stage Gain and Phase

The double pole at 6 kHz causes the phase to drop to approximately -140° at around 15 kHz. The ESR zero, at 33.9 kHz, provides a +90° boost that prevents the phase from dropping to -180º. If this loop were left uncompensated, the bandwidth would be approximately 15 kHz and the phase margin 40°. In theory, the loop would be stable, but would suffer from poor DC regulation (due to the low DC gain) and would be slow to respond to load transients (due to the low bandwidth.) In practice, the loop could easily become unstable due to tolerances in the output inductor, capacitor, or changes in output current, or input voltage. Therefore, the loop is compensated using the error amplifier and a few passive components.

For this example, a Type III, or three-pole-two-zero approach gives optimal bandwidth and phase.

In most voltage mode compensation schemes, including Type III, a single pole is placed at the origin to boost DC gain as high as possible. Two zeroes f_{Z1} and f_{Z2} are placed at the double pole frequency to cancel the double pole phase lag. Then, a pole, f_{P1} is placed at the frequency of the ESR zero. A final pole f_{P2} is placed at one-half of the switching frequency. The gain of the error amplifier transfer function is selected to give the best bandwidth possible without violating the Nyquist stability criteria. In practice, a good crossover point is one-fifth of the switching frequency, or 60 kHz for this example. The generic equation for the error amplifier transfer function is:

$$G_{EA} = A_{EA} \times \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \quad (30)$$

In this equation the variable A_{EA} is a ratio of the values of the capacitance and resistance of the compensation components, arranged as shown in Figure 52. A_{EA} is selected to provide the desired bandwidth. A starting value of 80,000 for A_{EA} should give a conservative bandwidth. Increasing the value will increase the bandwidth, but will also decrease phase margin. Designs with 45-60° are usually best because they represent a good trade-off between bandwidth and phase margin. In general, phase margin is lowest and gain highest (worst-case) for maximum input voltage and minimum output current. One method to select A_{EA} is to use an iterative process beginning with these worst-case conditions.

1. Increase A_{EA}
2. Check overall bandwidth and phase margin
3. Change V_{IN} to minimum and recheck overall bandwidth and phase margin
4. Change I_O to maximum and recheck overall bandwidth and phase margin

The process ends when both bandwidth and phase margin are sufficiently high. For this example input voltage can vary from 4.5V to 5.5V and output current can vary from 0 to 10A, and after a few iterations a moderate gain factor of 90 dB is used.

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The error amplifier of the LM3743 has a unity-gain bandwidth of 30 MHz. In order to model the effect of this limitation, the open-loop gain can be calculated as:

$$OPG = \frac{2\pi \times 30\ MHz}{s} \tag{31}$$

The new error amplifier transfer function that takes into account unity-gain bandwidth is:

$$H_{EA} = \frac{G_{EA} \times OPG}{1 + G_{EA} + OPG} \tag{32}$$

The gain and phase of the error amplifier are shown in Figure 54.

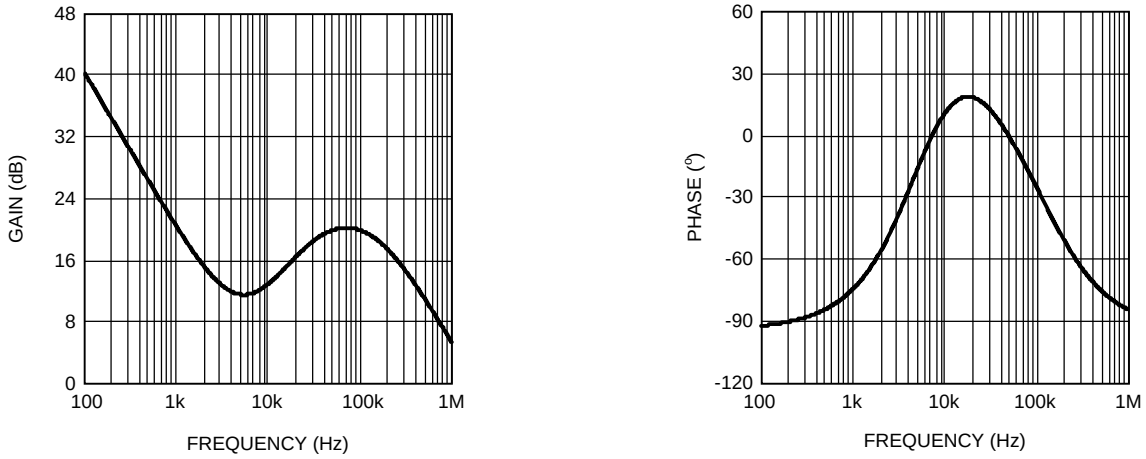

Figure 54. Error Amp. Gain and Phase

In VM regulators, the top feedback resistor R2 forms a part of the compensation. Setting R2 to 10 kΩ±1%, usually gives values for the other compensation resistors and capacitors that fall within a reasonable range. (Capacitances > 1 pF, resistances <1 MΩ) C7, C8, C9, R4, and R5 are selected to provide the poles and zeroes at the desired frequencies, using the following equations:

$$C7 = \frac{f_{Z1}}{A_{EA} \times 10{,}000 \times f_{P2}} = 49\ pF \tag{33}$$

$$C9 = \frac{1}{A_{EA} \times 10{,}000} - C7 = 1.2\ nF \tag{34}$$

$$C8 = \frac{1}{2\pi \times 10{,}000} \times \left(\frac{1}{f_{Z2}} - \frac{1}{f_{P1}}\right) = 2.2\ nF \tag{35}$$

$$R4 = \frac{1}{2\pi \times C9 \times f_{Z1}} = 22.1\ k\Omega \tag{36}$$

$$R5 = \frac{1}{2\pi \times C8 \times f_{P1}} = 2.15\ k\Omega \tag{37}$$

In practice, a good trade off between phase margin and bandwidth can be obtained by selecting the closest ±10% capacitor values above what are suggested for C7 and C8, the closest ±10% capacitor value below the suggestion for C9, and the closest ±1% resistor values below the suggestions for R4, R5. Note that if the suggested value for R5 is less than 100Ω, it should be replaced by a short circuit. Following this guideline, the compensation components will be:

C7 = 47 pF±10%, C9 = 1.5 nF±10%

C8 = 2.2 nF±10%, R4 = 22.6 kΩ±1%

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R5 = 2.1 kΩ±1%

The transfer function of the compensation block can be derived by considering the compensation components as impedance blocks Z_F and Z_I around an inverting op-amp:

$$G_{EA\text{-}ACTUAL} = \frac{Z_F}{Z_I} \tag{38}$$

$$Z_F = \frac{\frac{1}{sC7} \times \left(10{,}000 + \frac{1}{sC9}\right)}{10{,}000 + \frac{1}{sC7} + \frac{1}{sC9}} \tag{39}$$

$$Z_1 = \frac{R4\left(R5 + \frac{1}{sC8}\right)}{R4 + R5 + \frac{1}{sC8}} \tag{40}$$

As with the generic equation, $G_{EA\text{-}ACTUAL}$ must be modified to take into account the limited bandwidth of the error amplifier. The result is:

$$H_{EA} = \frac{G_{EA\text{-}ACTUAL} \times OPG}{1 + G_{EA\text{-}ACTUAL} + OPG} \tag{41}$$

The total control loop transfer function H is equal to the power stage transfer function multiplied by the error amplifier transfer function.

$$H = G_{PS} \times H_{EA} \tag{42}$$

The bandwidth and phase margin can be read graphically from Bode plots of H_{EA} as shown in Figure 55.

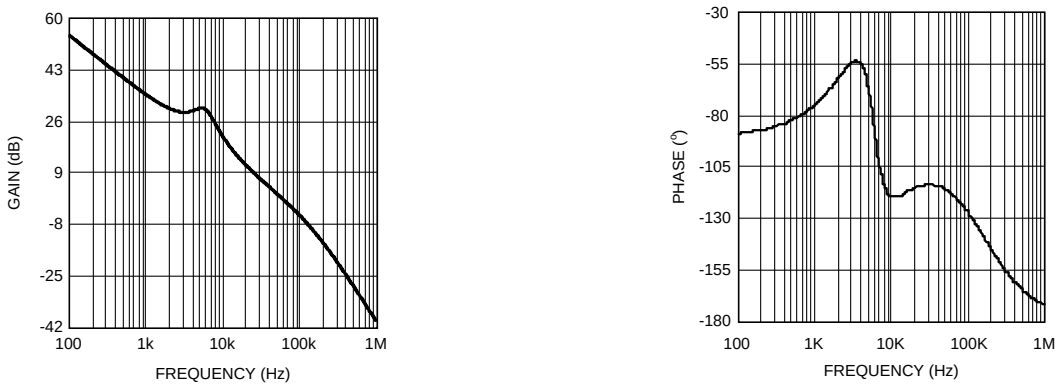

Figure 55. Overall Loop Gain and Phase

The bandwidth of this example circuit is 59 kHz, with a phase margin of 60°.

EFFICIENCY CALCULATIONS

The following is a sample calculation.

A reasonable estimation of the efficiency of a switching buck controller can be obtained by adding together the Output Power (P_{OUT}) loss and the Total Power loss (P_{LOSS}):

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \times 100\% \quad (43)$$

The Output Power (P_{OUT}) for the Typical Application Circuit design is (1.8V x 10A) = 18W. The Total Power (P_{LOSS}), with an efficiency calculation to complement the design, is shown below.

The majority of the power losses are due to the low side and high side MOSFET's losses. The losses in any MOSFET are switching (P_{SW}), conduction losses (P_{CND}), and gate charging losses (P_{GATE})

FET Switching Loss (P_{SW})

$$P_{SW} = P_{SW(ON)} + P_{SW(OFF)} \quad (44)$$

$$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \quad (45)$$

$$P_{SW} = 0.5 \times 5V \times 10A \times 300\ kHz \times 67\ ns \quad (46)$$

$$P_{SW} = 503\ mW \quad (47)$$

The Si4866DY has a typical turn-on rise time t_r and turn-off fall time t_f of 32 ns and 35 ns, respectively. The switching losses for the upper FET (Q1) is 0.503W. The low side FET (Q2) does not incur switching losses.

FET Conduction Loss (P_{CND})

$$P_{CND} = P_{CND1} + P_{CND2} \quad (48)$$

$$P_{CND1} = I^2_{OUT} \times R_{DS(ON)} \times k \times D \quad (49)$$

$$P_{CND2} = I^2_{OUT} \times R_{DS(ON)} \times k \times (1\text{-}D) \quad (50)$$

$R_{DS(ON)}$ = 4.5 mΩ and the k factor accounts for the increase in $R_{DS(ON)}$ due to heating. k = 1.3 at T_J = 100°C

$$P_{CND1} = (10A)^2 \times 4.5\ m\Omega \times 1.3 \times 0.36 \quad (51)$$

$$P_{CND2} = (10A)^2 \times 4.5\ m\Omega \times 1.3 \times (1 - 0.36) \quad (52)$$

$$P_{CND} = P_{CND1} + P_{CND2} \quad (53)$$

$$P_{CND} = 211\ mW + 374\ mW = 585\ mW \quad (54)$$

FET Gate Charging Loss (P_{GATE})

$$P_{GATE\_H} = n \times (V_{CC} - V_{D1}) \times Q_{GS} \times f_{SW} \quad (55)$$

$$P_{GATE\_L} = n \times V_{CC} \times Q_{GS} \times f_{SW} \quad (56)$$

$$P_{GATES} = [\ 1 \times (\ 5.0V - 0.4V\ ) \times 22\ nC \times 300\ kHz\ ] + [\ 1 \times (\ 5.0V\ ) \times 22\ nC \times 300\ kHz\ ] \quad (57)$$

$$P_{GATES} = 29\ mW + 33\ mW = 62\ mW \quad (58)$$

The value n is the total number of FETs used and Q_{GS} is the typical gate-source charge value, which is 21 nC. For the Si4866DY the gate charging loss is 62 mW.

Thus the total MOSFET losses are:

$$P_{FET} = P_{SW} + P_{CND} + P_{GATES} =$$

$$503\ mW + 585\ mW + 62\ mW \quad (59)$$

$$P_{FET} = 1.15\ W \quad (60)$$

There are few additional losses that are taken into account:

IC Loss (P_{IC})

$$P_{OP} = I_{Q\_VCC} \times V_{CC} \quad (61)$$

$$P_{DR} = [[\ (n \times Q_{GS} \times f_{SW}) / D] + [\ (n \times Q_{GS} \times f_{SW}) / (1\text{–}D)\ ]] \times V_{CC}$$

where

- P_{OP} is the operating loss
- P_{DR} is the driver loss
- $I_{Q\text{-}VCC}$ is the typical operating V_{CC} current (62)

$$P_{OP} = (\ 1.3\ mA \times 5.0V\ ) \quad (63)$$

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$$P_{DR} = [(1 \times 22\ nC \times 300\ kHz) / .36] + [(1 \times 22\ nC \times 300\ kHz) / .64] \times V_{CC} \quad (64)$$

$$P_{IC} = P_{OP} + P_{DR} \quad (65)$$

$$P_{IC} = 6.5\ mW + 137\ mW = 143.5\ mW \quad (66)$$

Input Capacitor Loss (P_{CAP})

$$P_{CAP} = \frac{(I_{RMS\_RIP})^2 \times ESR}{n} \quad (67)$$

where,

$$I_{RMS\_RIP} = I_{OUT} \times \sqrt{D(1 - D)} \quad (68)$$

Here n is the number of paralleled capacitors, ESR is the equivalent series resistance of each, and P_{CAP} is the dissipation in each. So for example if we use only one input capacitor of 10mΩ.

$$P_{CAP} = \frac{(4.8A)^2 \times 10\ m\Omega}{1} \quad (69)$$

$$P_{CAP} = 230\ mW \quad (70)$$

Output Inductor Loss (P_{IND})

$$P_{IND} = I^2_{OUT} \times DCR$$

where

- DCR is the DC resistance (71)

Therefore, for example

$$P_{IND} = (10A)^2 \times 3\ m\Omega \quad (72)$$

$$P_{IND} = 302\ mW \quad (73)$$

Total System Efficiency

$$P_{LOSS} = P_{FET} + P_{IC} + P_{CAP} + P_{IND} \quad (74)$$

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \times 100\% \quad (75)$$

$$\eta = \frac{18W}{18W + 1.83W} = 90.8\% \quad (76)$$

PCB LAYOUT CONSIDERATIONS

To produce an optimal power solution with the LM3743, good layout and design of the PCB are as important as component selection. The following are several guidelines to aid in creating a good layout. For an extensive PCB layout explanation refer to AN-1229 (SNVA054)

).

Separate Power Ground and Signal Ground

Good layout techniques include a dedicated ground plane, preferably on an internal layer. Signal level components like the compensation and feedback resistors should be connected to a section of this internal plane, signal ground. The signal ground section of the plane should be connected to the power ground at a single point. The best place to connect the signal ground and power ground is right at the GND pin of the IC.

Low Impedance Power Path

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The power path includes the input capacitors, power FETs, output inductor, and output capacitors. Keep these components on the same side of the PCB and connect them with thick traces or copper planes on the same layer. Vias add resistance and inductance to the power path, and have high impedance connections to internal planes than do top or bottom layers of a PCB. If heavy switching currents must be routed through vias and/or internal planes, use multiple vias in parallel to reduce their resistance and inductance. The power components must be kept close together. The longer the paths that connect them, the more they act as antennas, radiating unwanted EMI.

Minimize the Switch Node Copper

The plane that connects the power FETs and output inductor together radiates more EMI as it gets larger. Use just enough copper to give low impedance to the switching currents.

Kelvin Traces For Sense Lines

The drain and the source of the high-side FET should be connected as close as possible to the V_{CC} filter resistor (R6) and the SW pin and each pin should connect with a separate trace. The feedback trace should connect the positive node of the output capacitor and connect to the top feedback resistor (R2). Keep this trace away from the switch node and from the output inductor. If driving the COMP pin low with a signal BJT or MOSFET make sure to keep the signal transistor as close as possible to the pin and keep the trace away from EMI radiating nodes and components.

Example Circuit 1
LM3743-300, V_{IN} = 5V, V_{OUT} = 1.5V, I_{LOAD} = 20A

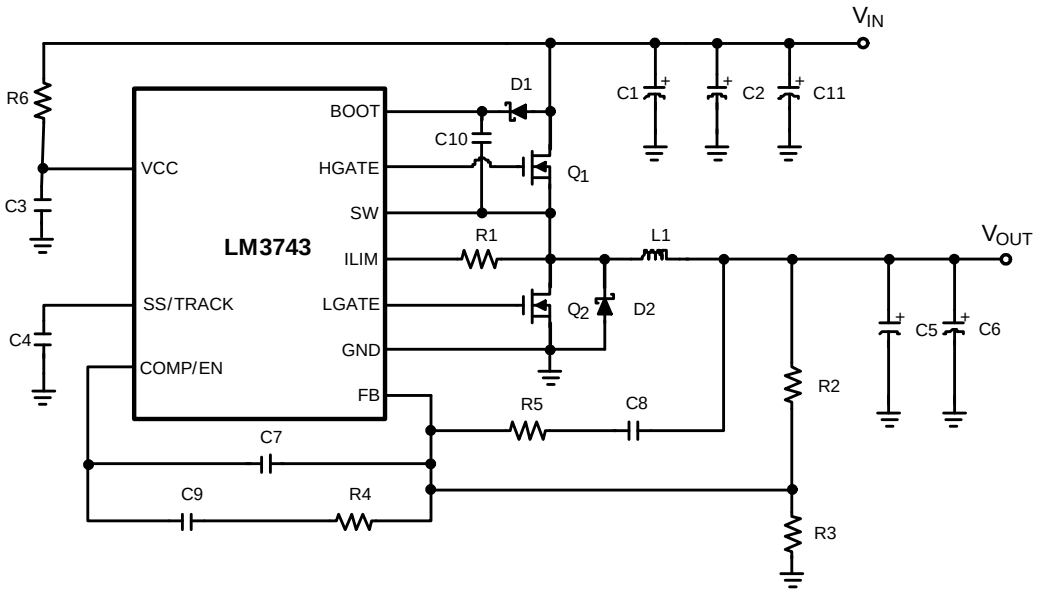

Figure 56. Schematic

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Designator(1)	Function	Description	Part Number	Vendor
U1	Controller	Buck Controller	LM3743VSSOP-10	Texas Instruments
C1	Input Filter	22µF,10V, X7R, 1210	1206ZD227MAT	AVX
C2, C11	Input Filter	POSCAP, 6V, 470µF	6TPD470M	Sanyo
C3	Decoupling	1µF, 10V, X7R, 0805	0805ZC105KAT	AVX
C4	Soft Start Cap	180nF, 25V, 0805	VJ0805Y184KXXA	Vishay
C5	Output Filter	680µF, 2.5V, 5mΩ	2R5TPD680M5	Sanyo
C6	Output Filter	150nF, 25V, 0805	VJ0805Y154KXXA	Vishay
C7	Comp Cap	22pF, 25V, 0603	VJ0603A220KXAA	Vishay
C8	Comp Cap	680pF, 25V, 0603	VJ0603A681KXAA	Vishay
C9	Comp Cap	1.5nF, 25V, 0603	VJ0603Y152KXXA	Vishay
C10	Bootstrap Cap	.47µF, 25V, 0805	VJ0805Y474KXXA	Vishay
R1	Current Limit Res	1.4k, 0603	CRCW06031401F	Vishay
R2	Top FB Resistor	24.9k, 0603	CRCW06032492F	Vishay
R3	Bottom FB Res	28k, 0603	CRCW06032802F	Vishay
R4	Comp Resistor	49.9k, 0603	CRCW06034992F	Vishay
R5	Comp Resistor	3.32k, 0603	CRCW06033321F	Vishay
R6	Vcc Filter Resistor	2 ohm, 0603	CRCW06032R00F	Vishay
L1	Output Filter	1.2µH, DCR = 2.9mΩ	SER2009-122ML	Coilcraft
D1	Bootstrap Diode	500mA, 20V, VF =.3V	MBR0520LT1	Onsemi
D2	LSPSD	IF=2A,VR=20V,VF =.3V	SL22	Vishay
Q1	Top FET	3.6mΩ@VGS=4.5V,24.5nC	Si7136DP	Vishay
Q2	Bottom FET	1.7mΩ@VGS=4.5V,61nC	Si7470DP	Vishay

(1) R3 = 7.87 kΩ (Vout = 3.3V), 11.5 kΩ (Vout = 2.5V), 19.6 kΩ (Vout = 1.8V), 28 kΩ (Vout = 1.5V), 49.9 kΩ (Vout = 1.2V), 100 kΩ (Vout = 1.0V), open (Vout = 0.8V)

Example Circuit
LM3743-300, V_{IN} = 3V to 5V, V_{OUT} = 1.5V, I_{LOAD} = 20A

In order to operate the LM3743 from an input voltage as low as 3V, the two components in the table below must replace the components found in the bill of materials above. Common loads requiring 20 A are digital rails for FPGAs, ASICs, and DSPs, and power distribution buses.

Designator	Function	Description	Part Number	Vendor
R1	Current Limit Res	1.5k, 0603	CRCW06031501F	Vishay
Q1	Top FET	4.5mΩ@VGS=4.5V,21nC	Si7882DP	Vishay

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	31

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3743MM-1000/NOPB	NRND	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SKNB	
LM3743MM-300/NOPB	NRND	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SKPB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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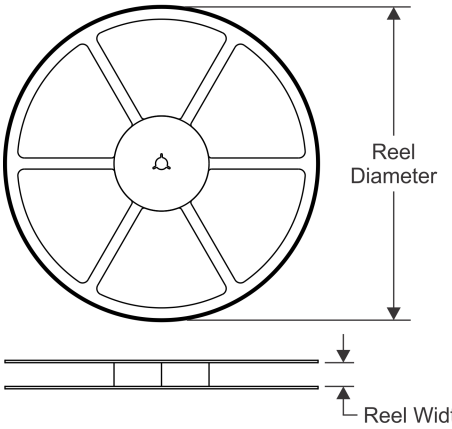
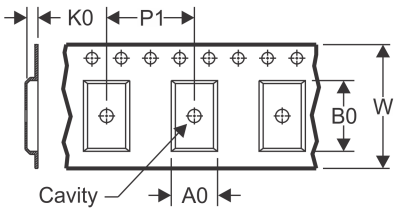
TAPE AND REEL INFORMATION

REEL DIMENSIONS

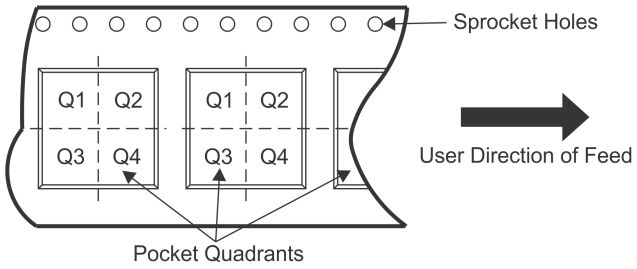


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

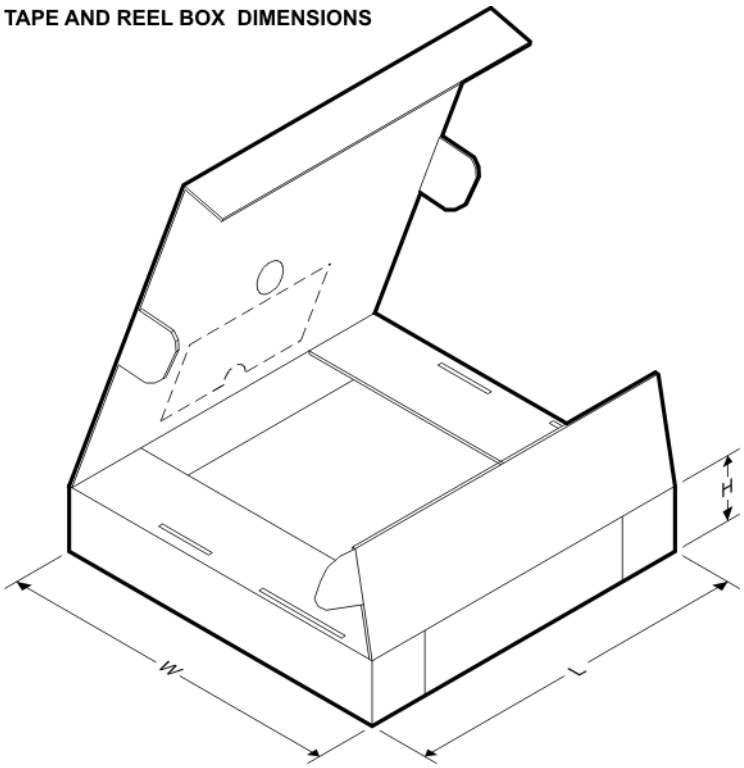
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3743MM-1000/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3743MM-300/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

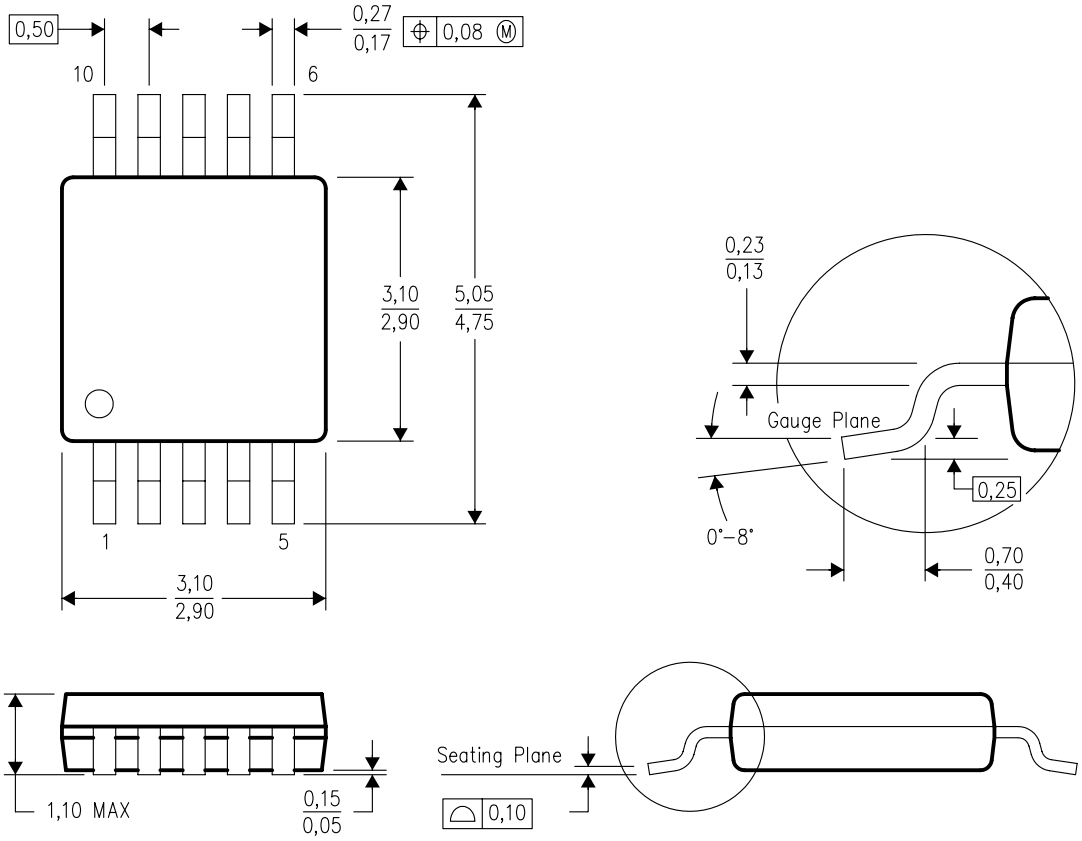
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3743MM-1000/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3743MM-300/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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