LM5007 High Voltage 80-V Step Down Switching Regulator

1 Features

- Integrated 80-V, 0.7-A N-Channel Buck Switch
- Internal HV V_{CC} Regulator
- No Control Loop Compensation Required
- Ultra-Fast Transient Response
- On Time Varies Inversely with Line Voltage
- Operating Frequency Nearly Constant with Varying Line Voltage
- Adjustable Output Voltage
- Highly Efficient Operation
- Precision Reference
- Low Bias Current
- Intelligent Current Limit Protection
- Thermal Shutdown
- External Shutdown Control
- VSSOP-8 and WSON-8 Packages

2 Applications

- Non-Isolated Buck Regulator
- Secondary High Voltage Post Regulator
- 42-V Automotive Systems

3 Description

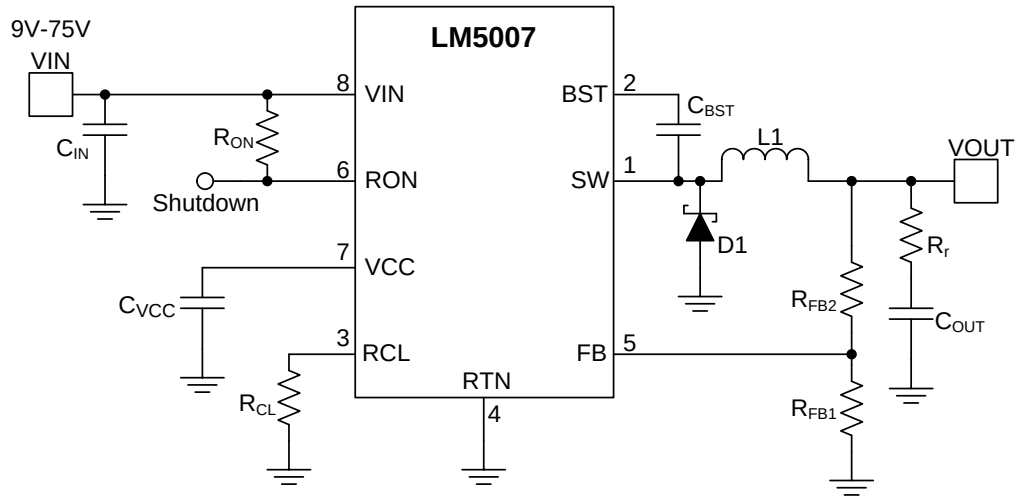
The LM5007 Step Down Switching Regulator features all of the functions needed to implement low cost, efficient, Buck bias regulators. This high voltage regulator contains an 80-V, 0.7-A N-Channel Buck Switch. The device is easy to apply and is provided in the VSSOP-8 and the thermally enhanced WSON-8 packages. The regulator is based on a hysteretic control scheme using an on time inversely proportional to V_{IN}. This feature allows the operating frequency to remain relatively constant with load and input voltage variations. The hysteretic control requires no control loop compensation, while providing very fast load transient response. An intelligent current limit is implemented in the LM5007 with forced off time that is inversely proportional to V_{OUT}. This current limiting scheme reduces load current foldback. Additional protection features include: Thermal Shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, and Max Duty Cycle limiter.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5007	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G — **Page**

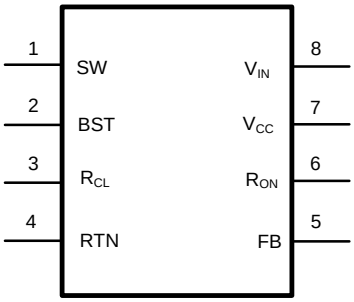
- Added *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Application Information*, *Design Requirements*, *Application Curves*, *Power Supply Recommendations*, *Layout*, and *Community Resources*. ... 1
- Added *Typical Application Schematic* ... 1
- Updated pinout drawing description ... 3

Changes from Revision E (March 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 11

5 Pin Configuration and Functions

DGK Package and NGT Package
8-Pin VSSOP and 8-Pin WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	SW	O	Switching Node	Power switching node. Connect to the LC output filter.
2	BST	I	Boost Boot–strap capacitor input	An external capacitor is required between the BST and the SW pins. A 0.01-µF ceramic capacitor is recommended. An internal diode between V_{CC} and BST completes the Buck gate drive bias network.
3	R_{CL}	I	Current Limit OFF time programming pin Toff = 10^{-5} / (0.59 + (FB / 7.22 x 10^{-6} x R_{CL}))	A resistor between this pin and RTN determines the variation of off time, along with the FB pin voltage, per cycle while in current limit. The off time is preset to 17 µS if FB =0 V and decreases as the FB pin voltage increases.
4	RTN	—	Circuit Ground	
5	FB	I	Feedback Signal from Regulated Output	This pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
6	R_{ON}	I	On time set pin Ton = 1.42 x 10^{-10} R_{ON} / V_{IN}	A resistor between this pin and V_{IN} sets the switch on time as a function of V_{IN}. The minimum recommended on time is 300 ns at the maximum input voltage.
7	V_{CC}	O	Output from the internal high voltage bias regulator. V_{CC} is nominally regulated to 7 V.	If an auxiliary voltage is available to raise the voltage on this pin, above the regulation set point (7V), the internal series pass regulator will shutdown, reducing the IC power dissipation. Do not exceed 14V. This output provides gate drive power for the internal Buck switch. An internal diode is provided between this pin and the BST pin. A local 0.1uF decoupling capacitor is recommended. Series pass regulator is current limited to 10mA.
8	V_{IN}	I	Input supply voltage	Recommended operating range: 9V to 75V.
—	EP	—	Exposed PAD, underside of the WSON package option	Internally bonded to the die substrate. Connect to GND potential for low thermal impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	V_{IN} to GND		80	V
	BST to GND		94	V
	SW to GND (Steady State)		–1	V
	BST to V_{CC}		80	V
	BST to SW		14	V
	V_{CC} to GND		14	V
	All other inputs to GND	–0.3	7	V
	Lead temperature (Soldering 4 sec)		260	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharge through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin. The machine model ESD compliance level for Pin 5 is 150 V. The human body ESD compliance level for Pin 7 and 8 is 1000 V.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	9		75	V
T_J	Junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM5007		UNIT
		DGK (VSSOP)	NGT (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.3	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.3	27.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	15.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.2	15.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

at T_J = 25°C, V_{IN} = 48 V (unless otherwise noted) (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} Regulator Output		6.6	7	7.4	V
	V_{CC} Current Limit(2)			11		mA
V_{CC} SUPPLY						
	V_{CC} undervoltage Lockout Voltage (V_{CC} increasing)			6.3		V
	V_{CC} Undervoltage Hysteresis			206		mV
	V_{CC} UVLO Delay (filter)			3		µs
	Operating Current (ICC)	Non-Switching, FB = 3 V		500	675	µA
	Shutdown/Standby Current	R_{ON} = 0 V		100	200	µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on)	I_{TEST} = 200 mA, VBST −VSW = 6.3 V(3)		0.74	1.34	Ω
	Gate Drive UVLO (VBST – VSW)	Rising	3.4	4.5	5.5	V
	Gate Drive UVLO Hysteresis			400		mV
	Breakdown voltage, V_{IN} to ground	T_J = 25°C	80			V
		T_J = -40°C to 125°C	76			V
	Breakdown voltage, BST to V_{CC}	T_J = 25°C	80			V
		T_J = -40°C to 125°C	76			V
CURRENT LIMIT						
	Current limit threshold		535	725	900	mA
	Current Limit Response Time	I_{switch} Overdrive = 0.1 A Time to Switch Off		225		ns
	OFF time generator (test 1)	FB=0V, RCL = 100K		17		µs
	OFF time generator (test 2)	FB=2.3V, RCL = 100K		2.65		µs
ON TIME GENERATOR						
	TON -1	V_{IN} = 10 V, R_{ON} = 200K	2.15	2.77	3.5	µs
	TON -2	V_{IN} = 75V, R_{ON} = 200K	290	390	490	ns
	Remote Shutdown Threshold	Rising	0.45	0.7	1.1	V
	Remote Shutdown Hysteresis			40		mV
MINIMUM OFF TIME						
	Minimum Off Timer	FB = 0V		300		ns
REGULATION AND OV COMPARATORS						
	FB Reference Threshold	Internal reference, Trip point for switch ON	2.445	2.5	2.550	V
	FB Over-Voltage Threshold	Trip point for switch OFF		2.875		V
	FB Bias Current			100		nA
THERMAL SHUTDOWN						
Tsd	Thermal Shutdown Temp.			165		°C
	Thermal Shutdown Hysteresis			25		°C

(1) All electrical characteristics having room temperature limits are tested during production with $T_A = T_J$ = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.
(3) For devices in the WSON-8 package, the Rds(on) limits are specified by design characterization data only.

6.6 Typical Characteristics

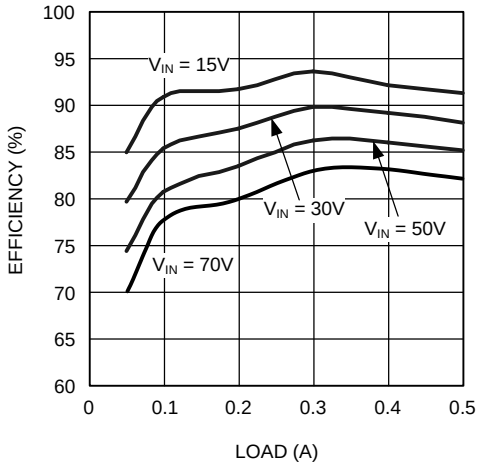


Figure 1. LM5007 10-V Output Efficiency

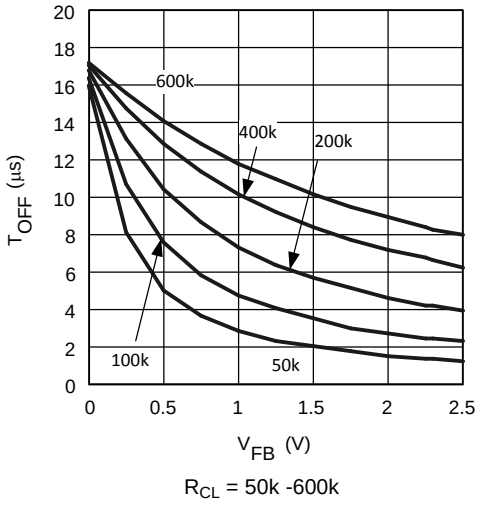


Figure 2. Current Limit V_{FB} vs T_{OFF}

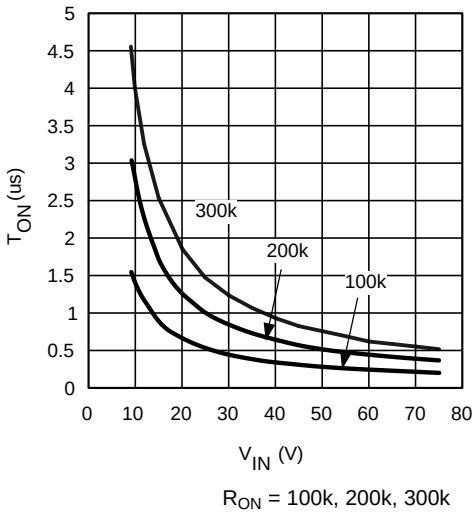


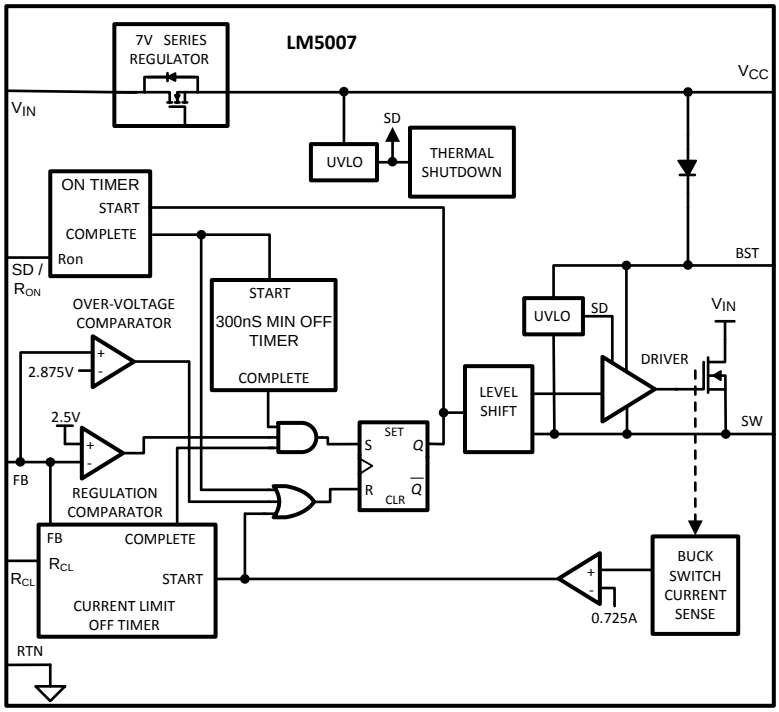
Figure 3. V_{IN} vs T_{ON}

7 Detailed Description

7.1 Overview

The LM5007 Step Down Switching Regulator features all of the functions needed to implement low cost, efficient, Buck bias regulators. This high voltage regulator contains an 80-V, 0.7-A N-Channel Buck Switch. The device is easy to apply and is provided in the VSSOP-8 and the thermally enhanced WSON-8 packages. The regulator is based on a hysteretic control scheme using an on time inversely proportional to V_{IN}. This feature allows the operating frequency to remain relatively constant with load and input voltage variations. The hysteretic control requires no control loop compensation, while providing very fast load transient response. An intelligent current limit scheme is implemented in the LM5007 with forced off time, after current limit detection, which is inversely proportional to V_{OUT}. This current limiting scheme reduces load current foldback. Additional protection features include: Thermal Shutdown, V_{CC} undervoltage lockout, Gate drive undervoltage lockout and Max Duty Cycle limiter. The LM5007 can be applied in numerous applications to efficiently regulate step down higher voltage inputs. This regulator is well suited for 48-V Telcom and the new 42-V Automotive power bus ranges.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit Overview

The LM5007 is a Buck DC-DC regulator that uses an on time control scheme. The on time is programmed by an external resistor and varies inversely with line input voltage (V_{IN}). The core regulation elements of the LM5007 are the feedback comparator and the on time one-shot. The regulator output voltage is sensed at the feedback pin (FB) and is compared to an internal reference voltage (2.5 V). If the FB signal is below the reference voltage, the buck switch is turned on for a fixed time pulse determined by the line voltage and a programming resistor (R_{ON}). Following the on period the switch will remain off for at least the minimum off timer period of 300 ns. If the FB pin voltage is still below the reference after the 300-ns off time, the switch will turn on again for another on time period. This switching behavior will continue until the FB pin voltage reaches the reference voltage level.

Feature Description (continued)

The LM5007 operates in discontinuous conduction mode at light load currents or continuous conduction mode at heavier load currents. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak value during the buck switch on time and then back to zero during the off time. The inductor current remains at zero until the next on time period starts when FB falls below the internal reference. In discontinuous mode the operating frequency can be relatively low and will vary with load. Therefore at light loads the conversion efficiency is maintained, since the switching losses decrease with the reduction in load current and switching frequency. The approximate discontinuous mode operating frequency can be calculated as follows:

$$F = \frac{V_{OUT}^2 \times L}{1 \times 10^{-20} \times R_{Load} \times (R_{ON})^2} \quad (1)$$

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated as follows:

$$F = \frac{V_{OUT}}{1.42 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage (V_{OUT}) can be programmed by two external resistors as shown in Figure 4. The regulation point can be calculated as follows:

$$V_{OUT} = 2.5 \times (R1 + R2) / R2 \quad (3)$$

The feedback comparator in hysteretic regulators depend upon the output ripple voltage to switch the output transistor on and off at regular intervals. In order for the internal comparator to respond quickly to changes in output voltage, proportional to inductor current, a minimum amount of capacitor Equivalent Series Resistance (ESR) is required. A ripple voltage of 25 mV to 50 mV is recommended at the feedback pin (FB) for stable operation. In cases where the intrinsic capacitor ESR is too small, additional series resistance may be added.

For applications where lower output voltage ripple is required the load can be connected directly to the low ESR output capacitor, as shown in Figure 4. The series resistor (R) will degrade the load regulation. Another technique for enhancing the ripple voltage at the FB pin is to place a capacitor in parallel with the feedback divider resistor R1. The addition of the capacitor reduces the attenuation of the ripple voltage from the feedback divider

7.3.2 High Voltage Bias Regulator

The LM5007 contains an internal high voltage bias regulator. The input pin (V_{IN}) can be connected directly to line voltages from 9 V to 75 V. To avoid supply voltage transients due to long lead inductances on the input pin (V_{IN} Pin 8), it is always recommended to connect low ESR ceramic chip capacitor (≅ 0.1 µF) between V_{IN} pin and *RTN* pin (pin 4), located close to LM5007. The regulator is internally current limited to 10 mA. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. When the voltage on the V_{CC} pin reaches the regulation point of 7 V, the controller output is enabled.

An external auxiliary supply voltage can be applied to the V_{CC} pin. If the auxiliary voltage is greater than 7 V, the internal regulator will essentially shutoff, thus reducing internal power dissipation.

Feature Description (continued)

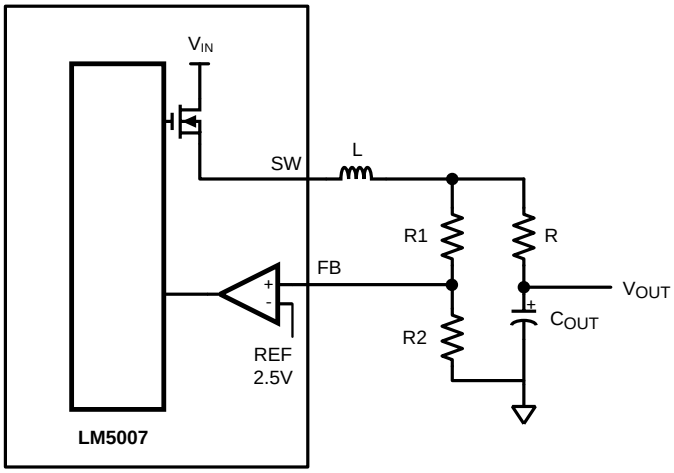


Figure 4. Low Ripple Output Configuration

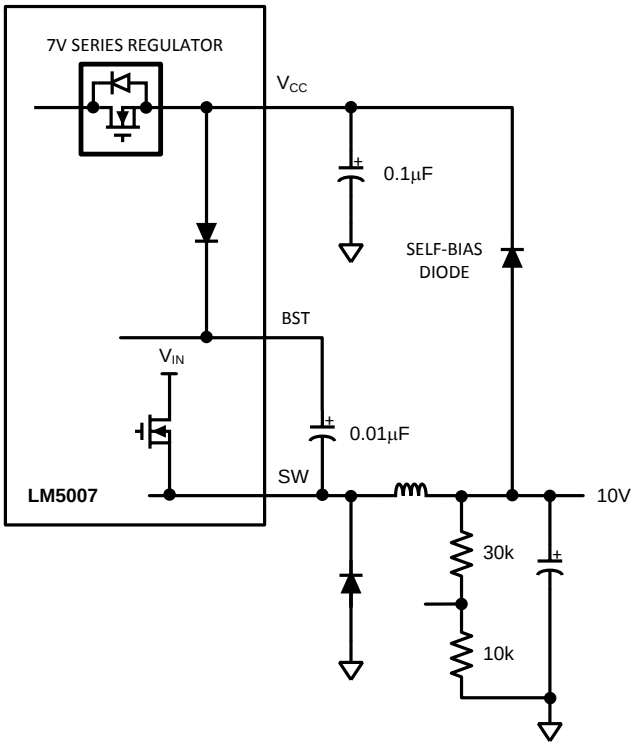


Figure 5. Self Biased Configuration

7.3.3 Over-Voltage Comparator

The over-voltage comparator is provided to protect the output from overvoltage conditions due to sudden input line voltage changes or output loading changes. The over-voltage comparator monitors the FB pin versus an internal 2.875V reference (OV_REF). If the voltage at FB rises above OV_REF the comparator immediately terminates the buck switch on time pulse.

Feature Description (continued)

7.3.4 ON Time Generator and Shutdown

The on time of the LM5007 is set inversely proportional to the input voltage by an external resistor connected between R_{ON} and V_{IN}. The R_{ON} terminal is a low impedance input biased at approximately 1.5 V. Thus the current through the resistor and into the R_{ON} terminal is approximately proportional to V_{IN} and used internally to control the on timer. This scheme of input voltage feed-forward hysteretic operation achieves nearly constant operational frequency over varying line and load conditions. The on time equation for the LM5007 is:

$$Ton = 1.42 \times 10^{-10} \times R_{ON} / V_{IN} \quad (4)$$

The R_{ON} pin of the LM5007 also provides a shutdown function which disables the regulator and significantly decreases quiescent power dissipation. By pulling the R_{ON} pin to below 0.7V logic threshold activates the low power shutdown mode. The V_{IN} quiescent current in the shutdown mode is approximately 100µA internal to the LM5007 plus the current in the R_{ON} resistor.

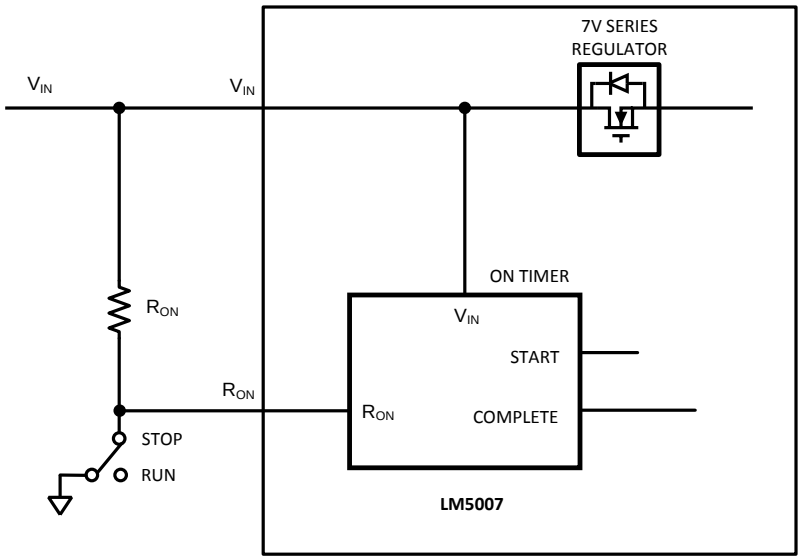


Figure 6. Shutdown Implementation

7.3.5 Current Limit

The LM5007 contains an intelligent current limit off timer intended to reduce the foldback characteristic inherent with fixed off-time over-current protection. If the current in the Buck switch exceeds 725 mA the present cycle on time is immediately terminated (cycle by cycle current limit). Following the termination of the cycle a non-resetable current limit off timer is initiated. The duration of the off time is a function of the external resistor (R_{CL}) and the FB pin voltage. When the FB pin voltage equals zero, the current limit off time is internally preset to 17 uS. This condition occurs in short circuit operation when a maximum amount of off time is required.

In cases of overload (not complete short circuit) the current limit off time can be reduced as a function of the output voltage (measured at the FB pin). Reducing the off time with smaller overloads reduces the amount of foldback and also reduces the initial start-up time. The current limit off time for a given FB pin voltage and R_{CI} resistor can be calculated by the following equation:

$$T_{OFF} = \frac{10^{-5}}{0.59 + \frac{V_{FB}}{\left(7.22 \times 10^{-6} \times R_{CL}\right)}} \quad (5)$$

Applications utilizing low resistance inductors and/or a low voltage drop rectifier may require special evaluation at high line, short circuit conditions. In this special case the preset 17µs (FB = 0V) off time may be insufficient to balance the inductor volt*time product. Additional inductor resistance, output resistance or a larger voltage drop rectifier may be necessary to balance the inductor cycle volt*time product and limit the short circuit current.

Feature Description (continued)

7.3.6 N-Channel Buck Switch and Driver

The LM5007 integrates an N-Channel Buck switch and associated floating high voltage gate driver. This gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. The bootstrap capacitor is charged by V_{CC} through the internal high voltage diode. A 0.01-µF ceramic capacitor connected between the BST pin and SW pin is recommended.

During each cycle when the Buck switch turns off, the SW pin is approximately 0 V. When the SW pin voltage is low, the bootstrap capacitor will be charged from V_{CC} through the internal diode. The minimum off timer, set to 300 ns, ensures that there will be a minimum interval every cycle to recharge the bootstrap capacitor.

An external re-circulating diode from the SW pin to ground is necessary to carry the inductor current after the internal Buck switch turns off. This external diode must be of the Ultra-fast or Schottky type to reduce turn-on losses and current over-shoot. The reverse voltage rating of the re-circulating diode must be greater than the maximum line input voltage.

7.3.7 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When thermal protection is activated, typically at 165 degrees Celsius, the controller is forced into a low power reset state, disabling the output driver. This feature is provided to prevent catastrophic failures from accidental device overheating.

7.3.8 Minimum Load Current

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor may discharge during the long off-time, and the circuit will either shutdown, or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, the feedback resistors should be chosen low enough in value so they provide the minimum required current at nominal V_{out}.

7.3.9 Ripple Configuration

LM5007 uses Constant-On-Time (COT) control in which the on-time is terminated by an on-timer and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be larger than any noise component present at the feedback node.

Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

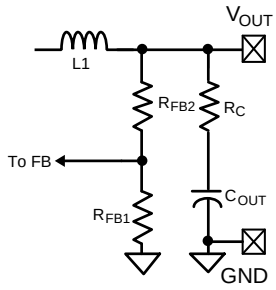
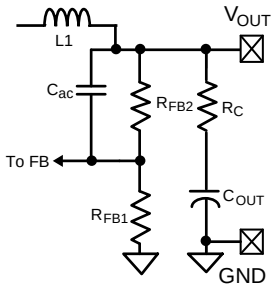
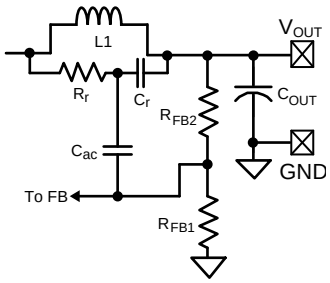
1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details for each ripple generation method.

Feature Description (continued)

Table 1. Ripple Configuration

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		
$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ (6)	$C \geq \frac{5}{f_{sw}(R_{FB2} \| \| R_{FB1})}$ $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$ (7)	$C_r = 3300\ pF$ $C_{ac} = 100\ nF$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$ (8)

7.4 Device Functional Modes

7.4.1 Standby Mode with V_{IN}

The LM5007 is intended to operate with input voltages above 9 V. The minimum operating input voltage is determined by the V_{CC} undervoltage lockout threshold of 6.3 V (typ). If V_{IN} is too low to support a V_{CC} voltage greater than the V_{CC} UVLO threshold, the controller switches to the standby mode with the buck switch in the off state.

7.4.2 RT Shutdown Mode

The LM5007 is in shutdown mode when the R_{ON} pin is pulled below 0.7 V (typ). In this mode, the buck FET is held off and the V_{CC} regulator is disabled.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5007 is a step down converter DC-DC converter. The LM5007 device is step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 500 mA. Use the following design procedure to select component values for the LM5007 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic of an LM5007 based buck converter is shown in Figure 7. For an output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (see *Electrical Characteristics*), the V_{CC} pin can be supplied from V_{OUT} through a diode for higher efficiency and lower power dissipation in the IC.

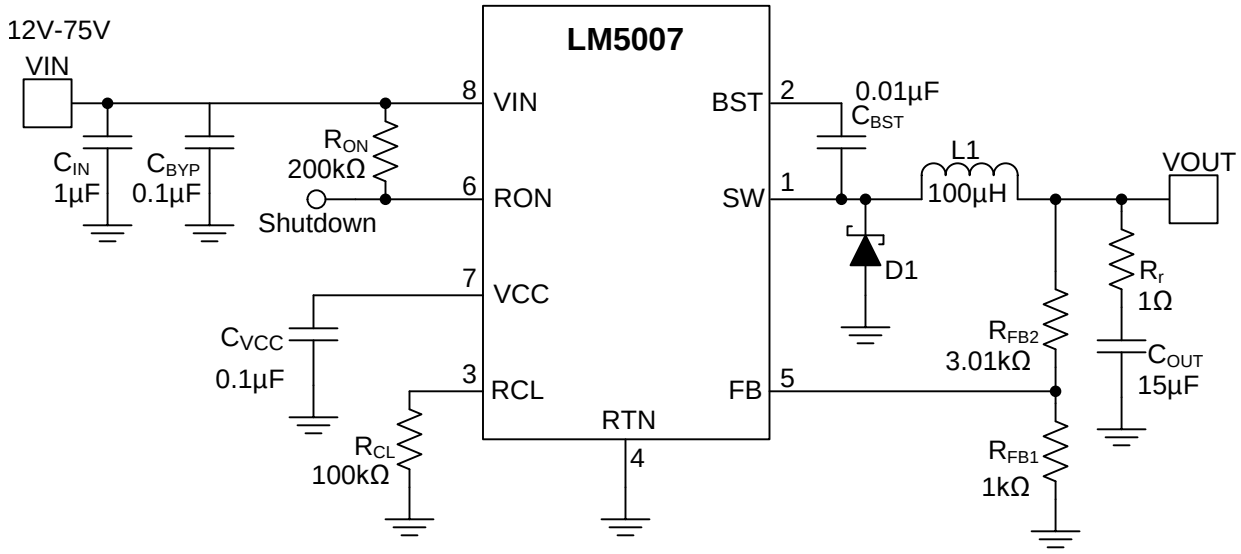


Figure 7. 12-V to 75-V Input and 10-V, 400-mA Output Buck Converter

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
Input Voltage	15 V to 75 V
Output Voltage	10 V
Maximum Output Current	400 mA
Nominal Switching Frequency	380 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 R_{FB2} and R_{FB1}

$V_{OUT}=V_{FB}$ x (R_{FB2}/R_{FB1}+1), and since V_{FB}=2.5 V in regulation, ratio of R_{FB2} to R_{FB1} is 3:1. Select standard values of R_{FB1}=1 kΩ and R_{FB2}=3.01 kΩ. Other values can be chosen as long as the 3:1 ratio is maintained.

8.2.2.2 Frequency Selection

The switching frequency is set by R_{ON} resistor using Equation 9.

$$R_{ON} = \frac{V_{OUT}}{1.42 \times 10^{-10} \times f_{sw}} \tag{9}$$

Selecting f_{sw} = 380 kHz results in R_{ON}=185 kΩ. A standard value of 200 kΩ is selected for this design.

8.2.2.3 Inductor Selection

The inductor is selected to provide a current ripple of 40-50% of the full load current. In addition, the peak inductor current at maximum load must be smaller than the minimum current limit threshold provided in *Electrical Characteristics*. The inductor current ripple is given by Equation 10.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{10}$$

The maximum ripple is observed at the maximum input voltage. Using V_{IN}=75 V and ΔI_L=50% x $I_{OUT(max)}$ results in L1=114 µH. A standard value of 100 µH is chosen. With this L1, the inductor current ripple ranges from 88 mA to 228 mA. The peak inductor and switch current at full load is given by Equation 11.

$$I_{L1} = I_{OUT} + \frac{\Delta I_L}{2} \tag{11}$$

At maximum V_{IN}, the peak inductor current is 514 mA, which is lower than the minimum current limit threshold of 535 mA. The selected inductor should be able to operate at the maximum current limit of 900 mA during startup and overload conditions without saturating.

8.2.2.4 Output Capacitator

The output capacitor is selected to minimize the capacitive ripple. The maximum ripple is observed at the maximum input voltage and is given by:

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{COUT}} \tag{12}$$

Where, ΔVC_{OUT} is the voltage ripple across the capacitor and ΔIL is the peak-to-peak inductor current ripple.

Substituting V_{IN}=75 V and targeting ΔV_{COUT}=10 mV gives C_{OUT}=7.5 µF. A standard 15-µF value is selected for C_{OUT}. An X5R or X7R type capacitor with a voltage rating of 16 V or higher should be selected.

8.2.2.5 Type I Ripple Circuit

Type I ripple circuit, as described in ripple configuration, is chosen for this example. For a constant on time converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on C_{OUT}.

Using type I ripple circuit equations with minimum FB pin ripple of 25 mV, the values of series resistor RC is calculated using Equation 13:

$$R_C = \frac{25\ mV}{\Delta I_{L(MIN)}} \times \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \tag{13}$$

to be 1.1 Ω. A standard value of 1 Ω is selected.

8.2.2.6 Input Capacitator

Input capacitor should be large enough to limit the input voltage ripple which can be calculated using the Equation 14.

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{f_{SW} \times \Delta V_{CIN}} \quad (14)$$

The input ripple reaches its maximum at D=0.5. Targeting a ΔVCIN = 0.5 V at using a duty cycle of D=0.5 results in CIN=0.526 µF. A standard value of 1µF is selected. The input capacitor should be rated for the maximum input voltage under all conditions. A 100-V, X7R type capacitor is selected for this design. The input capacitor should be placed close to the V_{IN} pin and the anode of the diode (D1) as it supplies high frequency switching current.

A 0.1-µF bypass capacitor (CBYP) should be placed very close to V_{IN} and RTN pins of ICs of the IC to avoid the supply voltage transients and ringing between V_{IN} and RTN.

8.2.2.7 R_{CL}

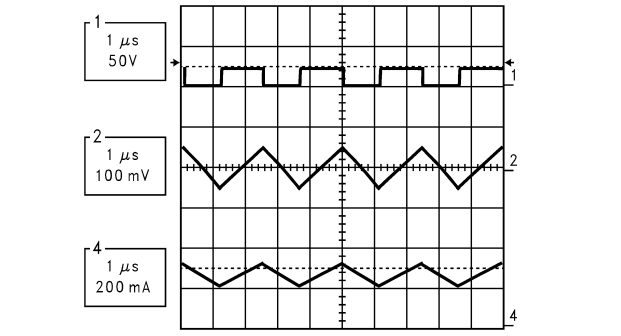
The current limit off-time is set by R_{CL} according to Equation 5. The usable values tend to be in the range of 100k Ω to 1 MΩ. The off time required for volt-second balance on the inductor in current limit is given by Equation 15.

$$T_{OFF(ILIM)} = \frac{V_{IN(MAX)} \times 225\ ns}{V_F + V_{OUT} + I_{LIM} \times r_L} \quad (15)$$

where 225 ns is the current limit response time, V_F is the forward voltage drop of the rectifier diode. V_{OUT} is the output voltage, I_{LIM} is the current limit, and r_L is the inductor resistance.

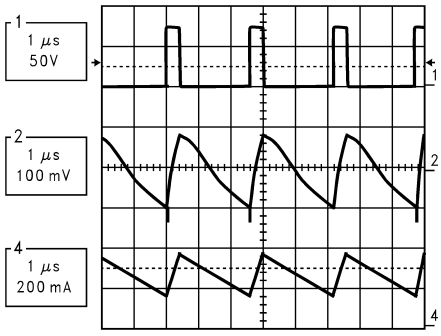
The programmed current limit off-time should be higher than the off-time needed for voltage second balance on the inductor. For a short at the output (V_{OUT}=0 V), and V_F=0.7 V, an inductor DCR of 390 mΩ or higher is needed to achieve volt-second balance in the maximum programmed current limit off-time of 17 µs. Using Equation 5 an R_{CL} of greater than 10 kΩ can be used. A conservative value of 100 kΩ is selected in this design.

8.2.3 Application Curves



V_{OUT} = 10 V
CH1: Switch Node
V_{IN} = 20 V
CH2: V_{OUT} (AC)
I_{OUT} = 250 mA
CH4: Inductor Current

Figure 8. Operational Waveforms: LM5007 Operation



V_{OUT} = 10 V
CH1: Switch Node
V_{IN} = 75 V
CH2: V_{OUT} (AC)
I_{OUT} = 250 mA
CH4: Inductor Current

Figure 9. Operational Waveforms: LM5007 Operation

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 9 V and 75 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required at the input terminals of the converter in addition to the calculated values to limit the inductive spikes due to the input cables or wires.

10 Layout

10.1 Layout Guidelines

Layout considerations are critical for optimum performance:

- FB node trace should be away from noise sources and inductors. The lower feedback resistor should connect to ground close to the IC RTN.
- SW pin copper area should be minimize to reduce dv/dt noise.
- The area of the high di/dt loop consisting of V_{IN} bypass capacitor, SW node, and diode rectifier should be minimized.
- The V_{IN}-RTN bypass capacitor and the V_{CC}-TRN bypass capacitors should be as close to the IC as possible.

If the internal dissipation of the LM5007 produces excessive junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PC board, and that plane should extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PC board traces, where possible, can also help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

10.2 Layout Example

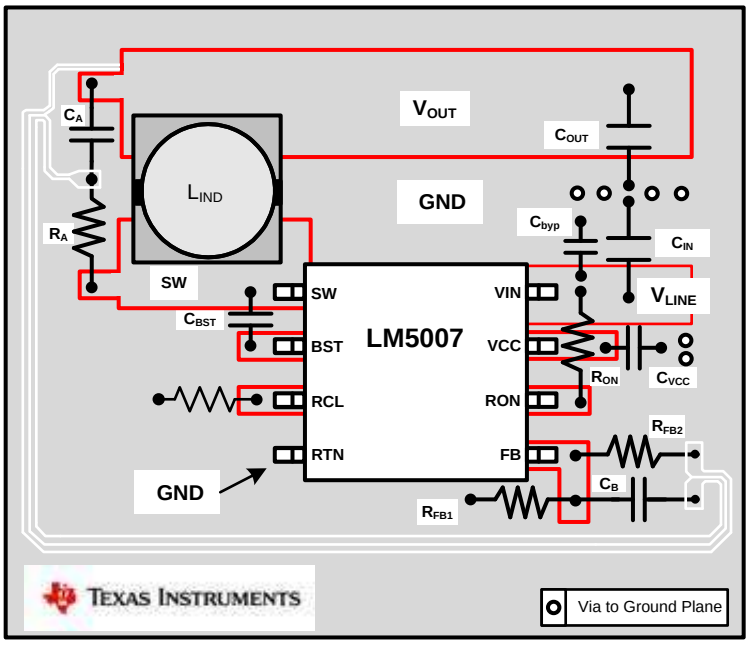


Figure 10. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5007MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	S81B	
LM5007MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S81B	Samples
LM5007MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S81B	Samples
LM5007SD	NRND	WSON	NGT	8	1000	TBD	Call TI	Call TI	-40 to 125	L00031B	
LM5007SD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L00031B	Samples
LM5007SDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L00031B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

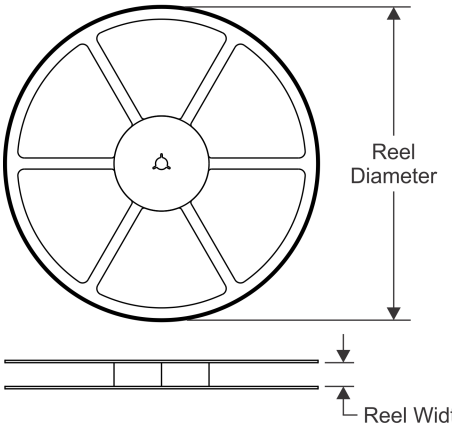
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

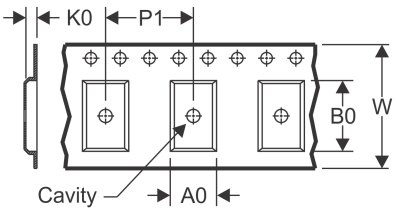
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

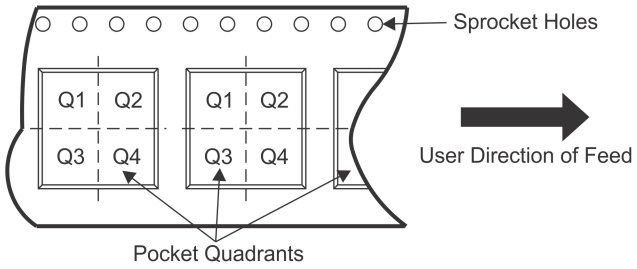


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

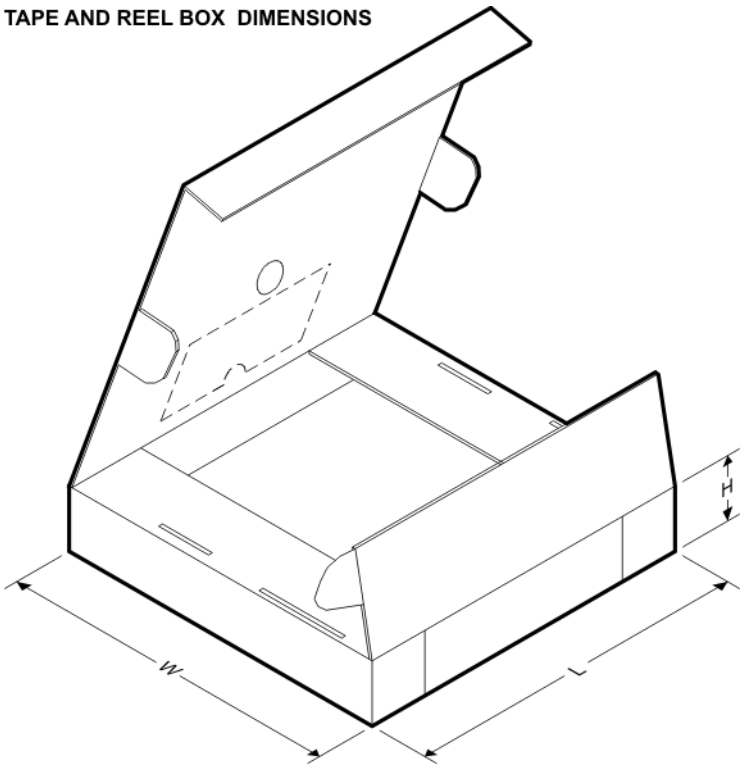
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5007MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5007MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5007MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5007SD	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5007SD/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5007SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

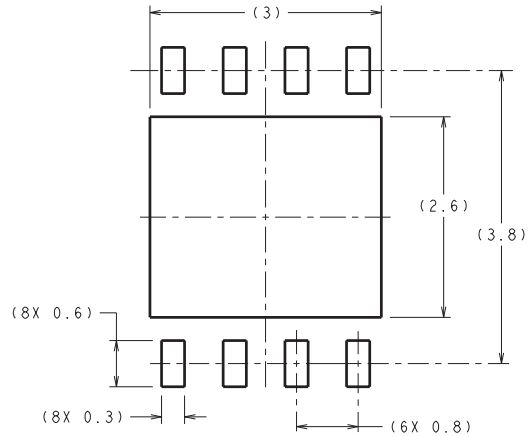
TAPE AND REEL BOX DIMENSIONS



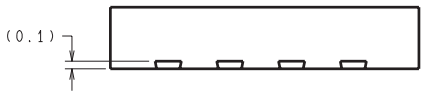
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5007MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5007MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5007MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5007SD	WSON	NGT	8	1000	210.0	185.0	35.0
LM5007SD/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LM5007SDX/NOPB	WSON	NGT	8	4500	346.0	346.0	35.0

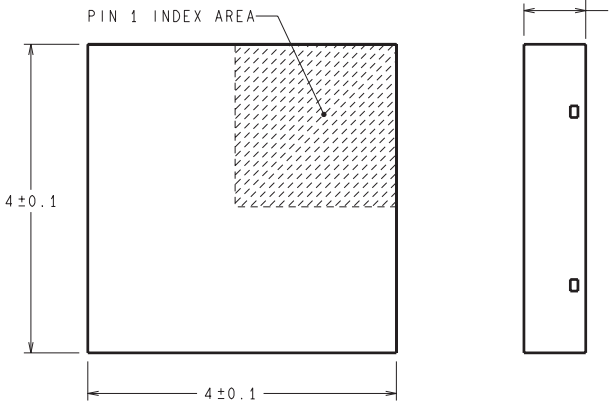
NGT0008A

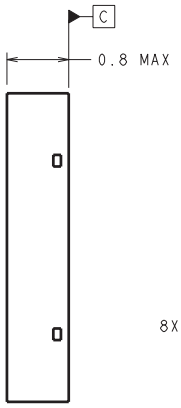


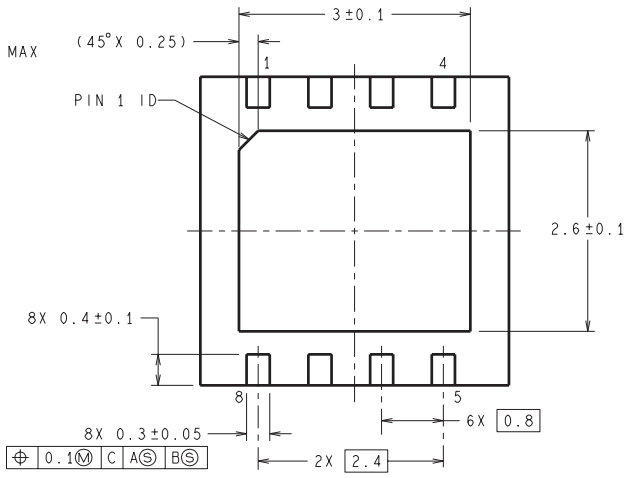
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

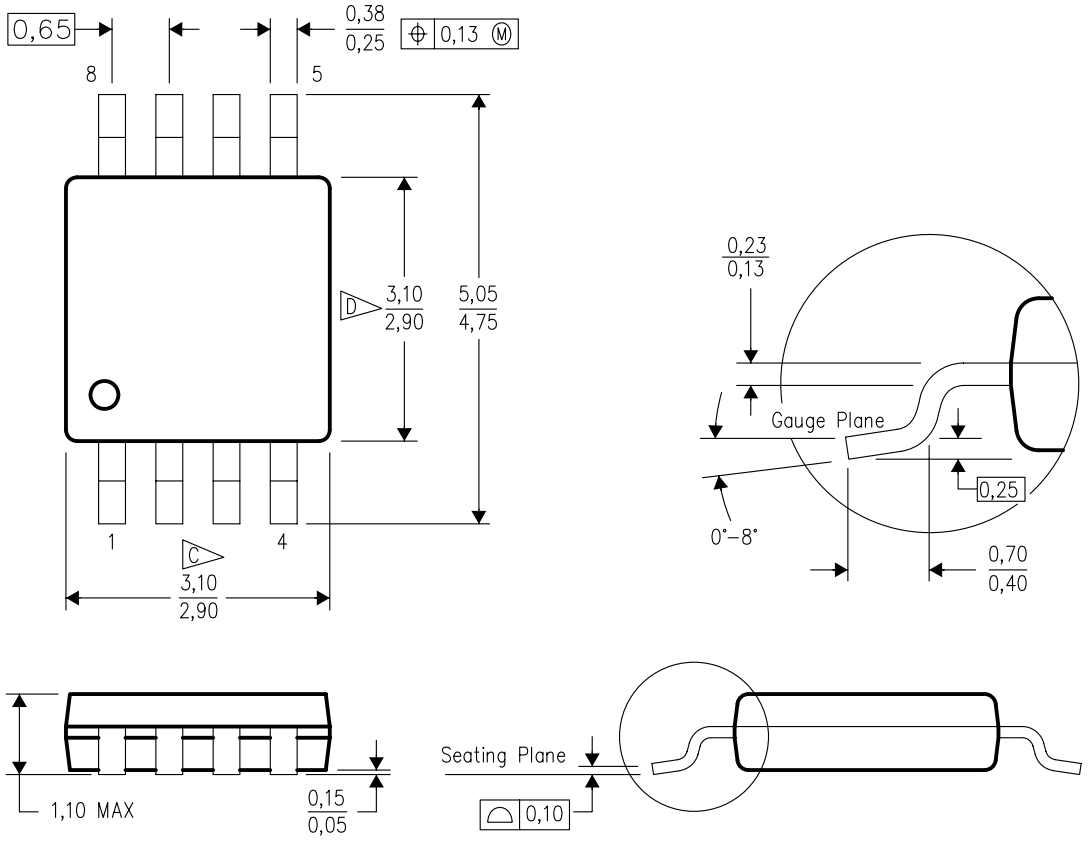






SDC08A (Rev A)

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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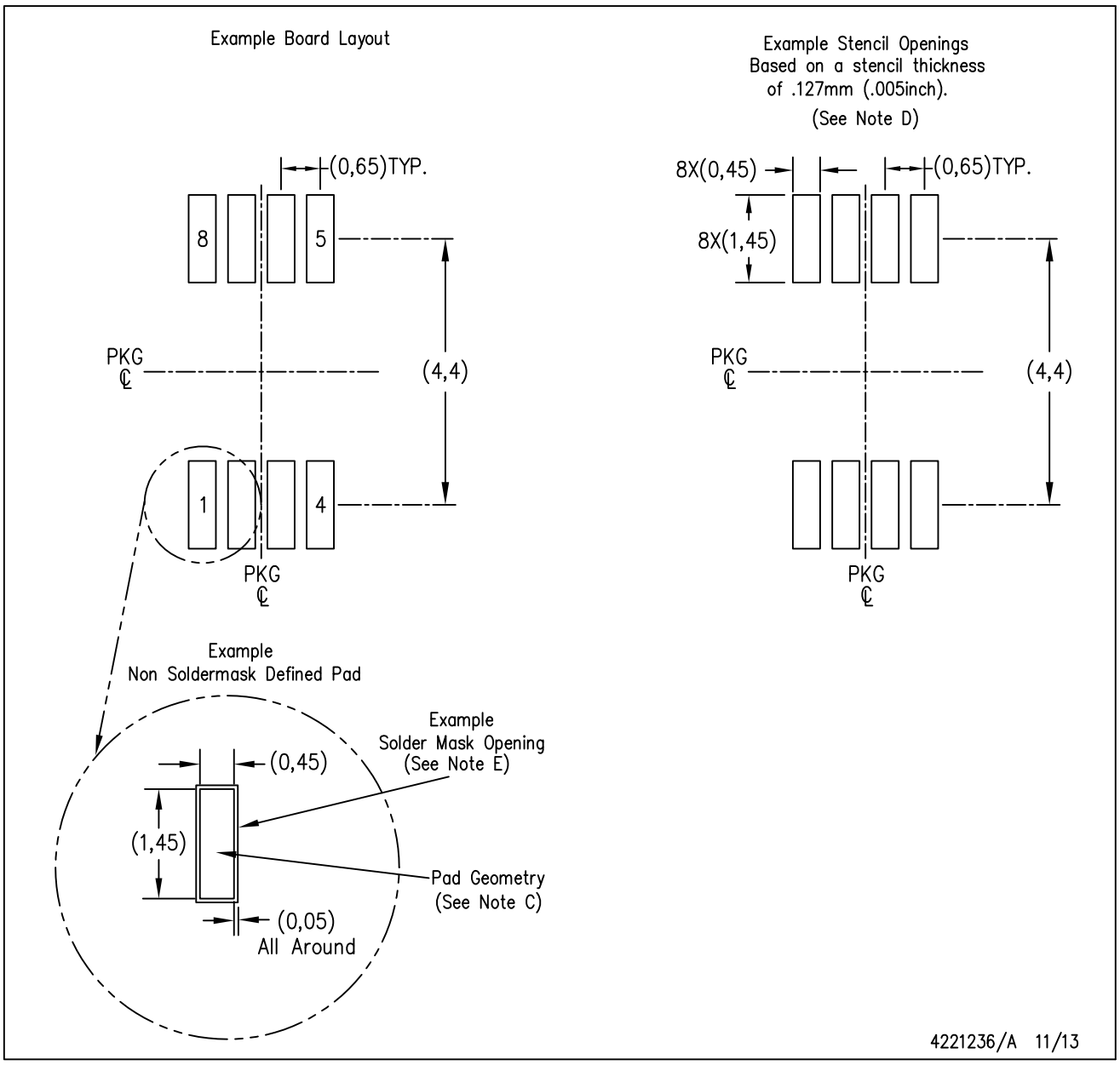
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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