LM614 Quad Operational Amplifier and Adjustable Reference

Check for Samples: LM614

FEATURES

Op Amp

- **Low Operating Current: 450µA**
- **Wide Supply Voltage Range: 4V to 36V**
- **Wide Common-Mode Range: V^- to (V^+ − 1.8V)**
- **Wide Differential Input Voltage: ±36V**

Reference

- **Adjustable Output Voltage: 1.2V to 5.0V**
- **Initial Tolerance: ±2.0%**
- **Wide Operating Current Range: 17µA to 20mA**
- **Tolerant of Load Capacitance**

APPLICATIONS

- **Transducer Bridge Driver and Signal Processing**
- **Process and Mass Flow Control Systems**
- **Power Supply Voltage Monitor**
- **Buffered Voltage References for A/D's**

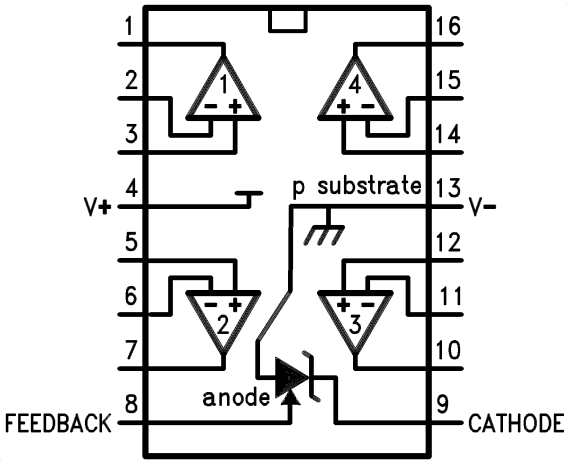
DESCRIPTION

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), initial tolerance (2.0%), and the ability to be programmed from 1.2V to 5.0V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of TI's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Connection Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Voltage on Any Pins except V_R (referred to V^- pin)		36V (Max)(3) −0.3V (Min)(4)
Current through Any Input Pin & V_R Pin		±20
Differential Input Voltage	LM614I	±36V
	LM614C	±32V
Storage Temperature Range		$-65°C \le T_J \le +150°C$
Maximum Junction Temperature		150°C
Thermal Resistance, Junction-to-Ambient(5)		150°C
Soldering Information (Soldering, 10 sec.)		220°C
ESD Tolerance(6)		±1kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Input voltage above V+ is allowed.
(4) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V−, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
(5) Junction temperature may be calculated using TJ = TA + P DθjA. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θjA is 90°C/W for the DW package.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Temperature Range

LM614I	$-40°C \le T_J \le +85°C$
LM614C	$0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **Boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typ(1)	LM614I LM614C Limits(2)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM614C)	450 **550**	1000 **1070**	µA max µA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	V min V min
			46 **43**	32 **32**	V max V max
OPERATIONAL AMPLIFIER					
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM614C)	1.5 **2.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.8V$), V^+ = 30V	1.0 **1.5**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	See (2)	**15**		µV/°C max
I_B	Input Bias Current		10 **11**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	nA max nA max

(1) Typical values in standard typeface are for TJ = 25°C; values in boldface type apply for the full operating temperature range. These values represent the most likely parametric norm.
(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Electrical Characteristics (continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **Boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typ(1)	LM614I LM614C Limits(2)	Units
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**		pA/°C
R_{IN}	Input Resistance	Differential	1800		MΩ
		Common-Mode	3800		MΩ
C_{IN}	Input Capacitance	Common-Mode Input	5.7		pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74		nV/√Hz
I_n	Current Noise	f = 100 Hz, Input Referred	58		fA/√Hz
CMRR	Common-Mode	V^+ = 30V, 0V ≤ V_{CM} ≤ (V^+ − 1.8V),	95	75	dB min
	Rejection Ratio	CMRR = 20 log ($\Delta V_{CM}/\Delta V_{OS}$)	**90**	**70**	dB min
PSRR	Power Supply	4V ≤ V^+ ≤ 30V, V_{CM} = V^+/2,	110	75	dB min
	Rejection Ratio	PSRR = 20 log ($\Delta V^+/\Delta V_{OS}$)	**100**	**70**	dB min
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	94 **40**	V/mV min
SR	Slew Rate	V^+ = 30V(3)	±0.70 **±0.65**	±0.50 **±0.45**	V/µs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.52**		MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V for LM614C)	V^+ − 1.4 **V^+ − 1.6**	V^+ − 1.8 **V^+ − 1.9**	V min V min
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V for LM614C)	V^- + 0.8 **V^- + 0.9**	V^- + 0.95 **V^- + 1.0**	V max V max
I_{OUT}	Output Source	V_{OUT} = 2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	25 **15**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source	30 **40**	50 **60**	mA max mA max
		V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink	30 **32**	70 **90**	mA max mA max
VOLTAGE REFERENCE					
V_R	Voltage Reference	See (4)	1.244	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	See (5)	**10**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	See (6)	**3.2**		µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$(7)	1.5 **2.0**	5 **5.5**	mV max mV max

(3) Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

(4) V_R is the Cathode-feedback voltage, nominally 1.244V.

(5) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \cdot \Delta V_R/(V_{R[25°C]} \cdot \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is ensured by design and sample testing.

(6) Hysteresis is the change in V_R caused by a change in T_J, after the reference has been “dehysterized”. To dehysterize the reference; that is minimize the hysteresis to the typical value, cycle its junction temperature in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

(7) Low contact resistance is required for accurate measurement.

Electrical Characteristics (continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **Boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typ[1]	LM614I LM614C Limits[2]	Units
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA	**0.2**	**0.56**	Ω max
		$\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 µA	**0.6**	**13**	Ω max
$\frac{\Delta V_R}{AV_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 5.0V)}$ (3.76V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V+}$	V_R Change with V^+ Change	$V_{R(V+ = 5V)} - V_{R(V+ = 36V)}$ (V^+ = 32V for LM614C)	0.1 **0.1**	1.2 **1.3**	mV max mV max
		$V_{R(V+ = 5V)} - V_{R(V+ = 3V)}$	0.01 **0.01**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz, $V_{RO} = V_R$	30		μV_{RMS}

Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs Temperature on 5 Representative Units

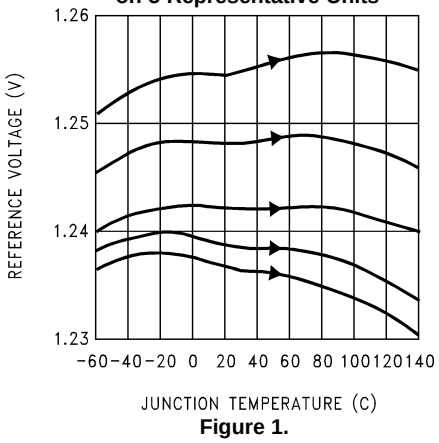


Figure 1.

Reference Voltage Drift

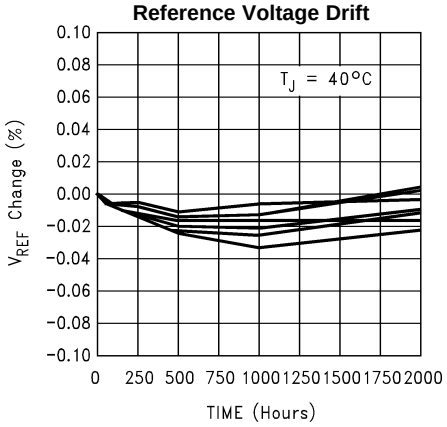


Figure 2.

Accelerated Reference Voltage Drift vs. Time

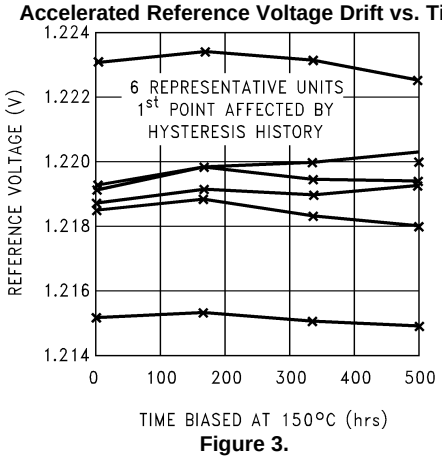


Figure 3.

Reference Voltage vs. Current and Temperature

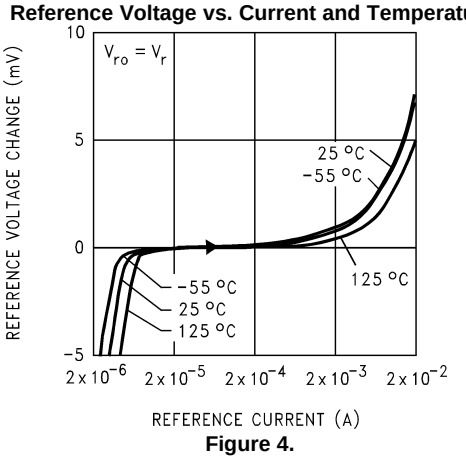


Figure 4.

Reference Voltage vs. Current and Temperature

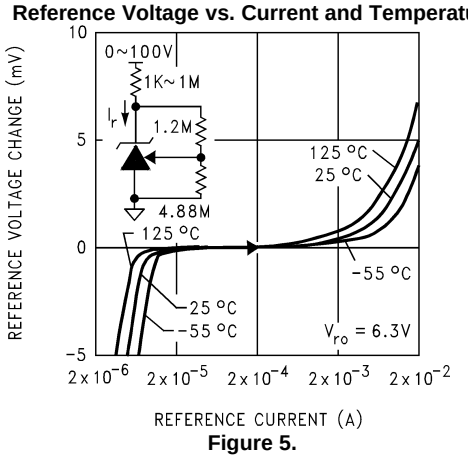


Figure 5.

Reference Voltage vs. Reference Current

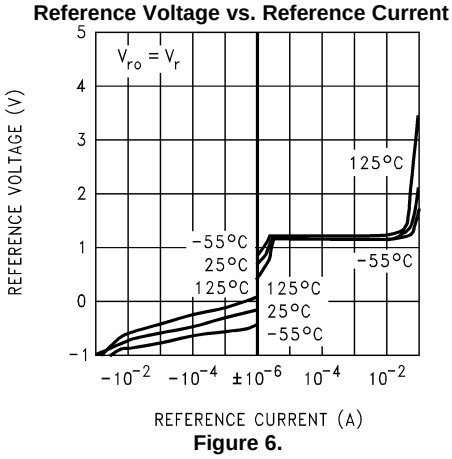


Figure 6.

Typical Performance Characteristics (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs. Reference Current

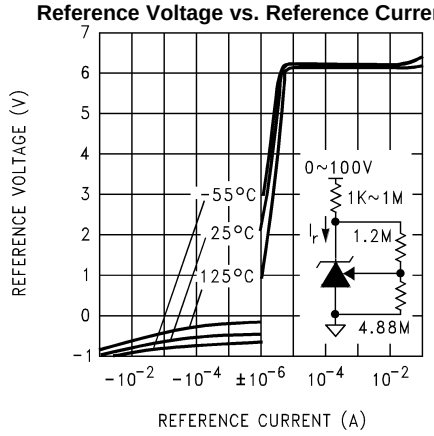


Figure 7.

Reference AC Stability Range

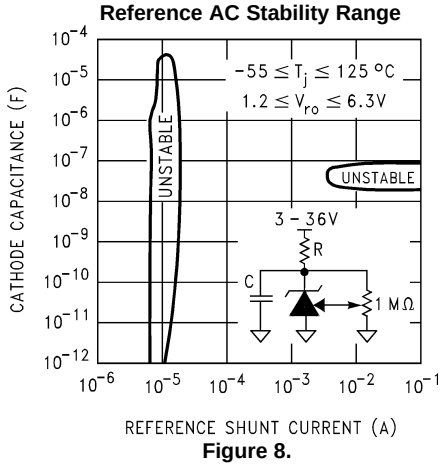


Figure 8.

FEEDBACK Current vs. FEEDBACK-to-Anode Voltage

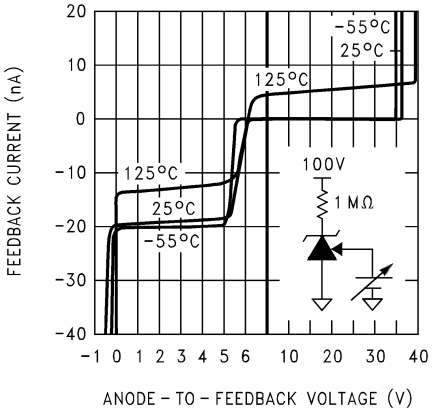


Figure 9.

FEEDBACK Current vs. FEEDBACK-to-Anode Voltage

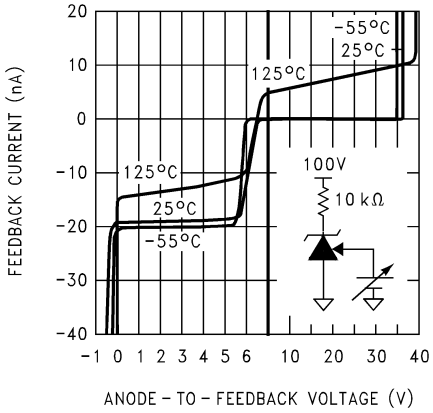


Figure 10.

Reference Noise Voltage vs. Frequency

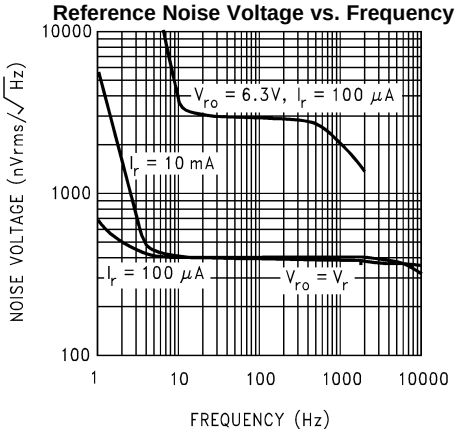


Figure 11.

Reference Small-Signal Resistance vs. Frequency

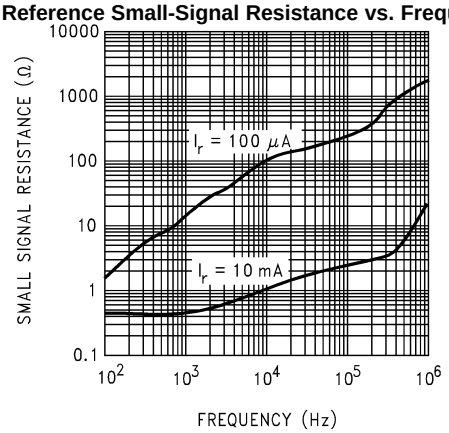


Figure 12.

Typical Performance Characteristics (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Power-Up Time

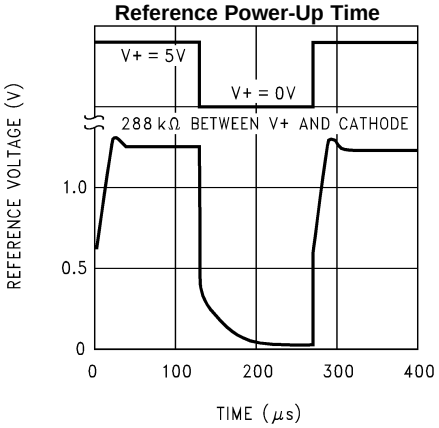


Figure 13.

Reference Voltage with FEEDBACK Voltage Step

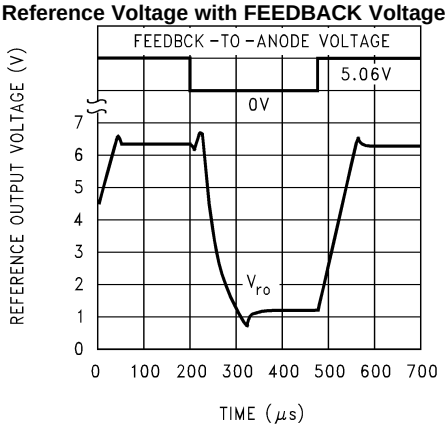


Figure 14.

Reference Voltage with 100~12 µA Current Step

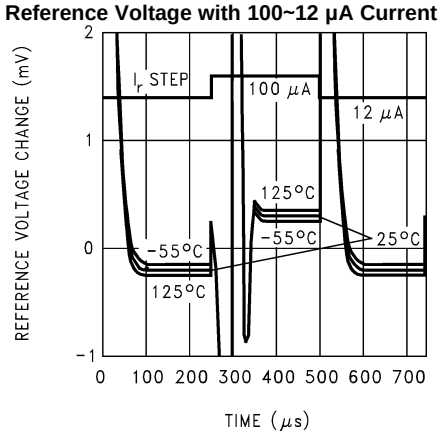


Figure 15.

Reference Step Response for 100 µA ~ 10 mA Current Step

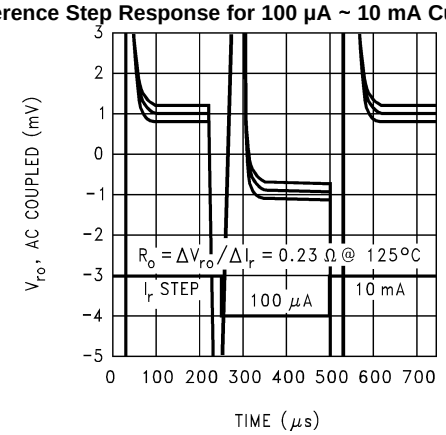


Figure 16.

Reference Voltage Change with Supply Voltage Step

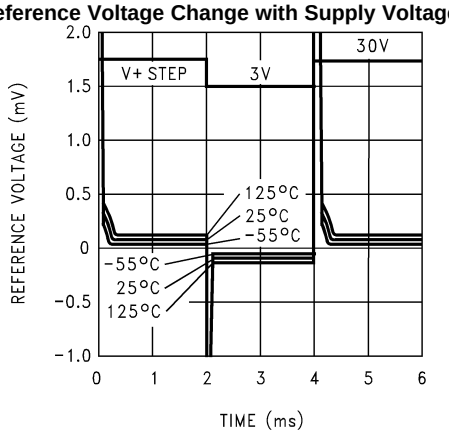


Figure 17.

Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C, unless otherwise noted

Input Common-Mode Voltage Range vs. Temperature

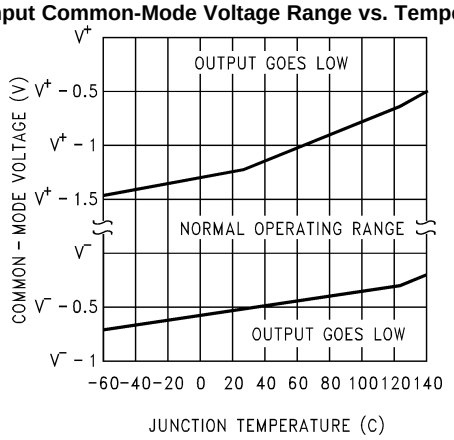


Figure 18.

V_{OS} vs. Junction Temperature on 9 Representative Units

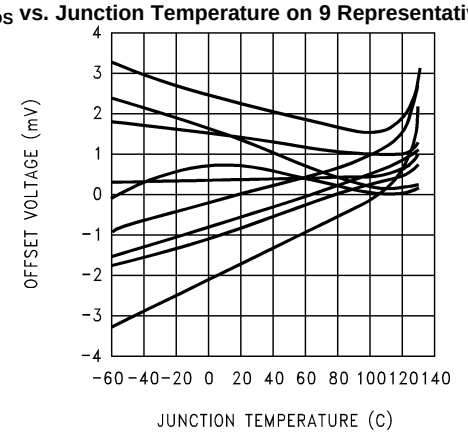


Figure 19.

Input Bias Current vs. Common-Mode Voltage

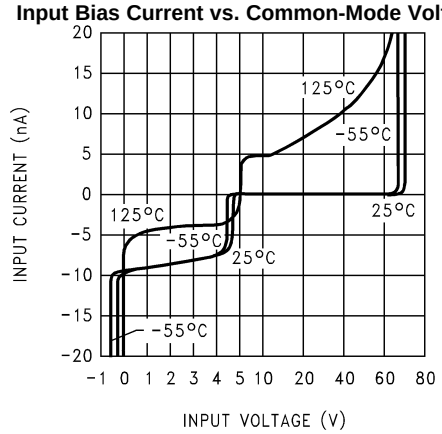


Figure 20.

Slew Rate vs. Temperature and Output Sink Current

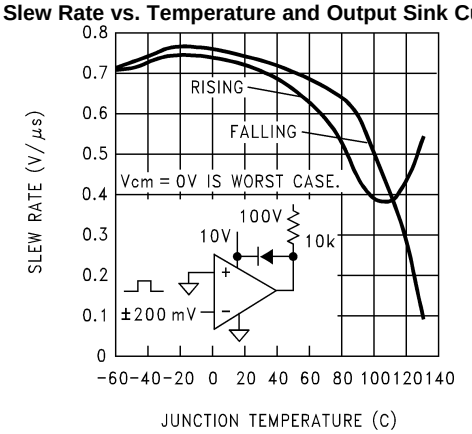


Figure 21.

Large-Signal Step Response

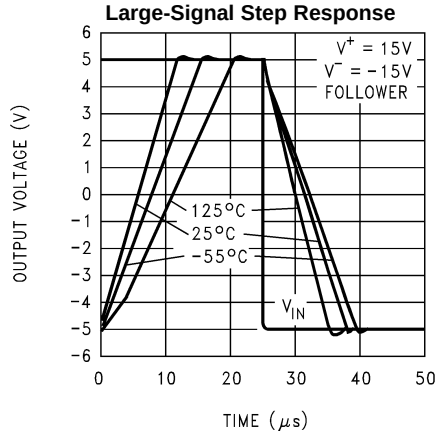


Figure 22.

Output Voltage Swing vs. Temp. and Current

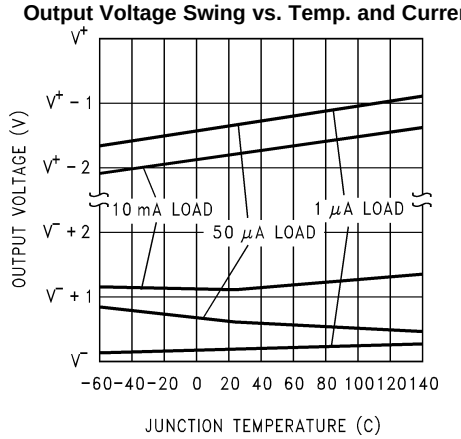


Figure 23.

Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Output Source Current vs. Output Voltage and Temp.

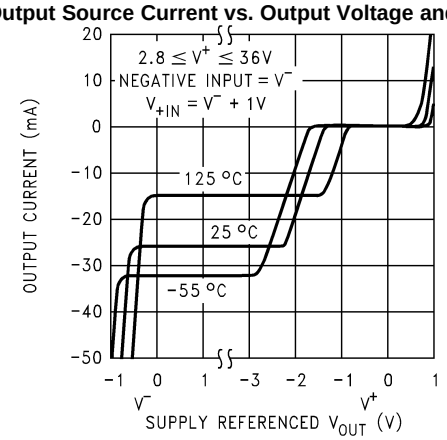


Figure 24.

Output Sink Current vs. Output Voltage and Temp.

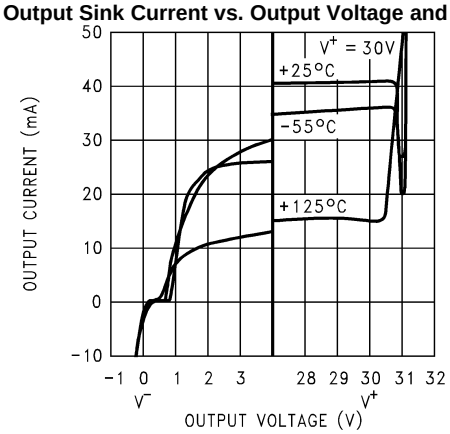


Figure 25.

Output Swing, Large Signal

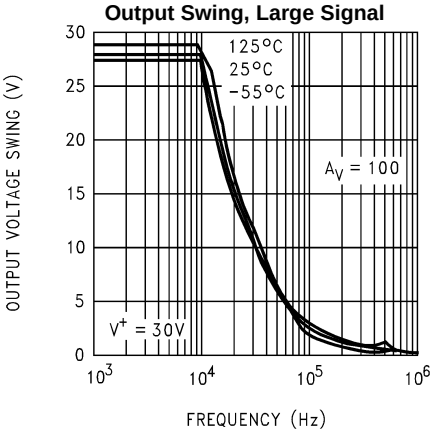


Figure 26.

Output Impedance vs. Frequency and Gain

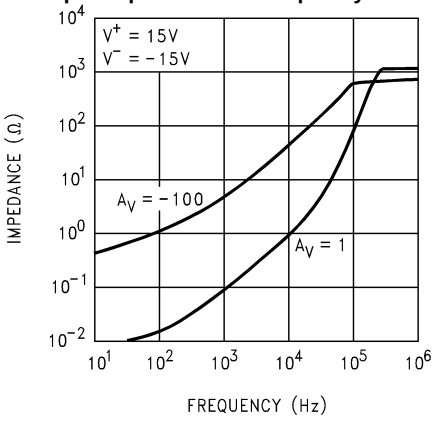


Figure 27.

Small-Signal Pulse Response vs. Temp.

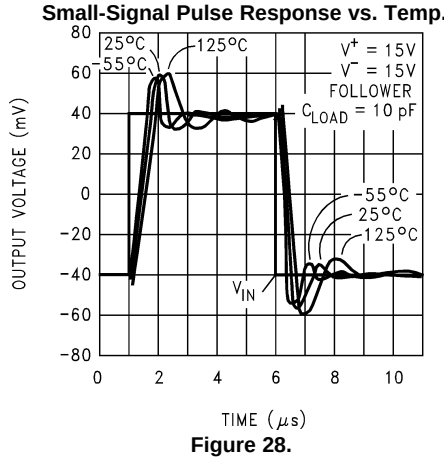


Figure 28.

Small-Signal Pulse Response vs. Load

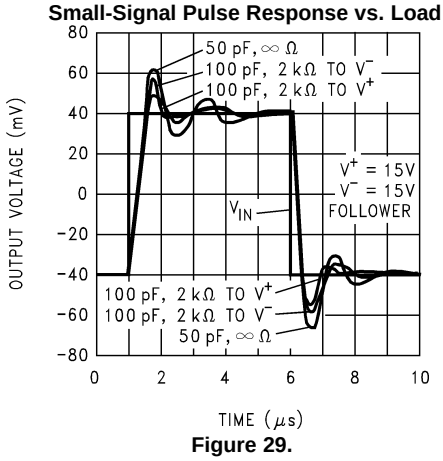


Figure 29.

Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C, unless otherwise noted

Op Amp Voltage Noise vs. Frequency

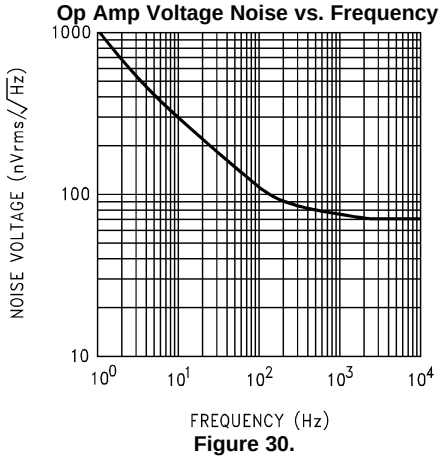


Figure 30.

Op Amp Current Noise vs. Frequency

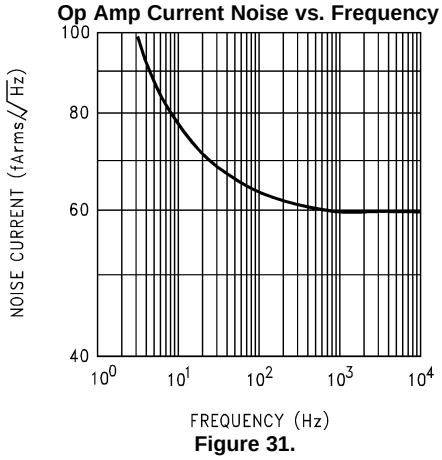


Figure 31.

Small-Signal Voltage Gain vs. Frequency and Temperature

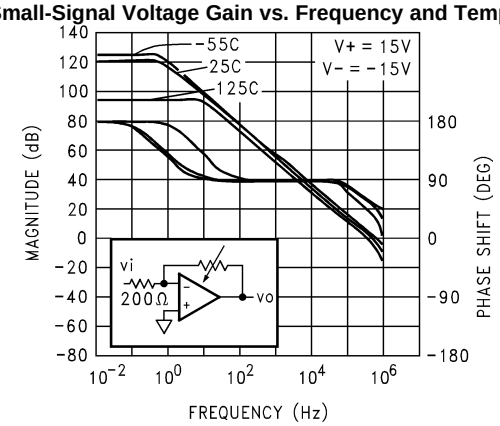


Figure 32.

Small-Signal Voltage Gain vs. Frequency and Load

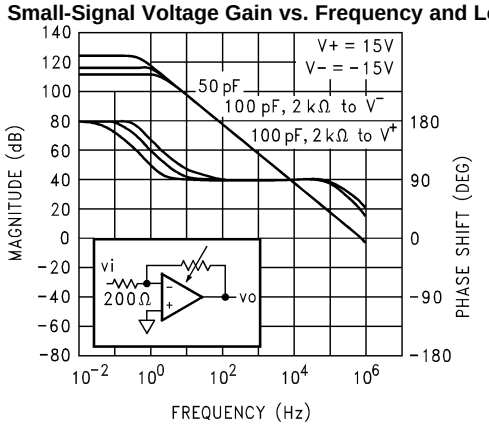


Figure 33.

Follower Small-Signal Frequency Response

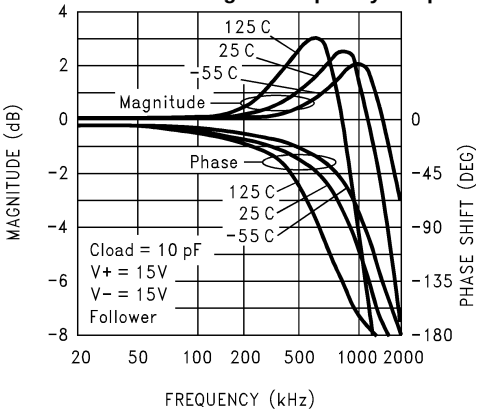


Figure 34.

Common-Mode Input Voltage Rejection Ratio

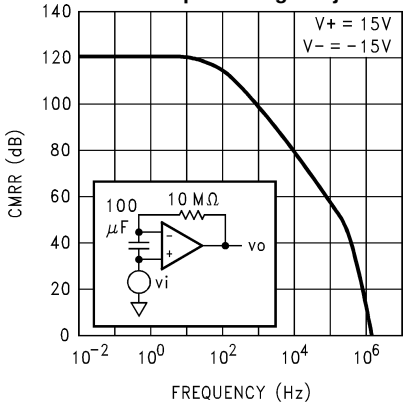


Figure 35.

Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

Power Supply Current vs. Power Supply Voltage

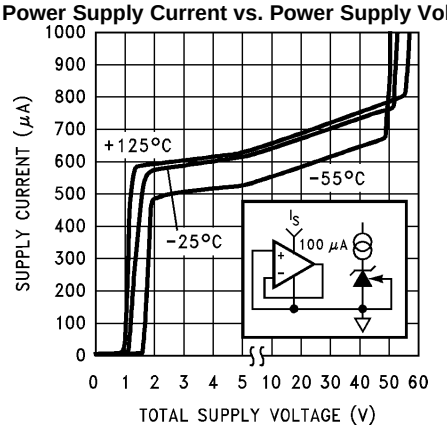


Figure 36.

Positive Power Supply Voltage Rejection Ratio

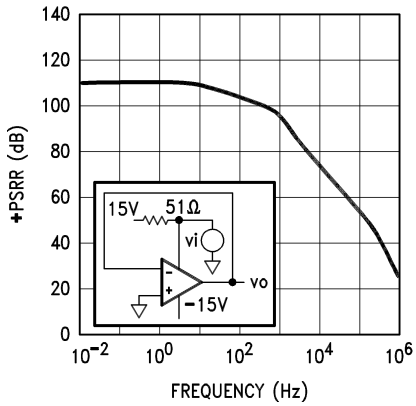


Figure 37.

Negative Power Supply Voltage Rejection Ratio

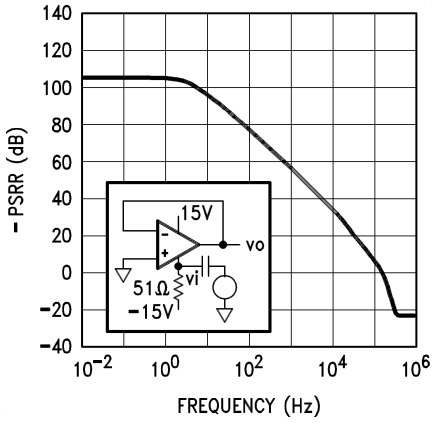


Figure 38.

Input Offset Current vs. Junction Temperature

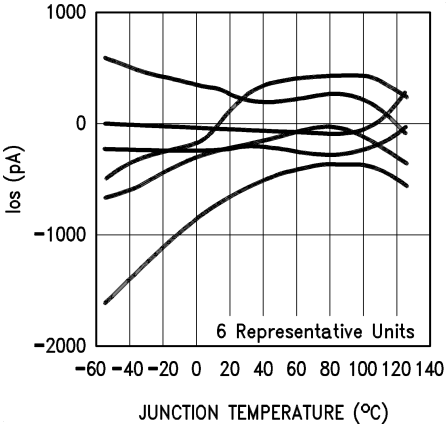


Figure 39.

Input Bias Current vs. Junction Temperature

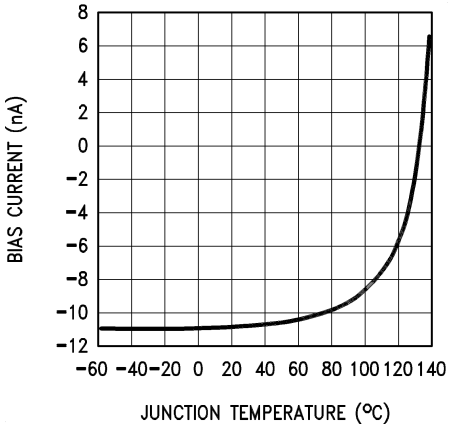


Figure 40.

Typical Performance Distributions

Average V_{OS} Drift Industrial Temperature Range

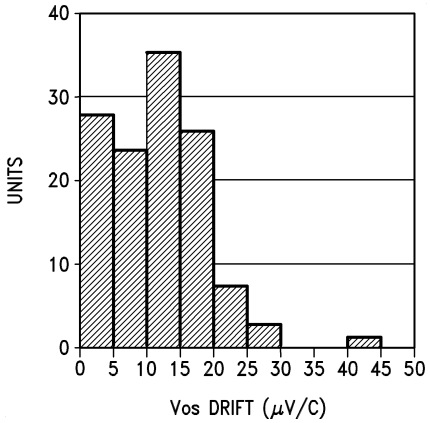


Figure 41.

Average V_{OS} Drift Commercial Temperature Range

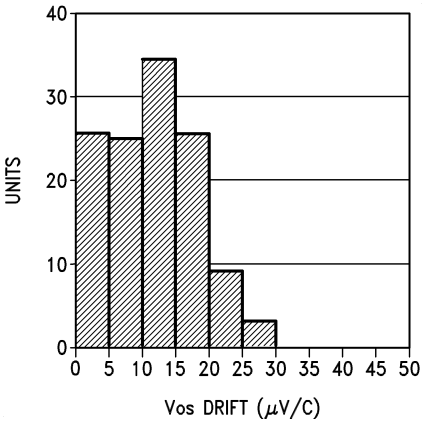


Figure 42.

Average I_{OS} Drift Industrial Temperature Range

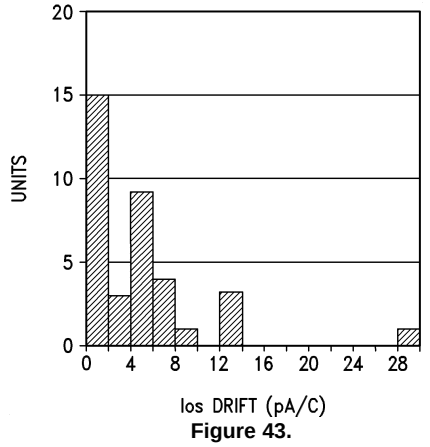


Figure 43.

Average I_{OS} Drift Commercial Temperature Range

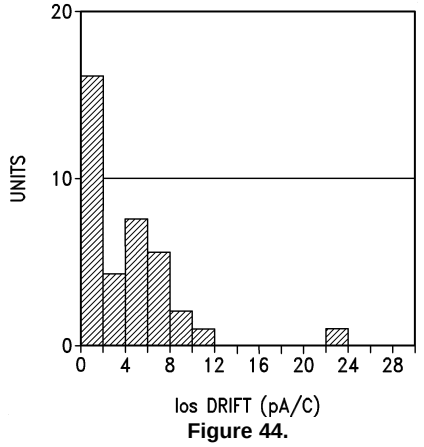


Figure 44.

Voltage Reference Broad-BandNoise Distribution

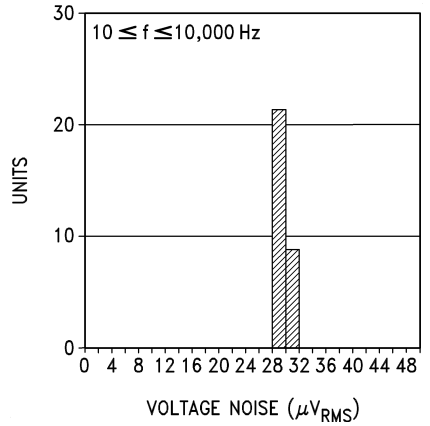


Figure 45.

Op Amp Voltage Noise Distribution

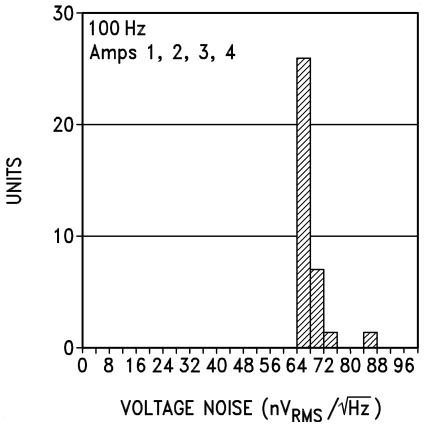


Figure 46.

Typical Performance Distributions (continued)

Op Amp Current Noise Distribution

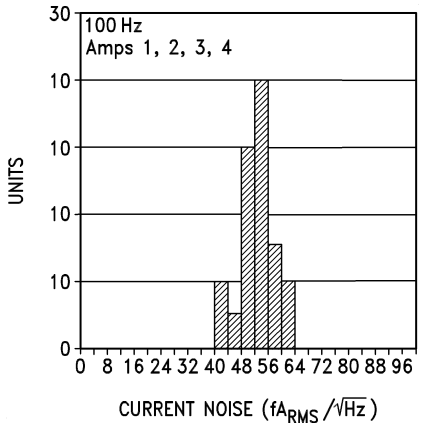


Figure 47.

APPLICATION INFORMATION

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 5.0V reference with V^+ = 3V is allowed.

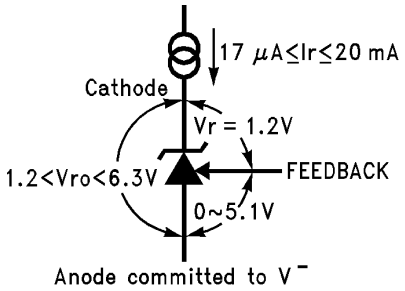


Figure 48. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how $V_r$is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

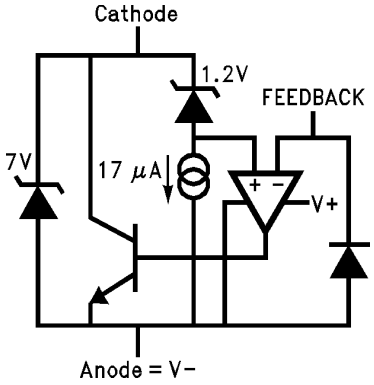


Figure 49. Reference Equivalent Circuit

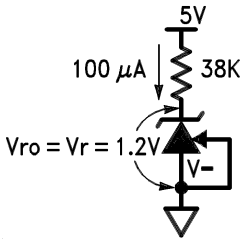


Figure 50. 1.2V Reference

Capacitors in parallel with the reference are allowed. See Reference AC Stability Range typical curve for capacitance values—from 20 µA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 5.0V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I=V_r/R1$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2=3.76/I. For a 1% error, use R1 such that I is greater than one hundred times the FEEDBACK bias current. For example, keep I ≥ 5.5µA.

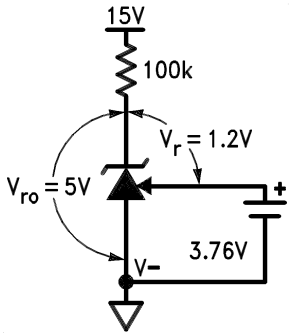
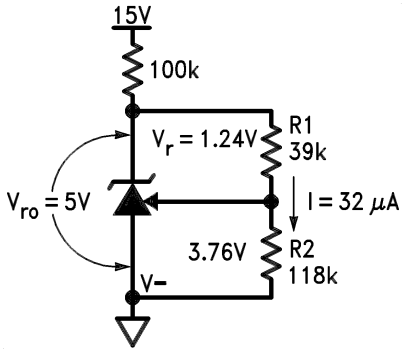


Figure 51. Thevenin Equivalent of Reference with 5V Output



R1 = Vr/I = 1.24/32µ = 39k
R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

Figure 52. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

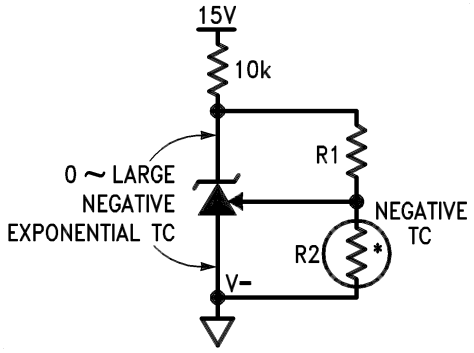


Figure 53. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

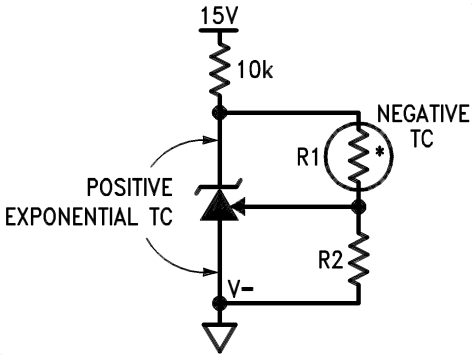


Figure 54. Output Voltage has Positive TC if R1 has Negative TC

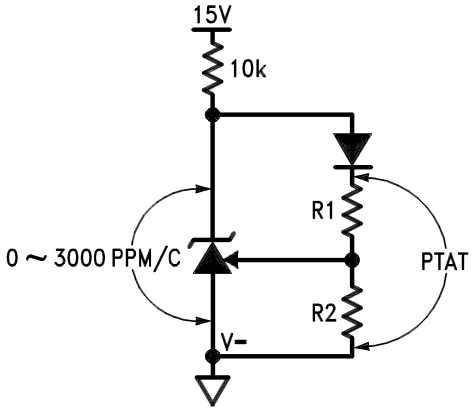
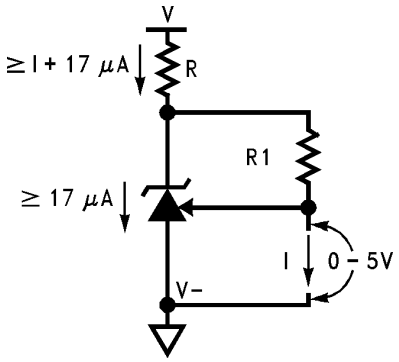


Figure 55. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



I = Vr/R1 = 1.24/R1

Figure 56. Current Source is Programmed by R1

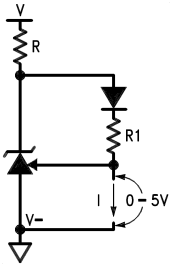


Figure 57. Proportional-to-Absolute-Temperature Current Source

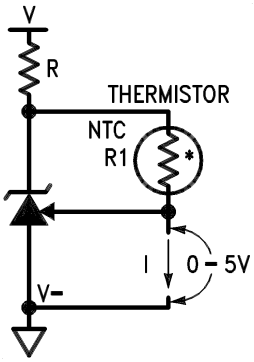


Figure 58. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Electrical Characteristics). One amp input may be outside the common-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. Output Swing: Unloaded, the 42µA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42µA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain
2. Cross-over Distortion: The LM614 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion
3. Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

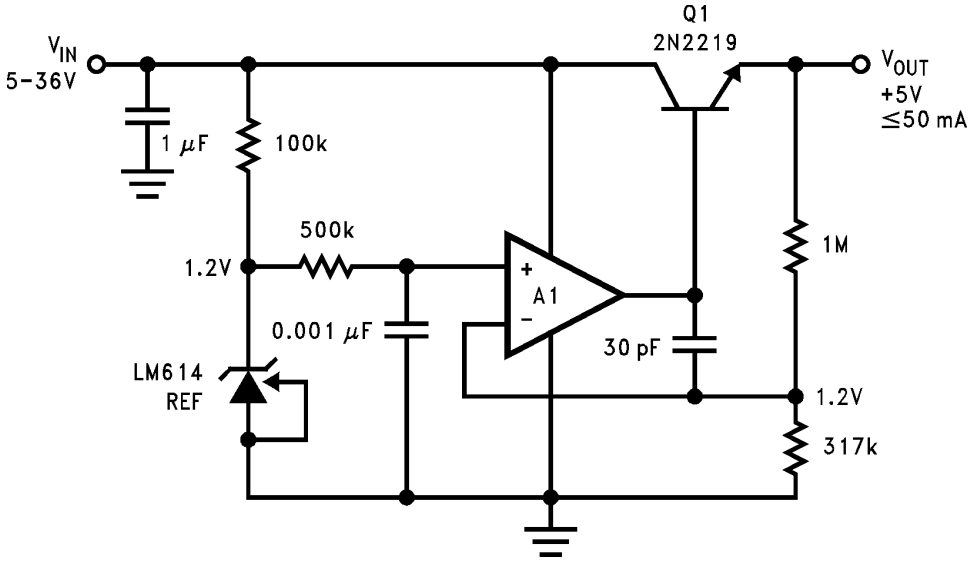
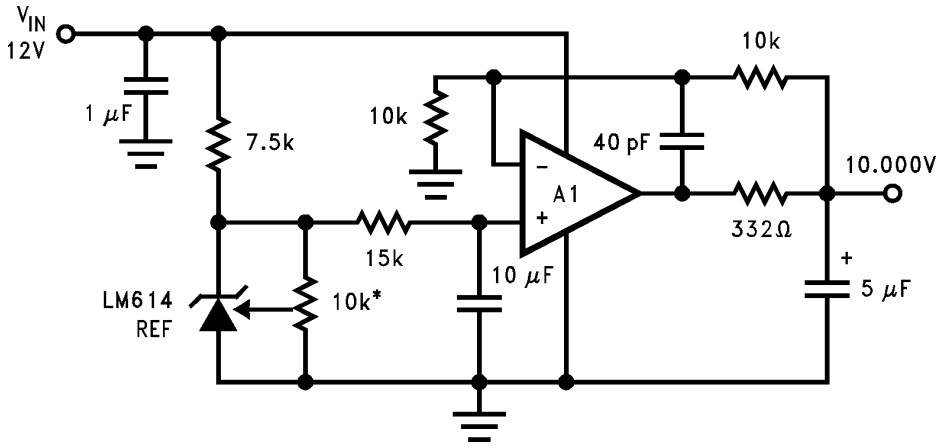
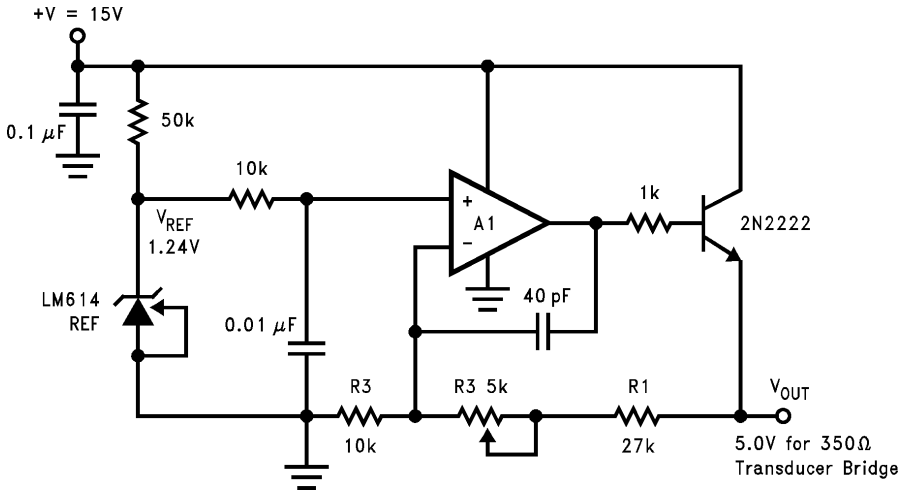


Figure 59. Simple Low Quiescent Drain Voltage Regulator. Total supply current approximately 320µA, when V_{IN} = +5V.



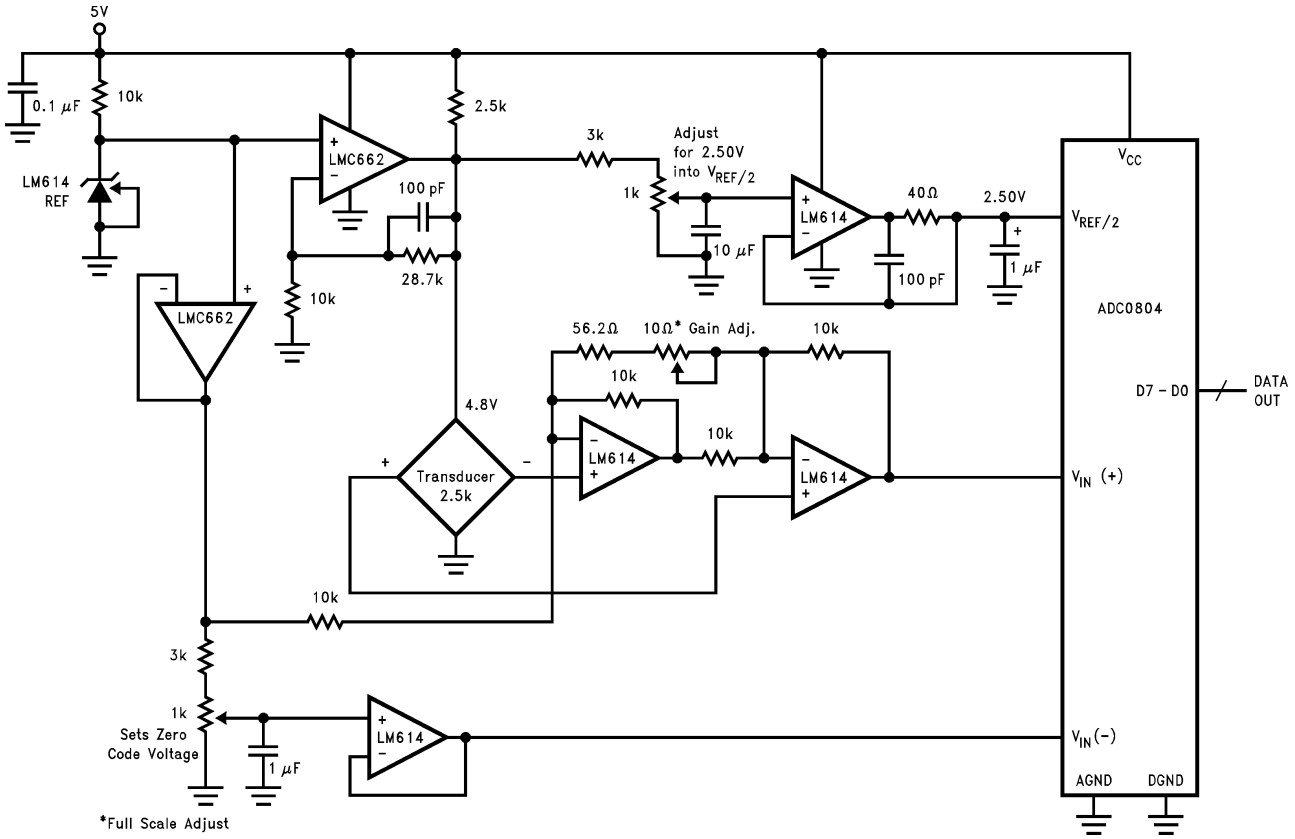
*10k must be low
t.c. trimpot.

Figure 60. Ultra Low Noise 10.00V Reference.
Total output noise is typically 14μV_{RMS}.



$V_{OUT} = (R_1 / Pe + 1)\ V_{REF}$
R_1, R_2 should be 1% metal film
P_β should be low T.C. trim pot

Figure 61. Slow Rise Time Upon Power-Up, Adjustable Transducer Bridge Driver.
Rise time is approximately 1ms.



(1) Set zero code voltage, then adjust 10Ω gain adjust pot for full scale.

Figure 62. Transducer Data Acquisition System.

Simplified Schematic Diagrams

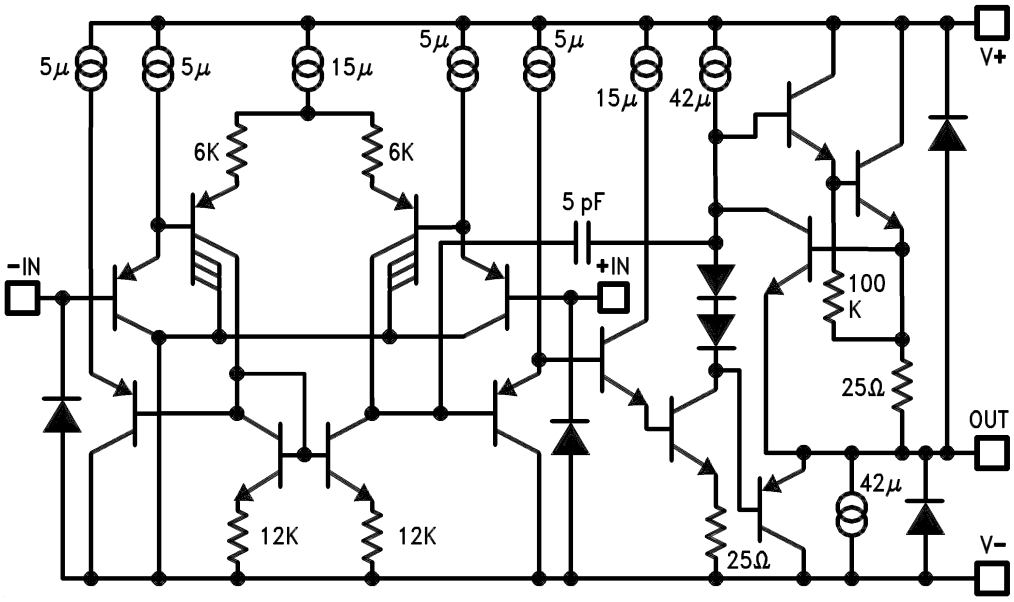


Figure 63. Op Amp

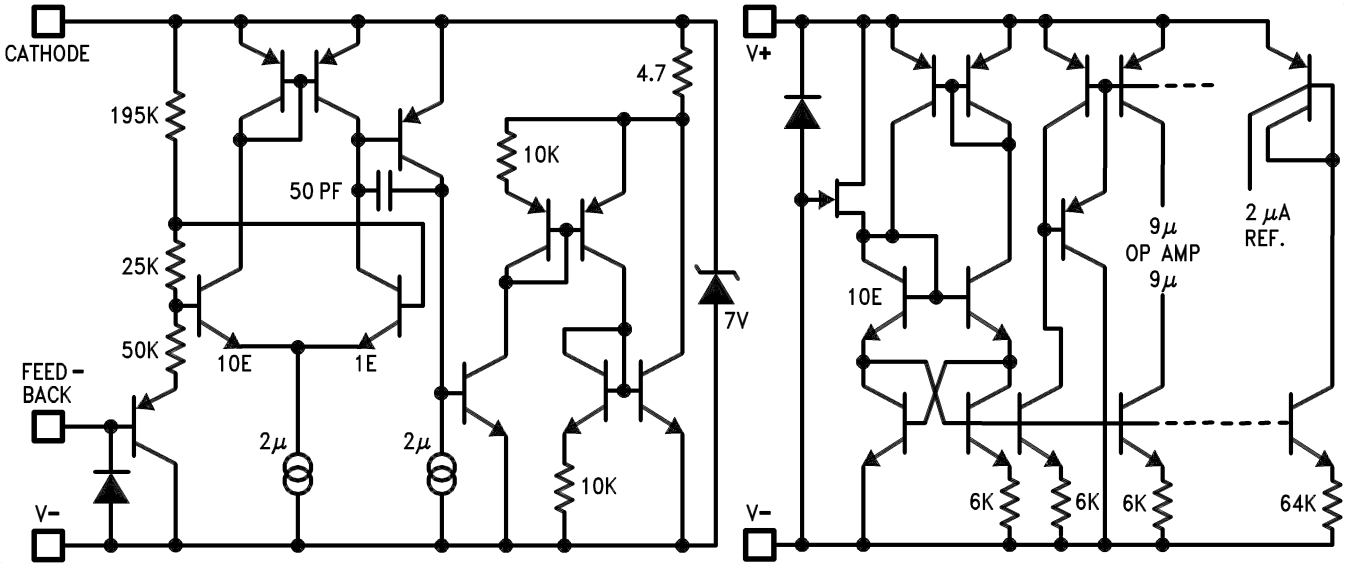


Figure 64. Reference / Bias

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM614 MDC	ACTIVE	DIESALE	Y	0	100	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM614CWM/NOPB	LIFEBUY	SOIC	DW	16	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM614CWM	
LM614IWM/NOPB	LIFEBUY	SOIC	DW	16	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM614IWM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

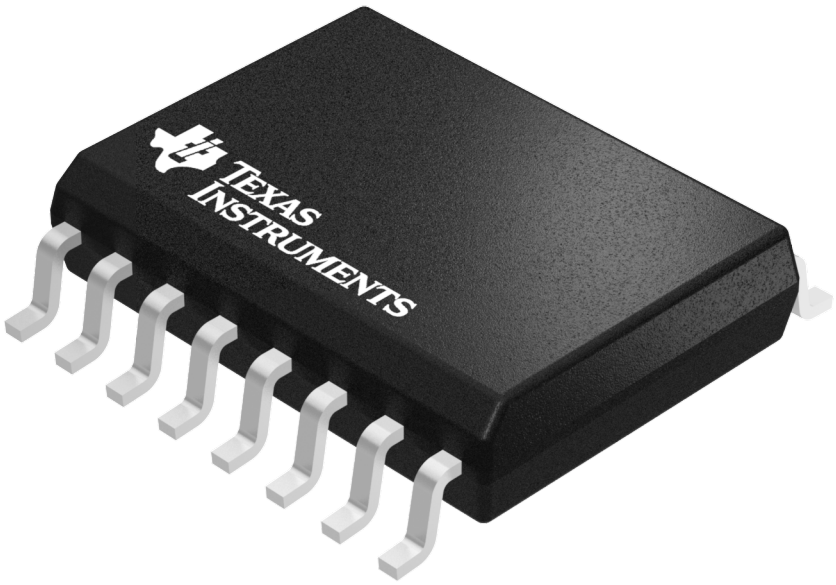
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

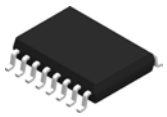
GENERIC PACKAGE VIEW

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

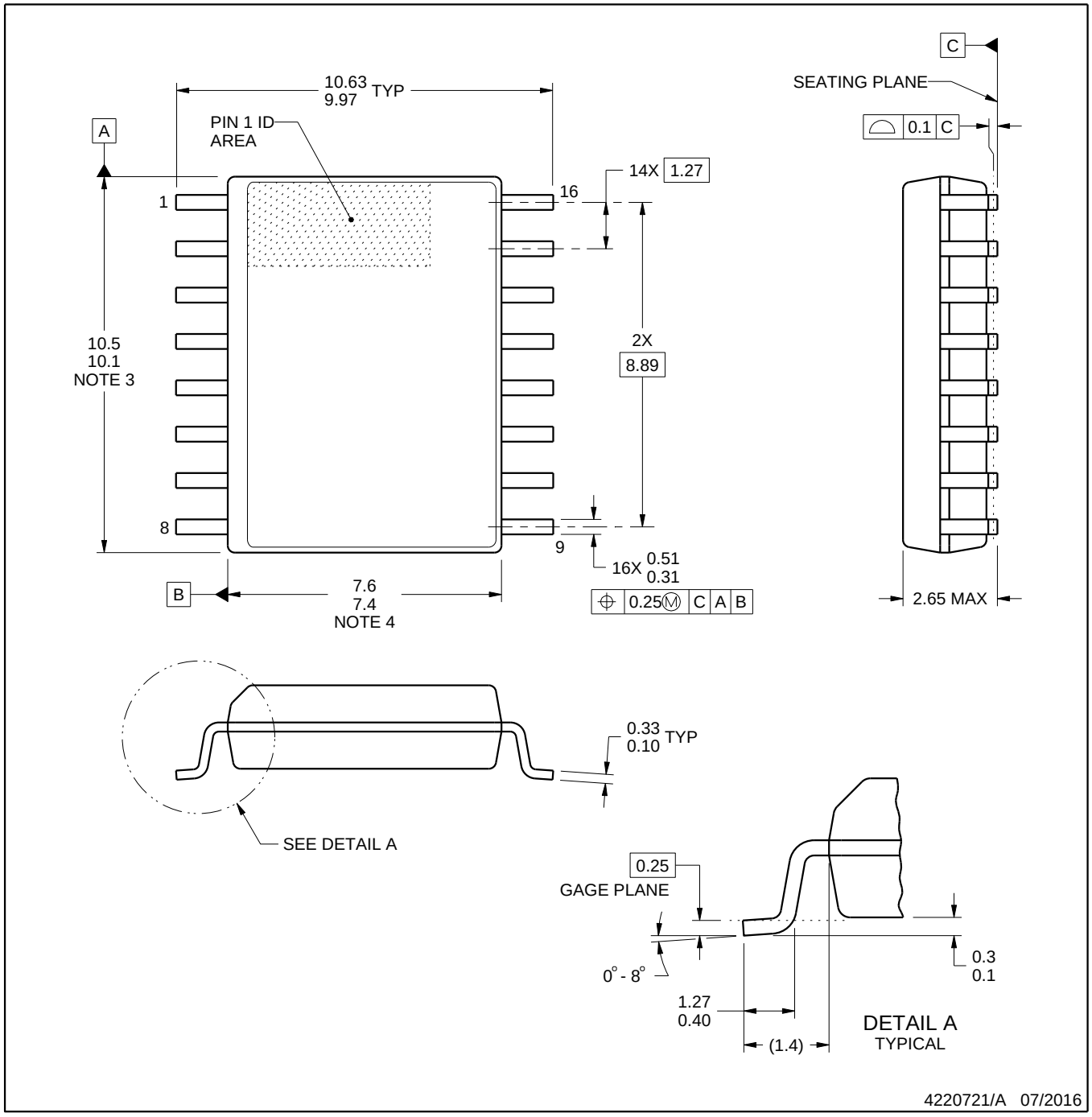


PACKAGE OUTLINE

DW0016A

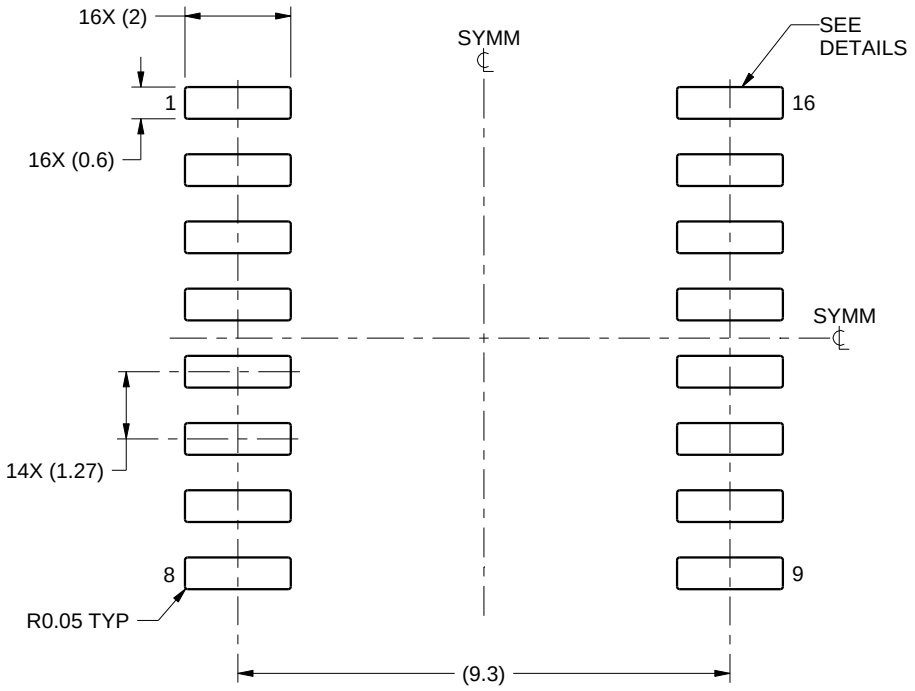
SOIC - 2.65 mm max height

SOIC

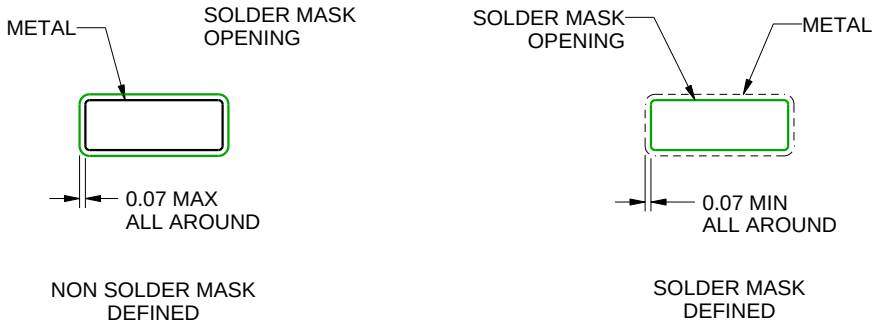


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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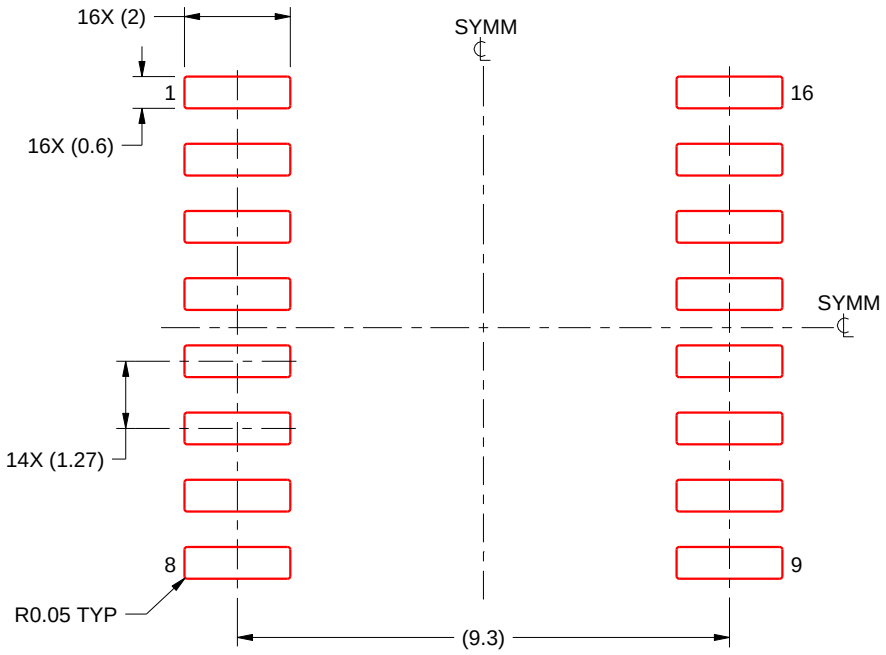
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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