

LMH664x Low Power, 130 MHz, 75 mA Rail-to-Rail Output Amplifiers

1 Features

($V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$, $A_V = +1$. Typical Values Unless Specified).

- -3 dB BW ($A_V = +1$) 130 MHz
- Supply Voltage Range 2.7 V to 12.8 V
- Slew Rate, ($A_V = -1$) $130\text{V}/\mu\text{s}$ ⁽¹⁾
- Supply Current (no load) 2.7 mA/amp
- Output Short Circuit Current +115 mA to 145 mA
- Linear Output Current $\pm 75\text{ mA}$
- Input Common Mode Volt. 0.5 V Beyond V^- , 1 V from V^+
- Output Voltage Swing 40 mV from Rails
- Input Voltage Noise (100 kHz) $17\text{nV}/\sqrt{\text{Hz}}$
- Input Current Noise (100 kHz) $0.9\text{pA}/\sqrt{\text{Hz}}$
- THD (5MHz, $R_L = 2\text{k}\Omega$, $V_O = 2V_{PP}$, $A_V = +2$) -62 dBc
- Settling Time 68 ns
- Fully Characterized for 3 V, 5 V, and $\pm 5\text{ V}$
- Overdrive Recovery 100 ns
- Output Short Circuit Protected⁽²⁾
- No Output Phase Reversal with CMVR Exceeded

⁽¹⁾ Slew rate is the average of the rising and falling slew rates

⁽²⁾ Output short circuit duration is infinite for $V_S < 6\text{ V}$ at room temperature and below. For $V_S > 6\text{ V}$, allowable short circuit duration is 1.5 ms.

2 Applications

- Active Filters
- CD/DVD ROM
- ADC Buffer Amp
- Portable Video
- Current Sense Buffer

3 Description

The LMH664X family true single supply voltage feedback amplifiers offer high speed (130 MHz), low distortion (-62 dBc), and exceptionally high output current (approximately 75 mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5 V below V^- and 1 V from V^+ . Output voltage range extends to within 40 mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75 mA in order to drive heavy loads. Fast output Slew Rate ($130\text{ V}/\mu\text{s}$) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40 MHz with a 3 V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6642	SOT-23 (5)	2.90 mm x 1.60 mm
	SOIC (8)	4.90 mm x 3.91 mm
LMH6643	SOIC (8)	3.00 mm x 3.00 mm
	VSSOP (8)	
LMH6644	SOIC (14)	8.64 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm

⁽¹⁾ For all available packages, see the orderable addendum at the end of the datasheet.

Closed Loop Gain vs. Frequency for Various Supplies

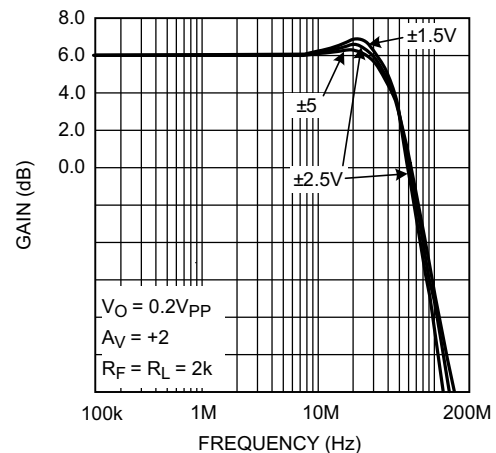


Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Description (continued) 3 6 Pin Configuration and Functions 4 7 Specifications 5 7.1 Absolute Maximum Ratings 5 7.2 Handling Ratings..... 5 7.3 Recommended Operating Conditions..... 5 7.4 Thermal Information 5 7.5 3V Electrical Characteristics 6 7.6 5V Electrical Characteristics 8 7.7 \pm 5V Electrical Characteristics 10 7.8 Typical Performance Characteristics 12 8 Detailed Description 21 8.1 Overview 21	8.2 Functional Block Diagram 21 8.3 Feature Description..... 21 8.4 Device Functional Modes..... 21 9 Application and Implementation 22 9.1 Application Information..... 22 9.2 Typical Application 22 10 Power Supply Recommendations 24 11 Layout 25 11.1 Layout Guidelines 25 11.2 Layout Example 25 12 Device and Documentation Support 26 12.1 Related Links 26 12.2 Trademarks 26 12.3 Electrostatic Discharge Caution..... 26 12.4 Glossary 26 13 Mechanical, Packaging, and Orderable Information 26
--	--

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (March 2013) to Revision Q	Page
• Added, revised, or updated the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Device and Documentation Support; Mechanical, Packaging, and Ordering Information	1
• Changed "Junction Temperature Range" to "Operating Temperature Range"	5
• Deleted $T_J = 25^\circ\text{C}$ for Electrical Characteristics tables.	6
• Changed from " R_L " to " R_f "	6
• Deleted $T_J = 25^\circ\text{C}$ for Typical Performance Characteristics	12

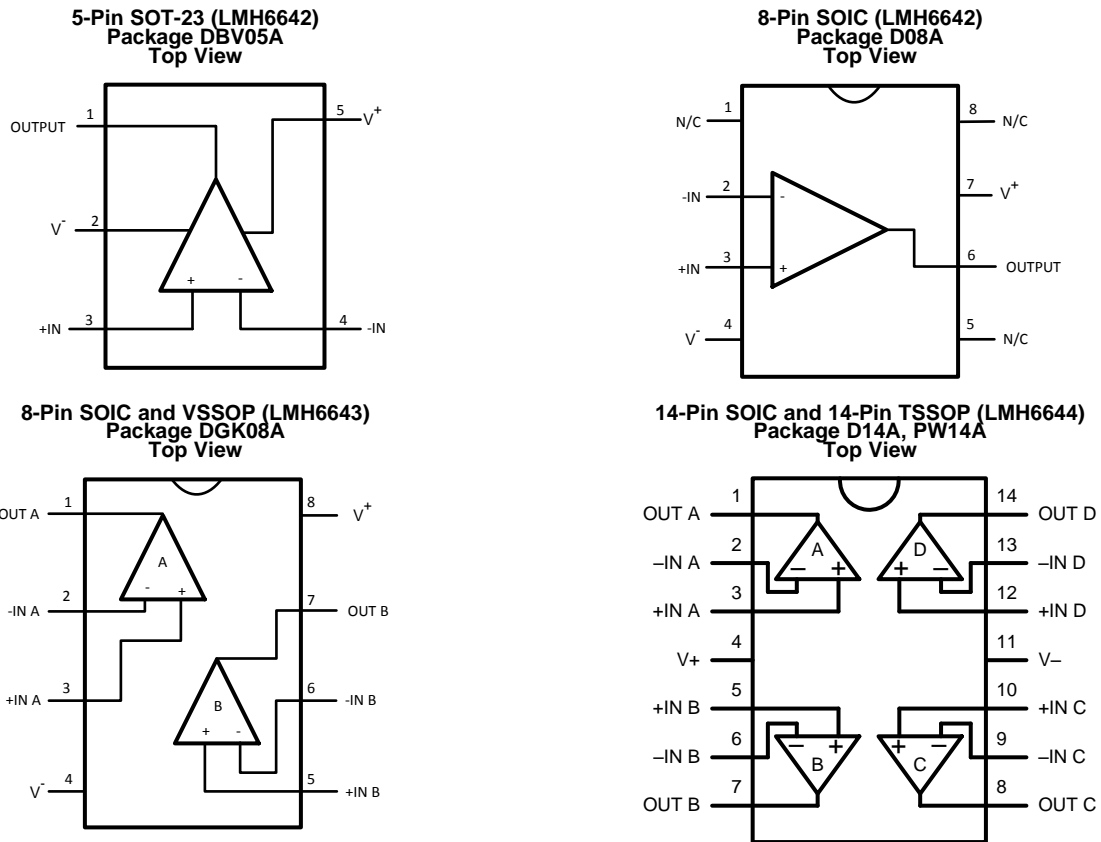
Changes from Revision O (March 2013) to Revision P	Page
• Changed layout of National Data Sheet to TI format	1

5 Description (continued)

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12 MHz under 150 Ω load and $A_V = +2$) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in an ADC buffer as well as high frequency filter applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150 Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642), dual (LMH6643), and quad (LMH6644) options.

6 Pin Configuration and Functions



Pin Functions

NAME	PIN				I/O	DESCRIPTION
	LMH6642		LMH6643	LMH6644		
	DBV05A	D08A	DGK08A	D14A and PW14A		
-IN	4	2			I	Inverting Input
+IN	3	3			I	Non-inverting Input
-IN A			2	2	I	ChA Inverting Input
+IN A			3	3	I	ChA Non-inverting Input
-IN B			6	6	I	ChB Inverting Input
+IN B			5	5	I	ChB Non-inverting Input
-IN C				9	I	ChC Inverting Input
+IN C				10	I	ChC Non-inverting Input
-IN D				13	I	ChD Inverting Input
+IN D				12	I	ChD Non-inverting Input
N/C		1,5,8			—	No connection
OUT A			1	1	O	ChA Output
OUT B			7	7	O	ChB Output
OUT C				8	O	ChC Output
OUT D				14	O	ChD Output
OUTPUT	1	6			O	Output
V ⁻	2	4	4	11	I	Negative Supply
V ⁺	5	7	8	4	I	Positive Supply

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN} Differential			±2.5	V
Output Short Circuit Duration		See ⁽³⁾ and ⁽⁴⁾		
Supply Voltage (V ⁺ - V ⁻)			13.5	V
Voltage at Input/Output pins			V ⁺ +0.8 V ⁻ -0.8	V
Input Current			±10	mA
Junction Temperature ⁽⁵⁾			+150	°C
Soldering Information	Infrared or Convection Reflow (20 sec)		235	°C
	Wave Soldering Lead Temp.(10 sec)		260	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
- (5) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	+150	°C
V _(ESD)	Electrostatic discharge ⁽¹⁾	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾	2000	V
		Machine model (MM) ⁽³⁾	200	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽⁴⁾	1000	

- (1) Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 0 Ω in series with 200 pF.
- (2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.
- (4) JEDEC document JEP157 states that 1000-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage (V ⁺ - V ⁻)		2.7	12.8	V
Operating Temperature Range ⁽²⁾		-40	+85	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMH6642		LMH6643	LMH6644		UNIT
		DBV05A	D08A	DGK08A	D14A	PW14A	
		5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient Thermal Resistance ⁽²⁾	265	190	235	145	155	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.5 3V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} $R_L = 2k\Omega$ to $V^+/2$			UNIT
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	
BW	-3dB BW	$A_V = +1$, $V_{OUT} = 200mV_{PP}$			80	115		MHz
		$A_V = +2$, -1 , $V_{OUT} = 200mV_{PP}$				46		
$BW_{0.1dB}$	0.1dB Gain Flatness	$A_V = +2$, $R_L = 150\Omega$ to $V^+/2$, $R_f = 402\Omega$, $V_{OUT} = 200mV_{PP}$				19		MHz
PBW	Full Power Bandwidth	$A_V = +1$, $-1dB$, $V_{OUT} = 1V_{PP}$				40		MHz
e_n	Input-Referred Voltage Noise	$f = 100kHz$				17		nV/\sqrt{Hz}
		$f = 1kHz$				48		
i_n	Input-Referred Current Noise	$f = 100kHz$				0.90		pA/\sqrt{Hz}
		$f = 1kHz$				3.3		
THD	Total Harmonic Distortion	$f = 5MHz$, $V_O = 2V_{PP}$, $A_V = -1$, $R_L = 100\Omega$ to $V^+/2$				-48		dBc
DG	Differential Gain	$V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.17%		
		$R_L = 1k\Omega$ to $V^+/2$				0.03%		
DP	Differential Phase	$V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.05		deg
		$R_L = 1k\Omega$ to $V^+/2$				0.03		
CT Rej.	Cross-Talk Rejection	$f = 5MHz$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$				47		dB
T_S	Settling Time	$V_O = 2V_{PP}$, $\pm 0.1\%$, 8pF Load, $V_S = 5V$				68		ns
SR	Slew Rate ⁽³⁾	$A_V = -1$, $V_I = 2V_{PP}$			90	120		$V/\mu s$
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644				± 7	± 1 ± 5	mV
		For LMH6643				± 7	± 1 ± 3.4	
TC V_{OS}	Input Offset Average Drift	See ⁽⁴⁾				± 5		$\mu V/^\circ C$
I_B	Input Bias Current	See ⁽⁵⁾			-3.25	-1.50	-2.60	μA
I_{OS}	Input Offset Current				1000	20	800	nA
R_{IN}	Common Mode Input Resistance					3		M Ω

- (1) All limits are ensured by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm.
- (3) Slew rate is the average of the rising and falling slew rates.
- (4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} $R_L = 2k\Omega$ to $V^+/2$			UNIT
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	
C_{IN}	Common Mode Input Capacitance					2		pF
CMVR	Input Common-Mode Voltage Range	CMRR \geq 50dB		-0.1	-0.5	-0.2		V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V			72	95		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.5V$ to $2.5V$ $R_L = 2k\Omega$ to $V^+/2$	75		80	96		dB
		$V_O = 0.5V$ to $2.5V$ $R_L = 150\Omega$ to $V^+/2$	70		74	82		
V_O	Output Swing High	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$			2.90	2.98		V
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$			2.80	2.93		
V_O	Output Swing Low	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$				25	75	mV
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$				75	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ $V_{ID} = 200mV$ ⁽⁶⁾	35		50	95		mA
		Sinking to $V^+/2$ $V_{ID} = -200mV$ ⁽⁶⁾	40		55	110		
I_{OUT}	Output Current	$V_{OUT} = 0.5V$ from either supply				± 65		mA
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 3.0V$ to $3.5V$, $V_{CM} = 1.5V$			75	85		dB
I_S	Supply Current (per channel)	No Load		4.50		2.70	4.00	mA

(6) Short circuit test is a momentary test. See [Note 7](#) under 5 V Electrical Characteristics.

7.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 5V, V^- = 0V,$ $V_{CM} = V_O = V^+/2, V_{ID}$ $R_L = 2k\Omega$ to $V^+/2$			UNIT
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	
BW	–3dB BW	$A_V = +1, V_{OUT} = 200mV_{PP}$			90	120		MHz
		$A_V = +2, -1, V_{OUT} = 200mV_{PP}$				46		
$BW_{0.1dB}$	0.1dB Gain Flatness	$A_V = +2, R_L = 150\Omega$ to $V^+/2,$ $R_f = 402\Omega, V_{OUT} = 200mV_{PP}$				15		MHz
PBW	Full Power Bandwidth	$A_V = +1, -1dB, V_{OUT} = 2V_{PP}$				22		MHz
e_n	Input-Referred Voltage Noise	$f = 100kHz$				17		nV/ \sqrt{Hz}
		$f = 1kHz$				48		
i_n	Input-Referred Current Noise	$f = 100kHz$				0.90		pA/ \sqrt{Hz}
		$f = 1kHz$				3.3		
THD	Total Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = +2$				–60		dBc
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.16%		
		$R_L = 1k\Omega$ to $V^+/2$				0.05%		
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.05		deg
		$R_L = 1k\Omega$ to $V^+/2$				0.01		
CT Rej.	Cross-Talk Rejection	$f = 5MHz, \text{Receiver:}$ $R_f = R_g = 510\Omega, A_V = +2$				47		dB
T_S	Settling Time	$V_O = 2V_{PP}, \pm 0.1\%, 8pF$ Load				68		ns
SR	Slew Rate ⁽³⁾	$A_V = -1, V_I = 2V_{PP}$			95	125		V/ μs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644		± 7		± 1	± 5	mV
		For LMH6643		± 7		± 1	± 3.4	
TC V_{OS}	Input Offset Average Drift	See ⁽⁴⁾				± 5		$\mu V/^\circ C$
I_B	Input Bias Current	See ⁽⁵⁾		–3.25		–1.70	–2.60	μA
I_{OS}	Input Offset Current			1000		20	800	nA
R_{IN}	Common Mode Input Resistance					3		M Ω
C_{IN}	Common Mode Input Capacitance					2		pF
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50dB$		–0.1		–0.5	–0.2	V
				3.6		3.8	4.0	
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V				72	95	dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.5V$ to $4.50V$ $R_L = 2k\Omega$ to $V^+/2$		82		86	98	dB
		$V_O = 0.5V$ to $4.25V$ $R_L = 150\Omega$ to $V^+/2$		72		76	82	

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} $R_L = 2k\Omega$ to $V^+/2$			UNIT	
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾		
V_O	Output Swing High	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$				4.90	4.98	V	
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$				4.65	4.90		
	Output Swing Low	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$					25	100	mV
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$					100	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ $V_{ID} = 200mV$ ⁽⁶⁾⁽⁷⁾	40			55	115	mA	
		Sinking to $V^+/2$ $V_{ID} = -200mV$ ⁽⁶⁾⁽⁷⁾	55			70	140		
I_{OUT}	Output Current	$V_O = 0.5V$ from either supply				± 70		mA	
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 4.0V$ to $6V$				79	90	dB	
I_S	Supply Current (per channel)	No Load			5.00		2.70	4.25	mA

(6) Short circuit test is a momentary test. See [Note 7](#).

(7) Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

7.7 ±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to ground.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID}			UNIT
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	
BW	-3dB BW	$A_V = +1$, $V_{OUT} = 200mV_{PP}$			95	130		MHz
		$A_V = +2$, -1 , $V_{OUT} = 200mV_{PP}$				46		
$BW_{0.1dB}$	0.1dB Gain Flatness	$A_V = +2$, $R_L = 150\Omega$ to $V^+/2$, $R_f = 806\Omega$, $V_{OUT} = 200mV_{PP}$				12		MHz
PBW	Full Power Bandwidth	$A_V = +1$, $-1dB$, $V_{OUT} = 2V_{PP}$				24		MHz
e_n	Input-Referred Voltage Noise	$f = 100kHz$				17		nV/\sqrt{Hz}
		$f = 1kHz$				48		
i_n	Input-Referred Current Noise	$f = 100kHz$				0.90		pA/\sqrt{Hz}
		$f = 1kHz$				3.3		
THD	Total Harmonic Distortion	$f = 5MHz$, $V_O = 2V_{PP}$, $A_V = +2$				-62		dBc
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.15%		
		$R_L = 1k\Omega$ to $V^+/2$				0.01%		
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$				0.04		deg
		$R_L = 1k\Omega$ to $V^+/2$				0.01		
CT Rej.	Cross-Talk Rejection	$f = 5MHz$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$				47		dB
T_S	Settling Time	$V_O = 2V_{PP}$, $\pm 0.1\%$, 8pF Load, $V_S = 5V$				68		ns
SR	Slew Rate ⁽³⁾	$A_V = -1$, $V_I = 2V_{PP}$			100	135		V/ μs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644			± 7	± 1	± 5	mV
		For LMH6643			± 7	± 1	± 3.4	
TC V_{OS}	Input Offset Average Drift	See ⁽⁴⁾				± 5		$\mu V/^\circ C$
I_B	Input Bias Current	See ⁽⁵⁾			-3.25	-1.60	-2.60	μA
I_{OS}	Input Offset Current				1000	20	800	nA
R_{IN}	Common Mode Input Resistance					3		M Ω
C_{IN}	Common Mode Input Capacitance					2		pF
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50dB$			-5.1	-5.5	-5.2	V
					3.6	3.8	4.0	
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from $-5V$ to $3.5V$			74	95		dB

- (1) All limits are ensured by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm.
- (3) Slew rate is the average of the rising and falling slew rates.
- (4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to ground.

PARAMETER	TEST CONDITIONS	AT TEMPERATURE EXTREMES			$V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID}			UNIT
		MIN	TYP	MAX	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	
A_{VOL}	Large Signal Voltage Gain	$V_O = -4.5V$ to $4.5V$, $R_L = 2k\Omega$	84			88	96	dB
		$V_O = -4.0V$ to $4.0V$, $R_L = 150\Omega$	74			78	82	
V_O	Output Swing High	$R_L = 2k\Omega$, $V_{ID} = 200mV$				4.90	4.96	V
		$R_L = 150\Omega$, $V_{ID} = 200mV$				4.65	4.80	
	Output Swing Low	$R_L = 2k\Omega$, $V_{ID} = -200mV$				-4.96	-4.90	V
		$R_L = 150\Omega$, $V_{ID} = -200mV$				-4.80	-4.65	
I_{SC}	Output Short Circuit Current	Sourcing to Ground $V_{ID} = 200mV$ ⁽⁶⁾⁽⁷⁾	35			60	115	mA
		Sinking to Ground $V_{ID} = -200mV$ ⁽⁶⁾⁽⁷⁾	65			85	145	
I_{OUT}	Output Current	$V_O = 0.5V$ from either supply				±75		mA
PSRR	Power Supply Rejection Ratio	$(V^+, V^-) = (4.5V, -4.5V)$ to $(5.5V, -5.5V)$				78	90	dB
I_S	Supply Current (per channel)	No Load			5.50	2.70	4.50	mA

(6) Short circuit test is a momentary test. See ⁽⁷⁾.

(7) Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

7.8 Typical Performance Characteristics

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

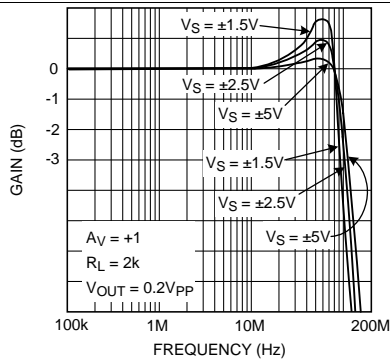


Figure 1. Closed Loop Frequency Response for Various Supplies

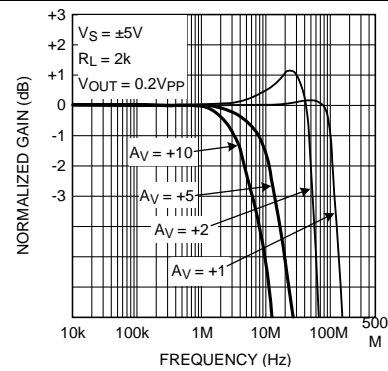


Figure 2. Closed Loop Gain vs. Frequency for Various Gain

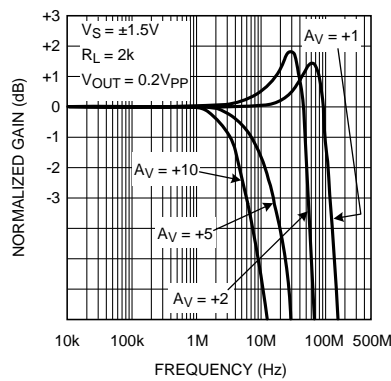


Figure 3. Closed Loop Gain vs. Frequency for Various Gain

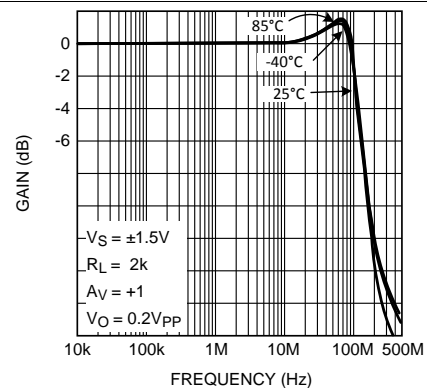


Figure 4. Closed Loop Frequency Response for Various Temperature

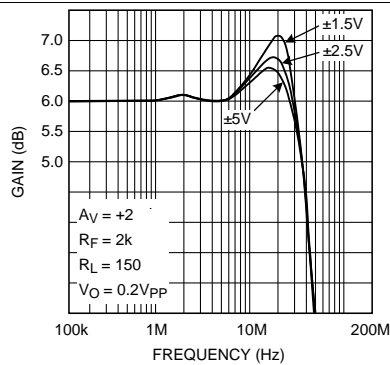


Figure 5. Closed Loop Gain vs. Frequency for Various Supplies

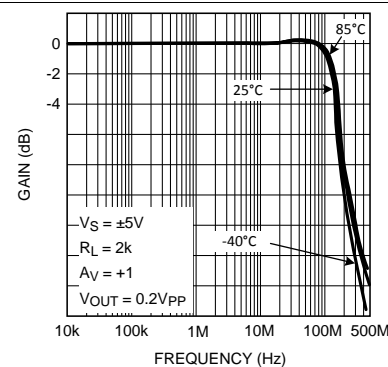


Figure 6. Closed Loop Frequency Response for Various Temperature

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

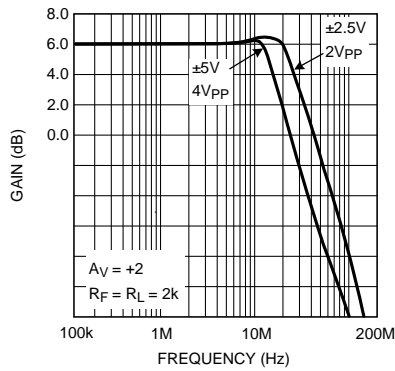


Figure 7. Large Signal Frequency Response

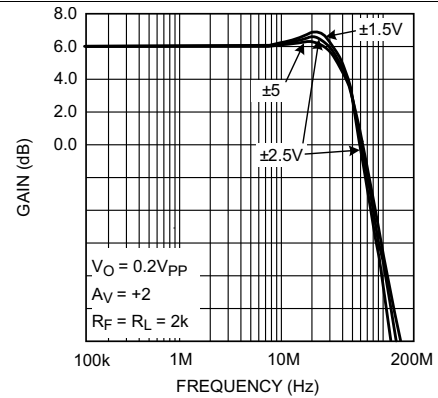


Figure 8. Closed Loop Small Signal Frequency Response for Various Supplies

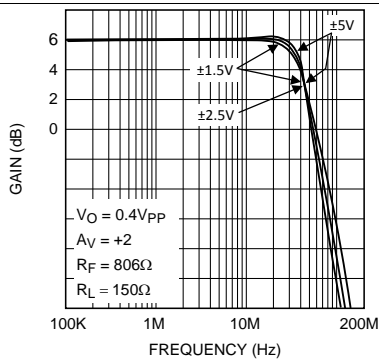


Figure 9. Closed Loop Frequency Response for Various Supplies

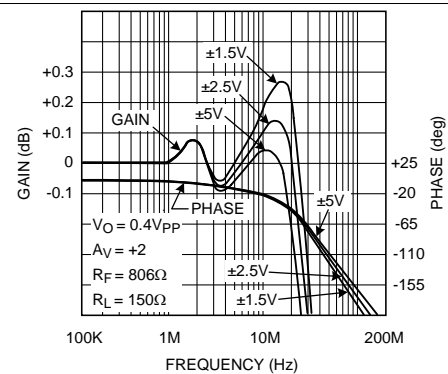


Figure 10. $\pm 0.1\text{dB}$ Gain Flatness for Various Supplies

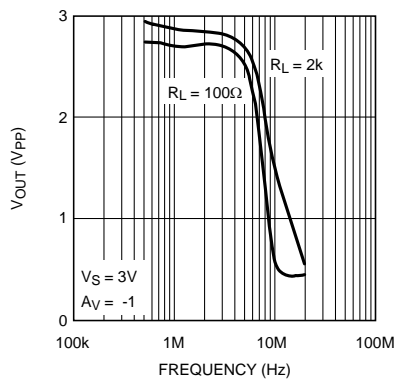


Figure 11. V_{OUT} (V_{PP}) for THD < 0.5%

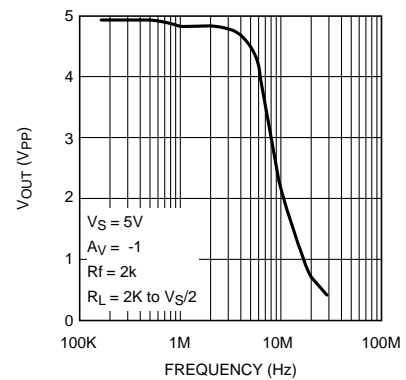


Figure 12. V_{OUT} (V_{PP}) for THD < 0.5%

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

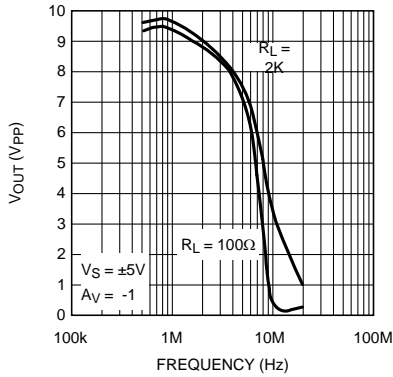


Figure 13. V_{OUT} (V_{PP}) for THD < 0.5%

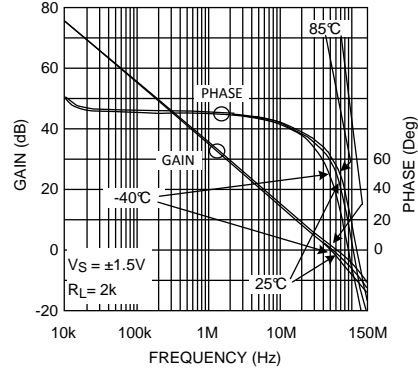


Figure 14. Open Loop Gain/Phase for Various Temperature

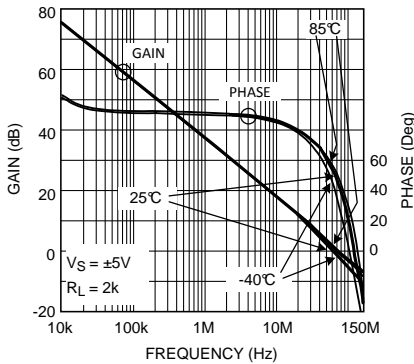


Figure 15. Open Loop Gain/Phase for Various Temperature

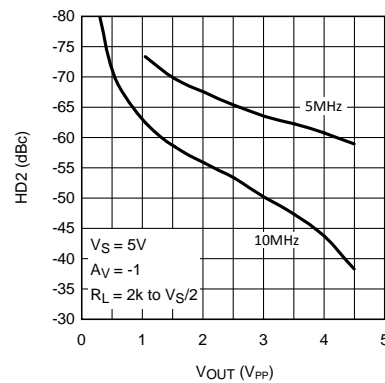


Figure 16. HD2 (dBc) vs. Output Swing

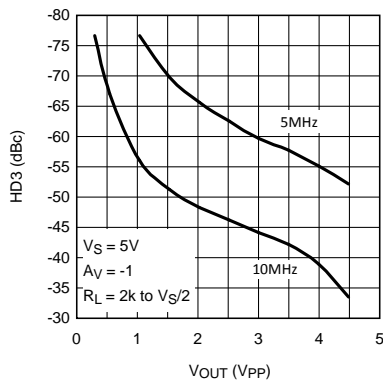


Figure 17. HD3 (dBc) vs. Output Swing

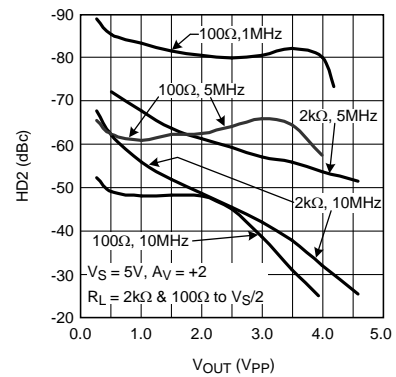


Figure 18. HD2 vs. Output Swing

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

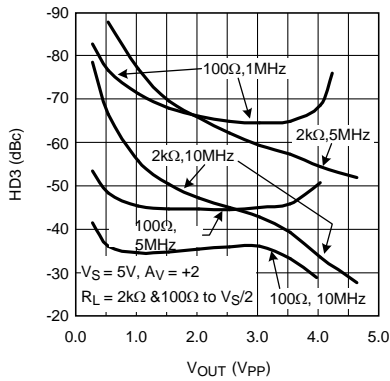


Figure 19. HD3 vs. Output Swing

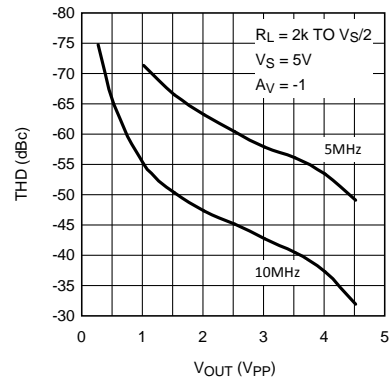


Figure 20. THD (dBc) vs. Output Swing

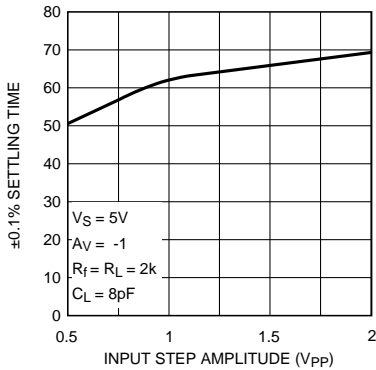


Figure 21. Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)

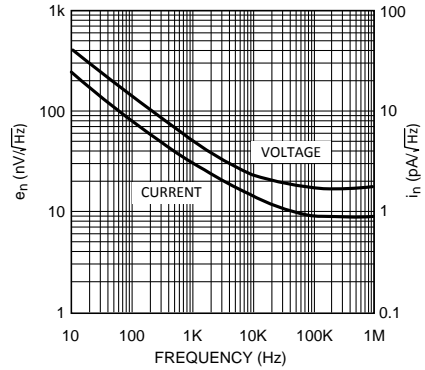


Figure 22. Input Noise vs. Frequency

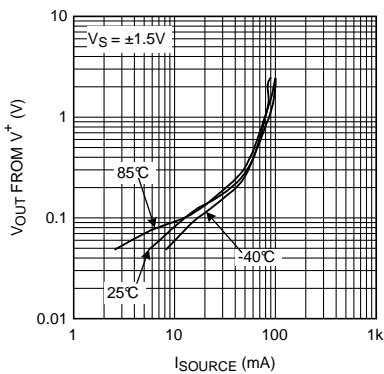


Figure 23. V_{OUT} from V^+ vs. I_{SOURCE}

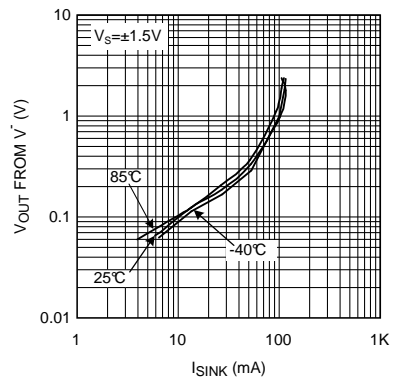


Figure 24. V_{OUT} from V^- vs. I_{SINK}

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

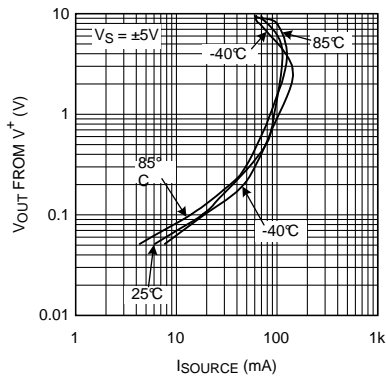


Figure 25. V_{OUT} from V^+ vs. I_{SOURCE}

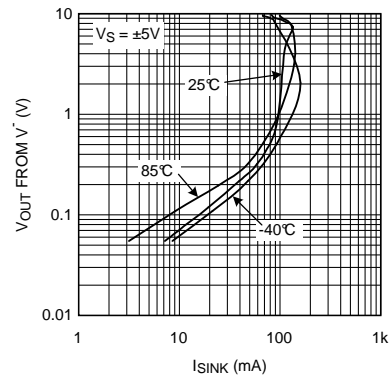


Figure 26. V_{OUT} from V^- vs. I_{SINK}

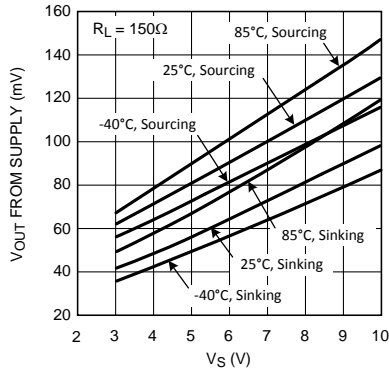


Figure 27. Swing vs. V_S

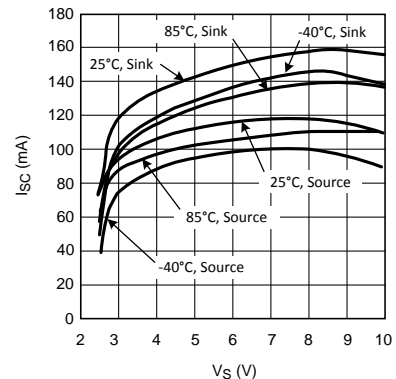


Figure 28. Short Circuit Current (to $V_S/2$) vs. V_S

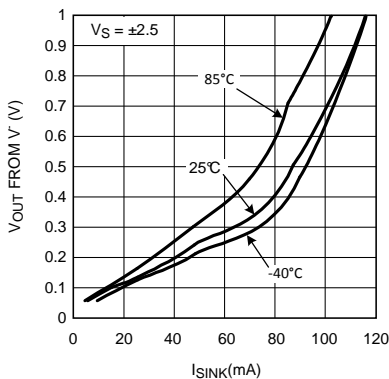


Figure 29. Output Sinking Saturation Voltage vs. I_{OUT}

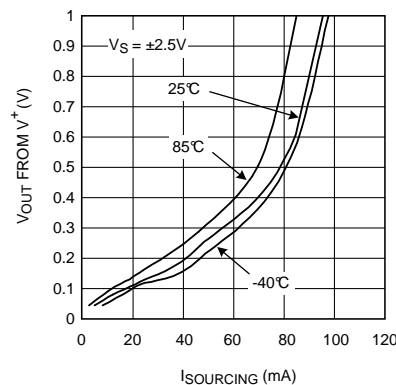


Figure 30. Output Sourcing Saturation Voltage vs. I_{OUT}

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

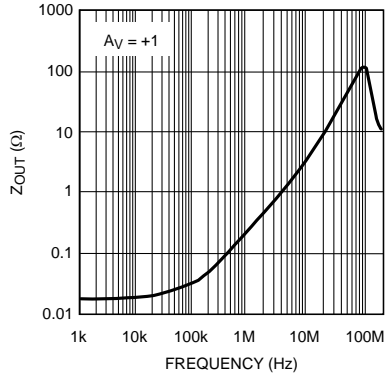


Figure 31. Closed Loop Output Impedance vs. Frequency $A_V = +1$

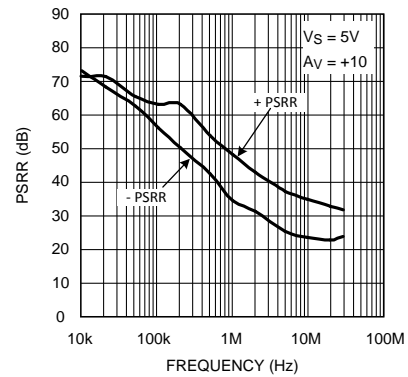


Figure 32. PSRR vs. Frequency

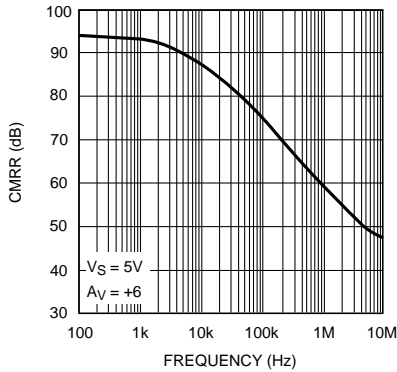


Figure 33. CMRR vs. Frequency

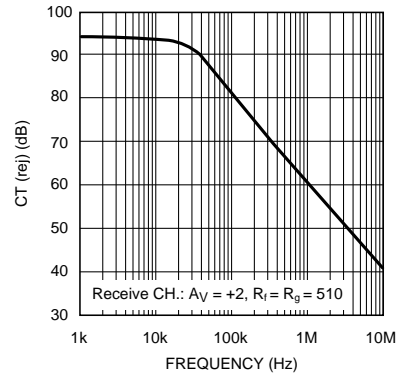


Figure 34. Crosstalk Rejection vs. Frequency (Output to Output)

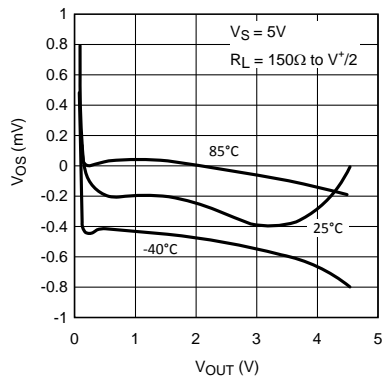


Figure 35. V_{OS} vs. V_{OUT} (Typical Unit)

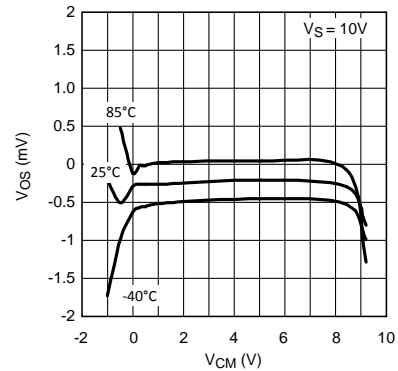


Figure 36. V_{OS} vs. V_{CM} (Typical Unit)

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

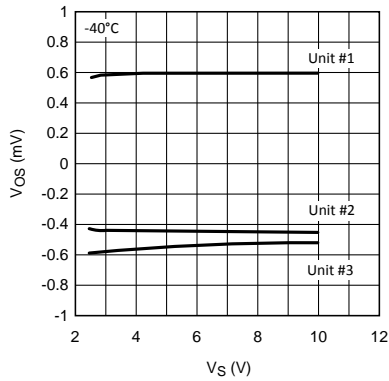


Figure 37. V_{OS} vs. V_S (for 3 Representative Units)

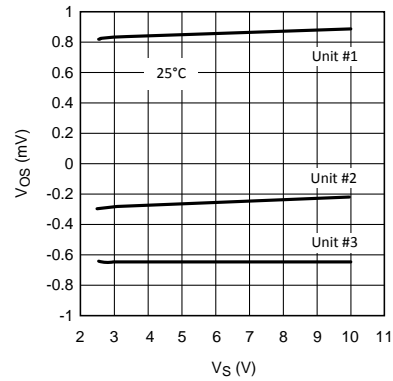


Figure 38. V_{OS} vs. V_S (for 3 Representative Units)

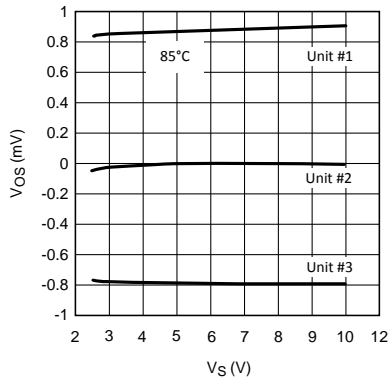


Figure 39. V_{OS} vs. V_S (for 3 Representative Units)

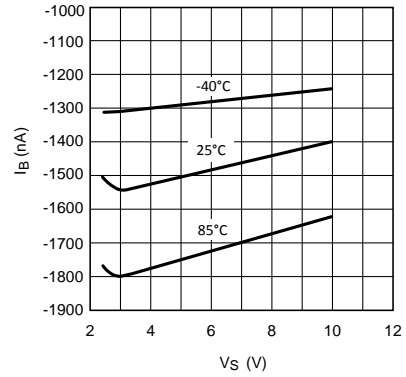


Figure 40. I_B vs. V_S

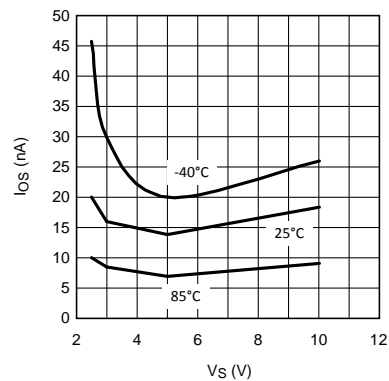


Figure 41. I_{OS} vs. V_S

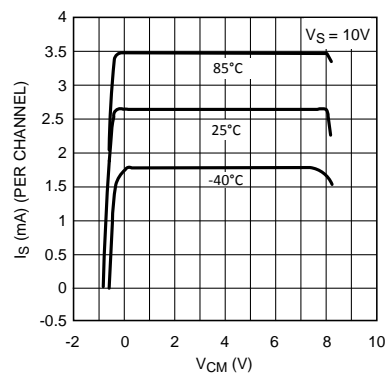


Figure 42. I_S vs. V_{CM}

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

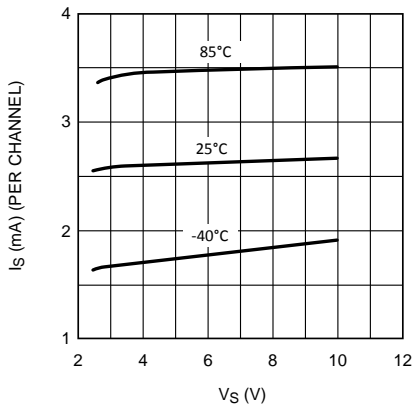


Figure 43. I_S vs. V_S

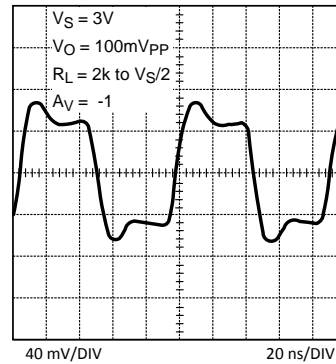


Figure 44. Small Signal Step Response

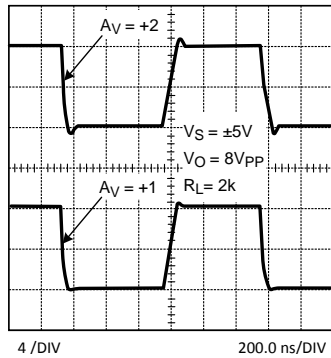


Figure 45. Large Signal Step Response

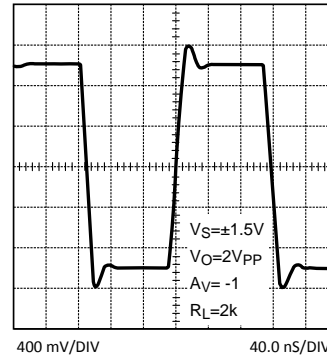


Figure 46. Large Signal Step Response

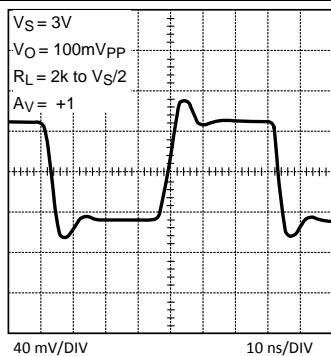


Figure 47. Small Signal Step Response

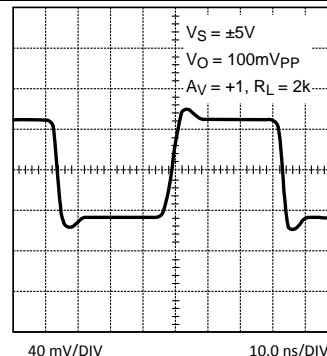
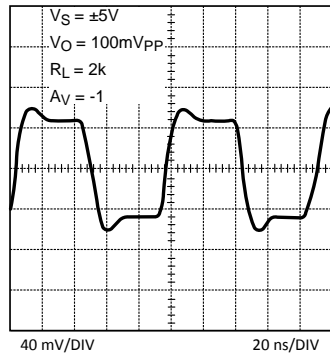
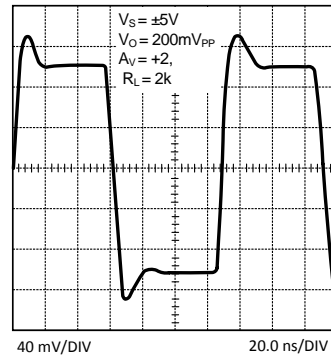
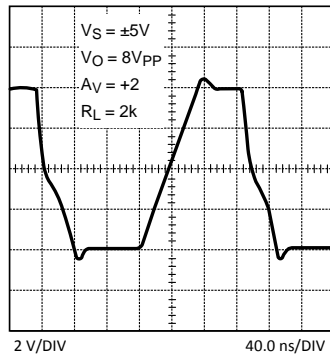
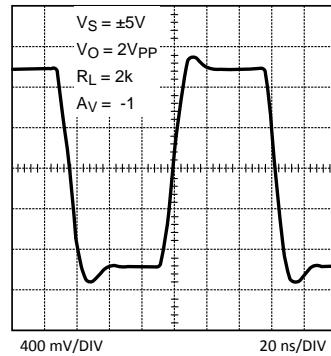
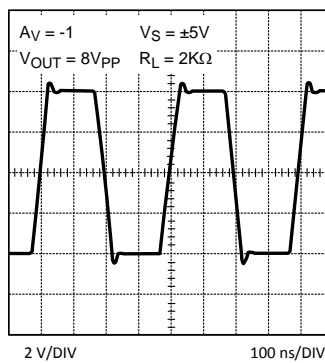


Figure 48. Small Signal Step Response

Typical Performance Characteristics (continued)
 $V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2\text{ k}\Omega$. Unless otherwise specified.

Figure 49. Small Signal Step Response

Figure 50. Small Signal Step Response

Figure 51. Large Signal Step Response

Figure 52. Large Signal Step Response

Figure 53. Large Signal Step Response

8 Detailed Description

8.1 Overview

The LMH664X family is based on proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7 V) and low bias current.
- A class A-B “turn-around” stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75 mA output current (at 0.5 V from the supply rails) while consuming only 2.7 mA of total supply current per channel. This architecture allows output to reach within mV of either supply rail.
- Consistent performance over the entire operating supply voltage range with little variation for the most important specifications (for example, BW, SR, I_{OUT} , and so forth)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

8.2 Functional Block Diagram

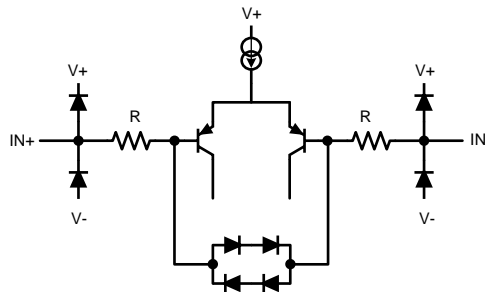


Figure 54. Input Equivalent Circuit

8.3 Feature Description

The LMH664X family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664X will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family’s specified parameters are included in the list of LMH664X ensured specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

8.4 Device Functional Modes

With 3-V supplies and a common mode input voltage range that extends 0.5 V below V^- , the LMH664X find applications in low voltage/low power applications. Even with 3-V supplies, the -3dB BW (@ $A_V = +1$) is typically 115 MHz with a tested limit of 80 MHz. Production testing guarantees that process variations will not compromise speed. High frequency response is exceptionally stable, confining the typical -3dB BW over the industrial temperature range to $\pm 2.5\%$.

As seen in [Typical Performance Characteristics](#), the LMH664X output current capability (~75 mA) is enhanced compared to AD805X. This enhancement increases the output load range, adding to the LMH664X’s versatility. Since LMH664X is capable of high output current, device junction temperature should not to exceed the Absolute Maximum Ratings.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See [Figure 56](#).

However, if the input voltage range of -0.5 V to 1 V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10 mA .

Output overdrive recovery time is less than 100 ns as can be seen in [Figure 57](#).

9.2 Typical Application

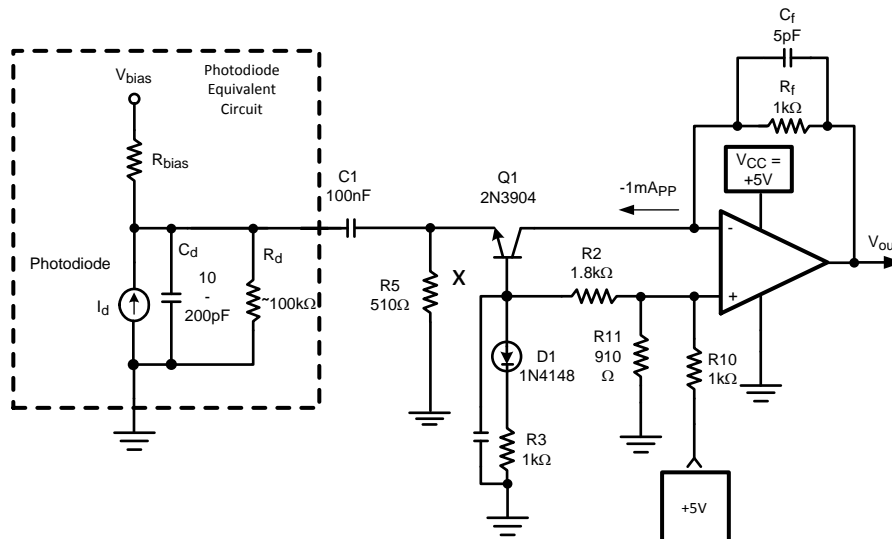


Figure 55. Single Supply Photodiode I-V Converter

9.2.1 Design Requirements

The circuit shown in [Figure 55](#) is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application. This circuit achieves approximately 1 V/mA of transimpedance gain and capable of handling up to 1 mA_{pp} from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5-V single supply, the device input/output is shifted to near half supply using a voltage divider from VCC. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

Typical Application (continued)

9.2.1.1 Input and Output Topology

All input / output pins are protected against excessive voltages by ESD diodes connected to V^+ and V^- rails (see [Figure 54](#)). These diodes start conducting when the input / output pin voltage approaches $1V_{be}$ beyond V^+ or V^- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in [Figure 54](#)), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching $2V_{be}$. This occurs most commonly when the device is used as a comparator (or with little or no feedback) and the device inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases and the differential input voltage is clamped. It is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through this protection circuit, extra series resistors can be placed. Together with the built-in series resistors of several hundred ohms, these external resistors can limit the input current to a safe number (that is, less than 10mA). Be aware that these input series resistors may impact the switching speed of the device and could slow down the device.

9.2.1.2 Single Supply, Low Power Photodiode Amplifier

The circuit shown in [Figure 55](#) is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC} . Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilize the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT} \left[\frac{C_{IN}}{2\pi \cdot \text{GBWP} \cdot R_F} \right]$$

where

- GBWP is the Gain Bandwidth Product of the Op Amp (1)

Optimized as such, the I-V converter will have a theoretical pole, f_p , at:

$$f_p = \text{SQRT} \left[\frac{\text{GBWP}}{2\pi R_F \cdot C_{IN}} \right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, $C_{IN} = 6$ pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57 MHz. Therefore, with $R_f = 1k$, from [Equation 1](#) and [Equation 2](#):

$$C_f = \sim 4.1 \text{ pF and } f_p = 39 \text{ MHz} \quad (3)$$

For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in [Figure 58](#) below showing about 9 ns rise/fall times, corresponding to about 39 MHz for f_p . The overall supply current from the +5 V supply is around 5 mA with no load.

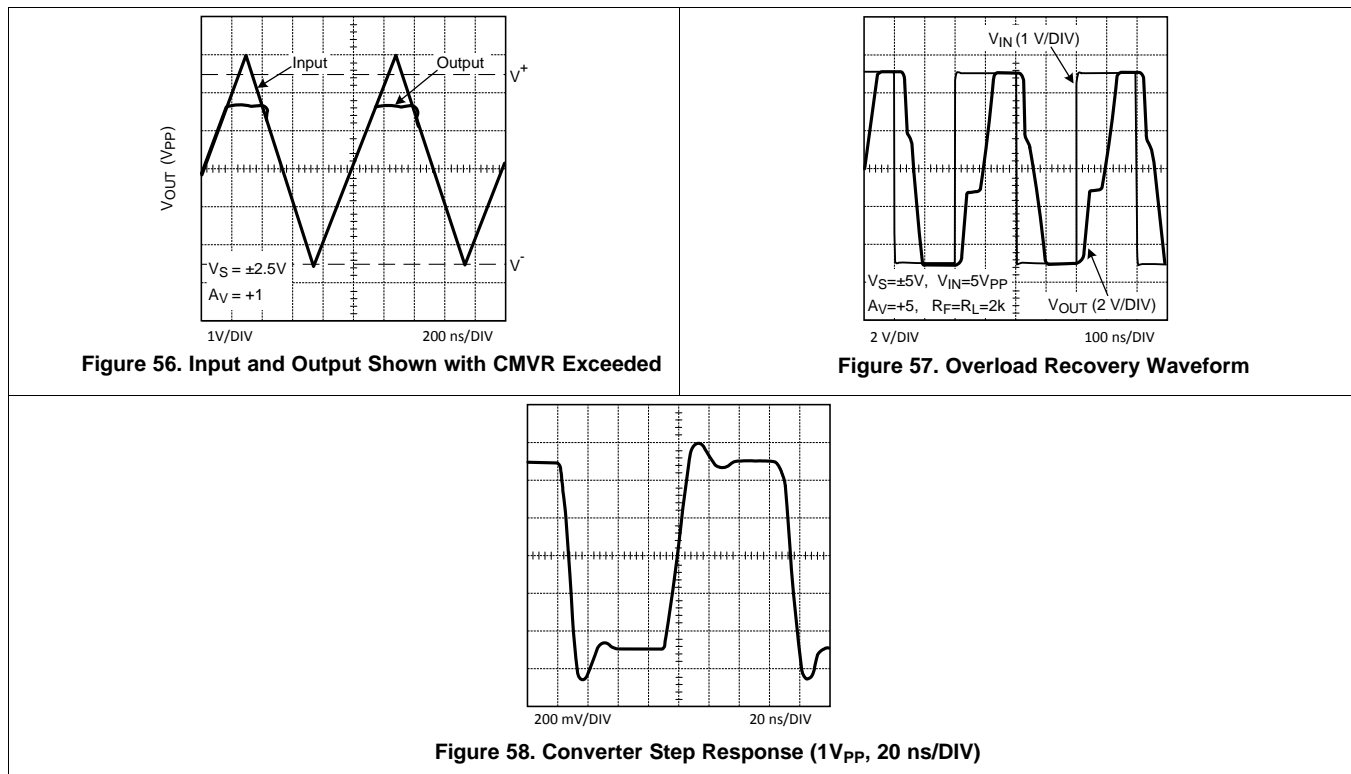
Typical Application (continued)

9.2.2 Detailed Design Procedure

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilize the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin where GBWP is the Gain Bandwidth Product of the Op Amp, Optimized as such, the I-V converter will have a theoretical pole, f_p , at: (2) With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, $C_{IN} = 6$ pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57 MHz. Therefore, with $R_f = 1k$, from Equation 2 and Equation 3 : $C_f = \sim 4.1$ pF and $f_p = 39$ MHz.

Single Supply Photodiode I-V Converter For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in Figure 58 showing about 9 ns rise/fall times, corresponding to about 39 MHz for f_p . The overall supply current from the +5 V supply is around 5 mA with no load.

9.2.3 Application Curves



10 Power Supply Recommendations

The LMH664x device family can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends all the way down to the V_- rail to simplify single supply applications. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

11 Layout

11.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers", [SNOA367](#), for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Table 1. Printed Circuit Board Layout And Component Values

DEVICE	PACKAGE	EVALUATION BOARD PN
LMH6642MF	5-Pin SOT-23	LMH730216
LMH6642MA	8-Pin SOIC	LMH730227
LMH6643MA	8-Pin SOIC	LMH730036
LMH6643MM	8-Pin VSSOP	LMH730123
LMH6644MA	14-Pin SOIC	LMH730231
LMH6644MT	14-Pin TSSOP	LMH730131

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

11.2 Layout Example

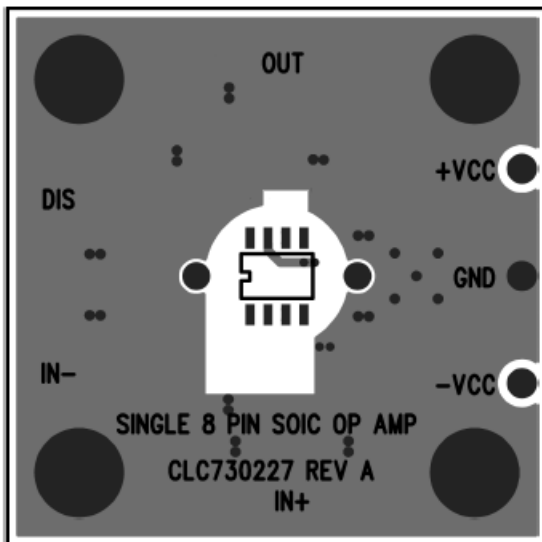


Figure 59. LMH6642/LMH6643/LMH6644 Layer 1

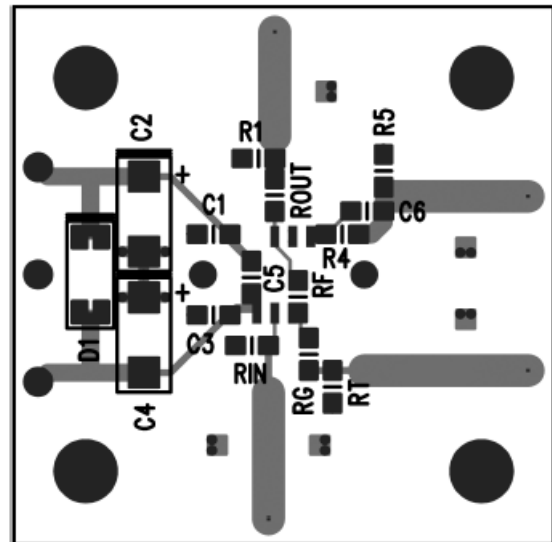


Figure 60. LMH6642/LMH6643/LMH6644 Layer 2

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6642	Click here	Click here	Click here	Click here	Click here
LMH6643	Click here	Click here	Click here	Click here	Click here
LMH6644	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6642MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA	Samples
LMH6642MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA	Samples
LMH6642MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A64A	
LMH6642MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A64A	Samples
LMH6642MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A64A	Samples
LMH6643MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 43MA	
LMH6643MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA	Samples
LMH6643MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA	Samples
LMH6643MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A65A	
LMH6643MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A65A	Samples
LMH6643MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A65A	Samples
LMH6644MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA	Samples
LMH6644MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA	Samples
LMH6644MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT	Samples
LMH6644MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6642MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6642MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6643MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6643MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6643MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6643MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6644MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6644MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMH6644MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6642MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6642MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6642MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6643MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6643MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6643MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6643MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6644MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMH6644MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMH6644MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

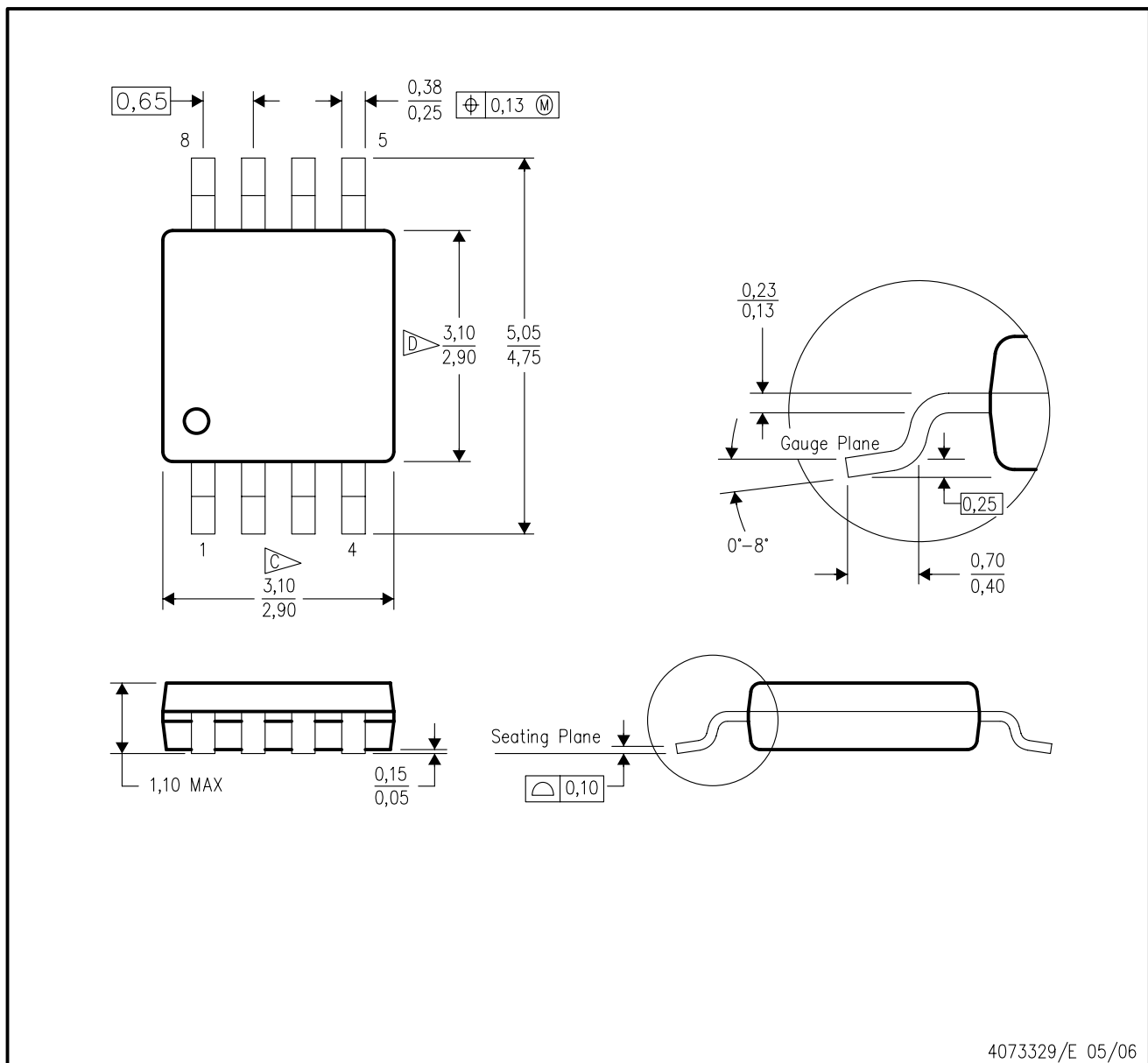
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.