LMH664x 2.7 V, 650 µA, 55 MHz, Rail-to-Rail Input and Output Amplifiers with Shutdown Option

1 Features

- (V_S = 2.7V, T_A = 25°C, R_L = 1kΩ to V^+/2, A_V = +1. Typical Values Unless Specified.
- −3dB BW 55 MHz
- Supply Voltage Range 2.5 V to 12 V
- Slew Rate 22 V/µs
- Supply Current 650 µA/channel
- Output Short Circuit Current 42 mA
- Linear Output Current ±20 mA
- Input Common Mode Voltage 0.3 V Beyond Rails
- Output Voltage Swing 20 mV from Rails
- Input Voltage Noise 17 nV/√Hz
- Input Current Noise 0.75 pA/√Hz

2 Applications

- Active Filters
- High Speed Portable Devices
- Multiplexing Applications (LMH6647)
- Current Sense Buffer
- High Speed Transducer Amp

3 Description

The LMH6645 (single) and LMH6646 (dual), rail-to-rail input and output voltage feedback amplifiers, offer high speed (55 MHz), and low voltage operation (2.7 V) in addition to micro-power shutdown capability (LMH6647, single).

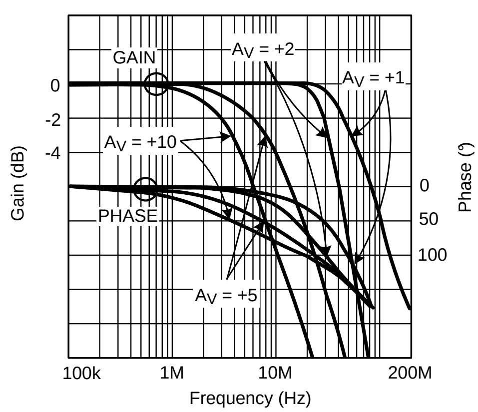
Input common mode voltage range exceeds either supply by 0.3 V, enhancing ease of use in multitude of applications where previously only inferior devices could be used. Output voltage range extends to within 20 mV of either supply rails, allowing wide dynamic range especially in low voltage applications. Even with low supply current of 650 µA/amplifier, output current capability is kept at a respectable ±20 mA for driving heavier loads. Important device parameters such as BW, Slew Rate and output current are kept relatively independent of the operating supply voltage by a combination of process enhancements and design architecture.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6645	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
LMH6646	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LMH6647	SOT-23 (6)	2.92 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Frequency Response for Various A_V



Closed Loop Frequency Response for Various Temperature

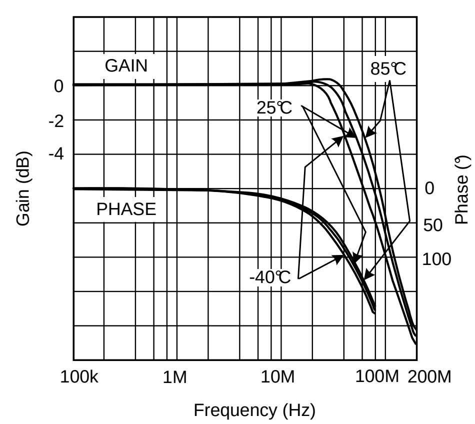


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D **Page**

- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support; Mechanical, Packaging, and Ordering Information*.......... 1

Changes from Revision B (April 2013) to Revision C **Page**

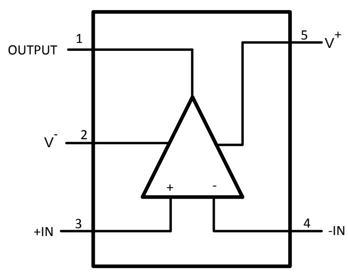
- Changed layout of National Data Sheet to TI format 1

5 Description (continued)

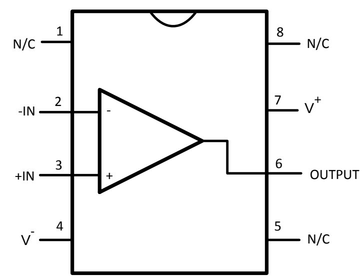
In portable applications, the LMH6647 provides shutdown capability while keeping the turn-off current to less than 50 µA. Both turn-on and turn-off characteristics are well behaved with minimal output fluctuations during transitions. This allows the part to be used in power saving mode, as well as multiplexing applications. Miniature packages (SOT-23, VSSOP-8, and SOIC-8) are further means to ease the adoption of these low power high speed devices in applications where board area is at a premium.

6 Pin Configuration and Functions

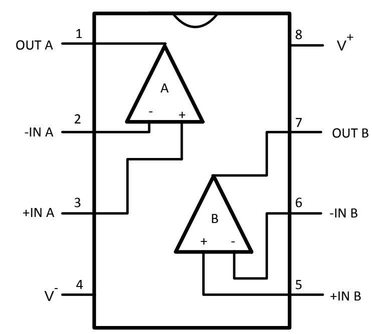
SOT-23-5 (LMH6645)
Package DBV05A
Top View



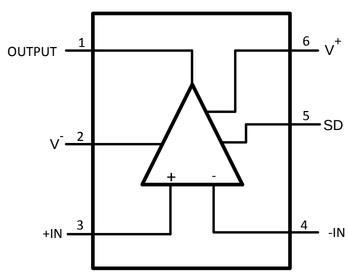
SOIC-8 (LMH6645)
Package D08A
Top View



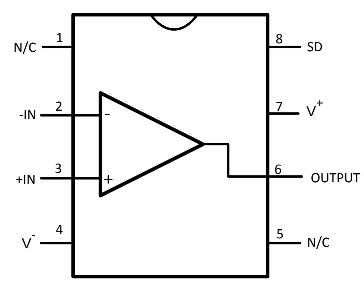
SOIC-8 and VSSOP-8 (LMH6646)
Packages D08A and DGK08A
Top View



SOT-23-6 (LMH6647)
Package DBV06A
Top View



SOIC-8 (LMH6647)
Package D08A
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	NUMBER						
	LMH6645		LMH6646	LMH6647			
	DBV05A	D08A	DGK08A	DBV06A	D08A		
-IN	4	2		4	2	I	Inverting input
+IN	3	3		3	3	I	Non-inverting input
-IN A			2			I	Inverting Input Channel A
+IN A			3			I	Non-inverting input Channel A
-IN B			6			I	Inverting input Channel B
+IN B			5			I	Non-inverting input Channel B
N/C		1,5,8			1,5	—	No Connection
OUTPUT	1	6		1	6	O	Output
OUT A			1			O	Output Channel A
OUT B			7			O	Output Channel B
SD				5	8	I	Shutdown
V^-	2	4	4	2	4	I	Negative Supply
V+	5	7	8	6	7	I	Positive Supply

7 Specifications

7.1 Absolute Maximum Ratings [1][2]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Output short circuit duration			See [3] and [4]	
V_{IN} differential			±2.5	V
Voltage at input/output pins			V^+ +0.8, V^- −0.8	V
Supply voltage (V^+ - V^-)			12.6	V
Junction temperature [5]			+150	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering (10 sec)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Output short circuit duration is infinite for V_S < 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]		2000	V
		Machine model (MM) [2]		200	V

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Human body model, 1.5 kΩ in series with 100pF.
(2) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process. Machine model, 0 Ω in series with 200 pF.

7.3 Recommended Operating Conditions [1]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ – V^-)	2.5	12	V
Temperature Range [2]	−40	+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

THERMAL METRIC [1]		LMH6645		LMH6646		LMH6647		UNIT
		SOT-23		SOIC-8	VSSOP-8	SOT-23	SOIC-8	
		5 PINS	8 PINS	8 PINS	8 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265	190	190	235	265	190	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics 2.7 V

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_f = 2kΩ, and R_L = 1kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
BW	−3dB BW	A_V = +1, V_{OUT} = 200 mV_{PP}, V_{CM} = 0.7 V		40	55		MHz
e_n	Input-referred voltage noise	f = 100 kHz			17		nV/√Hz
		f = 1 kHz			25		
i_n	Input-referred current noise	f = 100 kHz			0.75		pA/√Hz
		f = 1 kHz			1.20		
CT Rej.	Cross-talk rejection (LMH6646 only)	f = 5MHz, Receiver: R_f = R_g = 510 Ω, A_V = +2			47		dB
SR	Slew rate	A_V = −1, V_O = 2 V_{PP} See (3), (4)		15	22		V/μs
T_{ON}	Turn-on time (LMH6647 only)				250		ns
T_{OFF}	Turn-off time (LMH6647 only)				560		ns
TH_{SD}	Shutdown threshold (LMH6647 only)	I_S ≤ 50μA			1.95	2.30	V
I_{SD}	Shutdown pin input current (LMH6647 only)	See (5)			−20		μA
V_{OS}	Input offset voltage	0V ≤ V_{CM} ≤ 2.7 V		−3	±1	3	mV
			-40°C ≤ T_J ≤ 85°C	−4		4	
TC V_{OS}	Input offset average drift	See (6)			±5		μV/°C
I_B	Input bias current	V_{CM} = 2.5 V (5)			0.40	2	μA
			-40°C ≤ T_J ≤ 85°C			2.2	
		V_{CM} = 0.5 V (5)			−0.68	−2	
			-40°C ≤ T_J ≤ 85°C			−2.2	
I_{OS}	Input offset current	0 V ≤ V_{CM} ≤ 2.7 V			1	500	nA
R_{IN}	Common mode input resistance				3		MΩ
C_{IN}	Common mode input capacitance				2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			−0.5	−0.3	V
			-40°C ≤ T_J ≤ 85°C			−0.1	
				3.0	3.2		
			-40°C ≤ T_J ≤ 85°C	2.8			
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 2.7 V		46	77		dB
		V_{CM} Stepped from 0 V to 1.55 V		58	76		
A_{VOL}	Large signal voltage gain	V_O = 0.35 V to 2.35 V		76	87		dB
			-40°C ≤ T_J ≤ 85°C	74			
V_O	Output swing high	R_L = 1k to $V^+/2$		2.55	2.66		V
		R_L = 10k to $V^+/2$			2.68		
	Output swing low	R_L = 1k to $V^+/2$			40	150	mV
		R_L = 10k to $V^+/2$			20		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) ensured based on characterization only.
(5) Positive current corresponds to current flowing into the device.
(6) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_f = 2kΩ, and R_L = 1kΩ to V^+/2.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_{SC}	Output short circuit current	Sourcing to V^- V_{ID} = 200mV (7)(8)		43		mA
		Sinking to V^+ V_{ID} = −200mV (7)(8)		42		
I_{OUT}	Output current	V_{OUT} = 0.5V from rails		±20		mA
PSRR	Power supply rejection ratio	V^+ = 2.7V to 3.7V or V^- = 0V to −1V	75	83		dB
I_S	Supply current (per channel)	Normal Operation		650	1250	μA
		Shutdown Mode (LMH6647 only)		15	50	

(7) Short circuit test is a momentary test.
(8) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

7.6 Electrical Characteristics 5V

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_f = 2kΩ, and R_L = 1kΩ to $V^+/2$.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
BW	−3dB BW	A_V = +1, V_{OUT} = 200 mV_{PP}		40	55		MHz
e_n	Input-referred voltage noise	f = 100kHz			17		nV/√Hz
		f = 1kHz			25		
i_n	Input-referred current noise	f = 100kHz			0.75		pA/√Hz
		f = 1kHz			1.20		
CT Rej.	Cross-talk rejection (LMH6646 only)	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2			47		dB
SR	Slew rate	A_V = −1, V_O = 2 V_{PP} See (3), (4)		15	22		V/μs
T_{ON}	Turn-on time (LMH6647 only)				210		ns
T_{OFF}	Turn-off time (LMH6647 only)				500		ns
TH_{SD}	Shutdown threshold (LMH6647 only)	I_S ≤ 50μA			4.25	4.60	V
I_{SD}	Shutdown pin input current (LMH6647 only)	See (5)			−20		μA
V_{OS}	Input offset voltage	0V ≤ V_{CM} ≤ 5V		−3	±1	3	mV
			-40°C ≤ T_J ≤ 85°C	−4		4	
TC V_{OS}	Input offset average drift	See (6)			±5		μV/C
I_B	Input bias current	V_{CM} = 4.8V (5)			+0.36	+2	μA
			-40°C ≤ T_J ≤ 85°C			−2.2	
		V_{CM} = 0.5V (5)			−0.68	−2	
			-40°C ≤ T_J ≤ 85°C			−2.2	
I_{OS}	Input offset current	0V ≤ V_{CM} ≤ 5V			1	500	nA
R_{IN}	Common mode input resistance				3		MΩ
C_{IN}	Common mode input capacitance				2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			−0.5	−0.3	V
			-40°C ≤ T_J ≤ 85°C			−0.1	
				5.3	5.5		
			-40°C ≤ T_J ≤ 85°C	5.1			
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0V to 5V		56	82		dB
		V_{CM} Stepped from 0V to 3.8V		66	85		
A_{VOL}	Large signal voltage gain	V_O = 1.5V to 3.5V		76	85		dB
			-40°C ≤ T_J ≤ 85°C	74			

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) ensured based on characterization only.
(5) Positive current corresponds to current flowing into the device.
(6) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Electrical Characteristics 5V (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_f = 2kΩ, and R_L = 1kΩ to V^+/2.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output swing high	R_L = 1k to V^+/2	4.80	4.95		V
		R_L = 10k to V^+/2		4.98		
	Output swing low	R_L = 1k to V^+/2		50	200	mV
		R_L = 10k to V^+/2		20		
I_{SC}	Output short circuit current	Sourcing to V^- V_{ID} = 200mV (7)(8)		55		mA
		Sinking to V^+ V_{ID} = −200mV (7)(8)		53		
I_{OUT}	Output current	V_{OUT} = 0.5V From rails		±20		mA
PSRR	Power supply rejection ratio	V^+ = 5V to 6V or V^- = 0V to −1V	75	95		dB
I_S	Supply current (per channel)	Normal Operation		700	1400	μA
		Shutdown Mode (LMH6647 only)		10	50	

(7) Short circuit test is a momentary test.
(8) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

7.7 Electrical Characteristics ±5V

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, R_f = 2kΩ, and R_L = 1kΩ to GND.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
BW	−3dB BW	A_V = +1, V_{OUT} = 200 mV_{PP}		40	55		MHz
e_n	Input-referred voltage noise	f = 100 kHz			17		nV/√Hz
		f = 1 kHz			25		
i_n	Input-referred current noise	f = 100 kHz			0.75		pA/√Hz
		f = 1 kHz			1.20		
CT Rej.	Cross-talk rejection (LMH6646 only)	f = 5MHz, Receiver: R_f = R_g = 510 Ω, A_V = +2			47		dB
SR	Slew rate	A_V = −1, V_O = 2 V_{PP} (3)		15	22		V/µs
T_{ON}	Turn-on time (LMH6647 only)				200		ns
T_{OFF}	Turn-off time (LMH6647 only)				700		ns
TH_{SD}	Shutdown threshold (LMH6647 only)	I_S ≤ 50 µA			4.25	4.60	V
I_{SD}	Shutdown pin input current (LMH6647 only)	See (4)			−20		µA
V_{OS}	Input offset voltage	−5V ≤ V_{CM} ≤ 5 V		−3	±1	3	mV
			-40°C ≤ T_J ≤ 85°C	−4		4	
TC V_{OS}	Input offset average drift	See (5)			±5		µV/°C
I_B	Input bias current	V_{CM} = 4.8 V (4)			+0.40	+2	µA
			-40°C ≤ T_J ≤ 85°C			+2.2	
		V_{CM} = −4.5 V (4)			−0.65	−2	
			-40°C ≤ T_J ≤ 85°C			−2.2	
I_{OS}	Input offset current	−5V ≤ V_{CM} ≤ 5 V			3	500	nA
R_{IN}	Common mode input resistance				3		MΩ
C_{IN}	Common mode input capacitance				2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			−5.5	−5.3	V
			-40°C ≤ T_J ≤ 85°C			−5.1	
				5.3	5.5		
			-40°C ≤ T_J ≤ 85°C	5.1			
CMRR	Common mode rejection ratio	V_{CM} Stepped from −5 V to 5 V		60	84		dB
		V_{CM} Stepped from −5 V to 3.5 V		66	104		
A_{VOL}	Large signal voltage gain	V_O = −2 V to 2 V		76	85		dB
			-40°C ≤ T_J ≤ 85°C	74			

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Positive current corresponds to current flowing into the device.
(5) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Electrical Characteristics ±5V (continued)

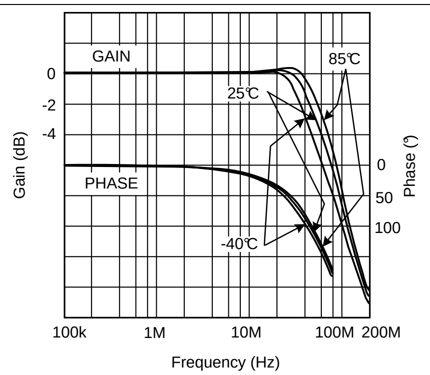
Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, R_f = 2kΩ, and R_L = 1kΩ to GND.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output swing high	R_L = 1 kΩ	4.70	4.92		V
		R_L = 10 kΩ		4.97		
	Output swing low	R_L = 1 kΩ		−4.93	−4.70	V
		R_L = 10 kΩ		−4.98		
I_{SC}	Output short circuit current	Sourcing to V^- V_{ID} = 200 mV(6)(7)		66		mA
		Sinking to V^+ V_{ID} = −200 mV(6)(7)		61		
I_{OUT}	Output current	V_{OUT} = 0.5V from rails		±20		mA
PSRR	Power supply rejection ratio	V^+ = 5 V to 6 V or V^- = −5 V to −6 V	76	95		dB
I_S	Supply current (per channel)	Normal Operation		725	1600	μA
		Shutdown Mode (LMH6647 only)		10	50	

(6) Short circuit test is a momentary test.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

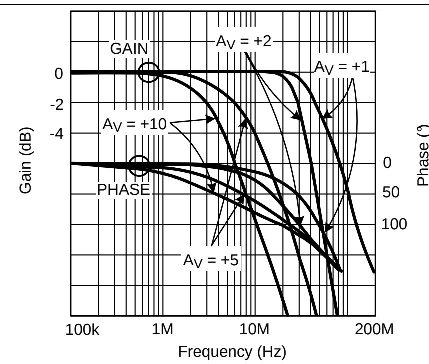
7.8 Typical Performance Characteristics

At T_J = 25°C. Unless otherwise specified.



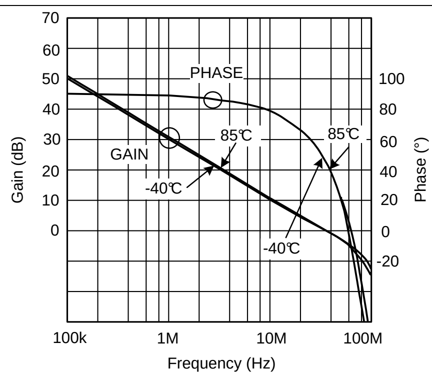
A_V = + 1 V_S = ±2.5 V R_L = 1k
V_{OUT} = 200 mVpp

Figure 1. Closed Loop Frequency Response for Various Temperature



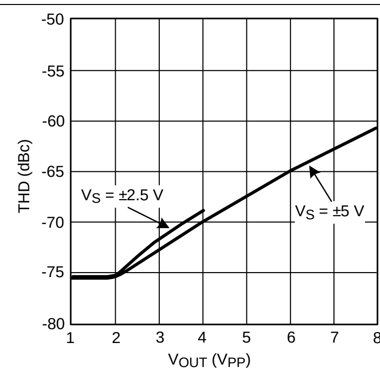
V_S = ±5 V R_L = 1 kΩ

Figure 2. Frequency Response for Various A_V



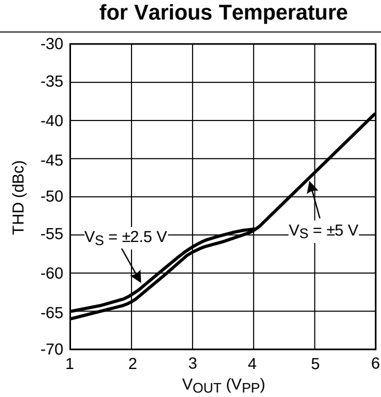
V_S = ±2.5 V R_L = 2k

Figure 3. Open Loop Gain/Phase vs. Frequency for Various Temperature



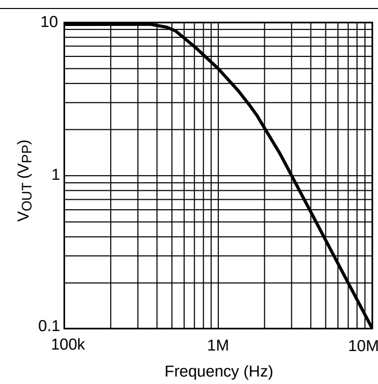
R_L = 500 Ω f = 100 KHz A_V = +2

Figure 4. THD vs. Output Swing



R_L = 500 Ω f = 1 MHz A_V = +2

Figure 5. THD vs. Output Swing

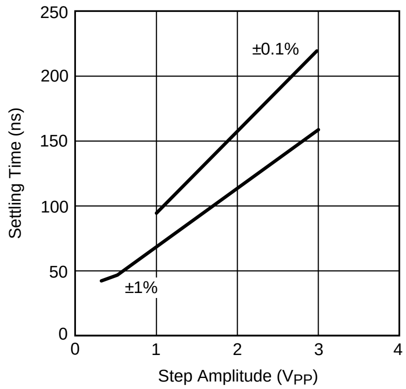


R_L = 500 Ω A_V = +2 V_S = ±5 V
R_f = R_g = 2K

Figure 6. Output Swing vs. Frequency

Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.



V_S = ±2.5 V   RL = 500 Ω C_L = 13 pF
A_V = -1

Figure 7. Settling Time vs. Step Size

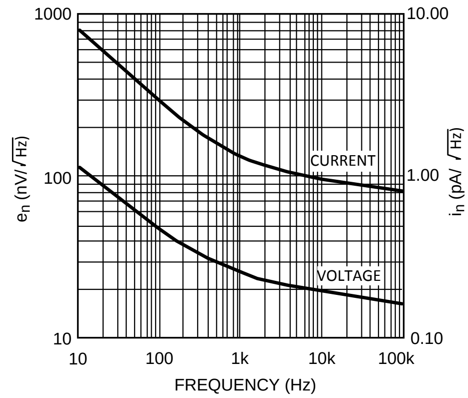
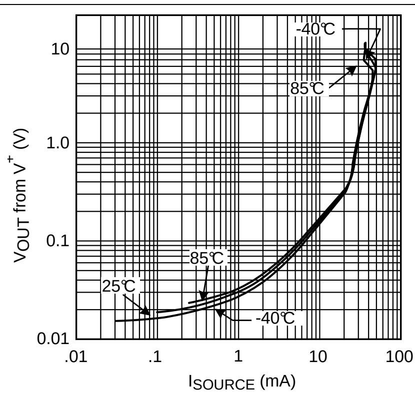
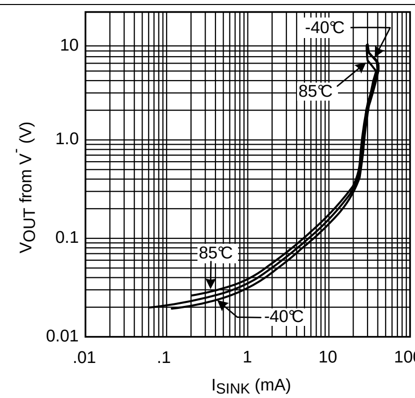


Figure 8. Noise vs. Frequency



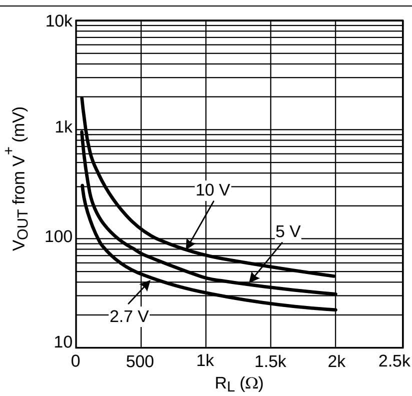
V_S = 10 V

Figure 9. V_{OUT} from V^+ vs. I_{SOURCE}



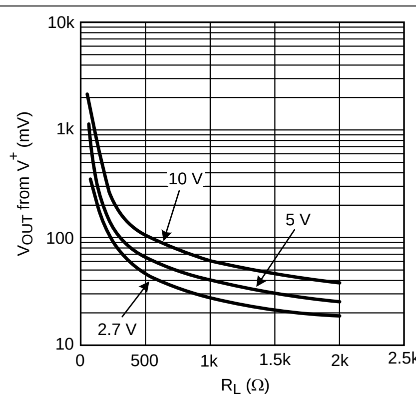
V_S = 10 V

Figure 10. V_{OUT} from V^- vs. I_{SINK}



T = 25°C A_V = +1

Figure 11. Output Swing from V^+ vs. R_L (tied to V_S/2)



T = -40°C A_V = +1

Figure 12. Output Swing from V^+ vs. R_L (Tied to V_S/2)

Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.

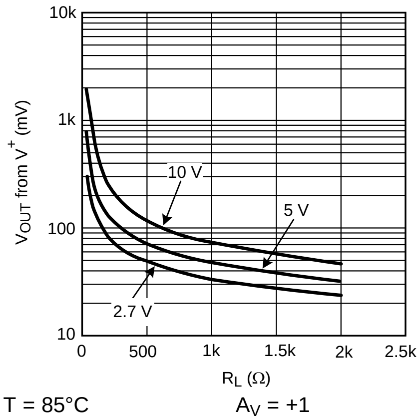


Figure 13. Output Swing from V^+ vs. R_L (Tied to V_S/2)

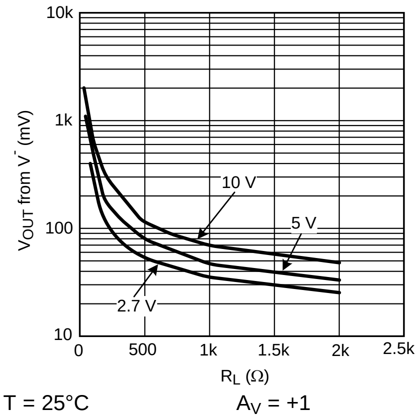


Figure 14. Output Swing from V^- vs. R_L (Tied to V_S/2)

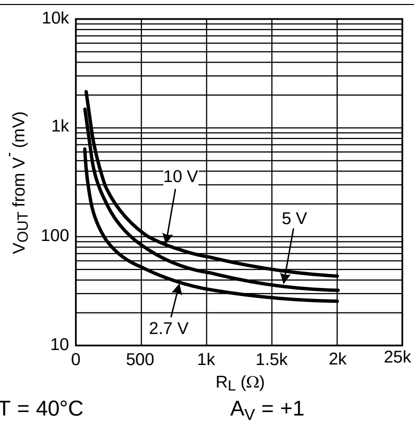


Figure 15. Output Swing from V^- vs. R_L (Tied to V_S/2)

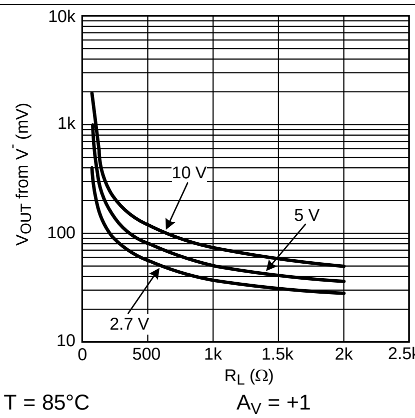


Figure 16. Output Swing from V^- vs. R_L (Tied to V_S/2)

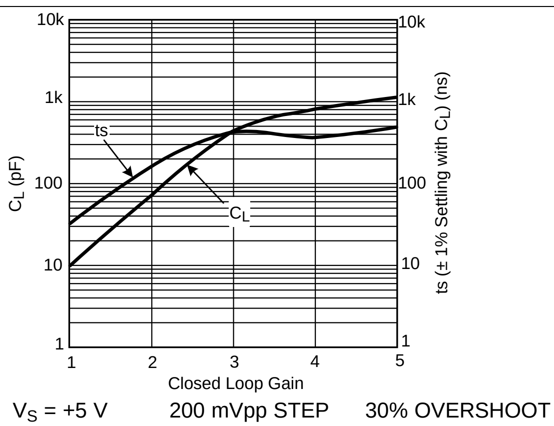


Figure 17. Cap Load Tolerance and Setting Time vs. Closed Loop Gain

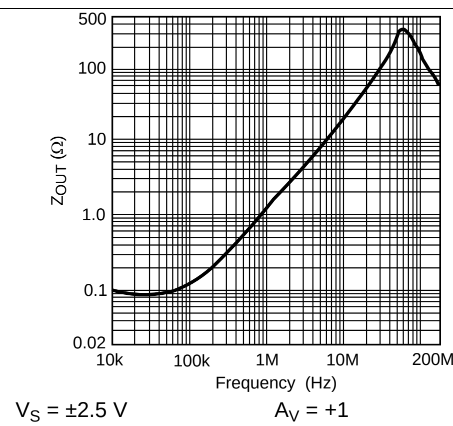
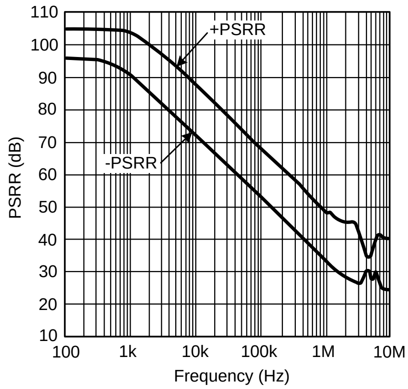


Figure 18. Z_{OUT} vs. Frequency

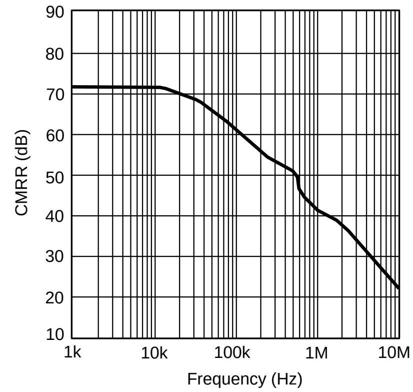
Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.



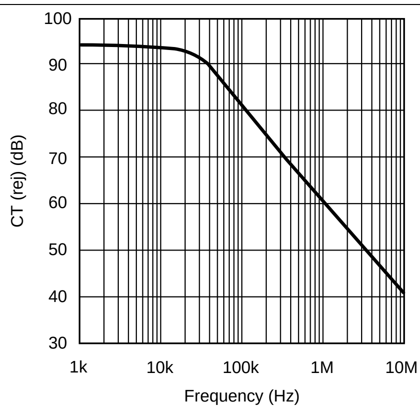
V_S = ±2.5V R_F = 10 kΩ R_G = 1 kΩ

Figure 19. PSRR vs. Frequency



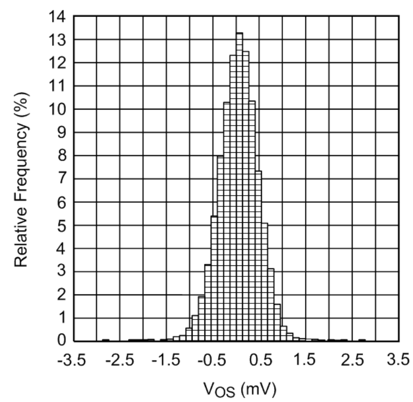
V_S = 5 V

Figure 20. CMRR vs. Frequency



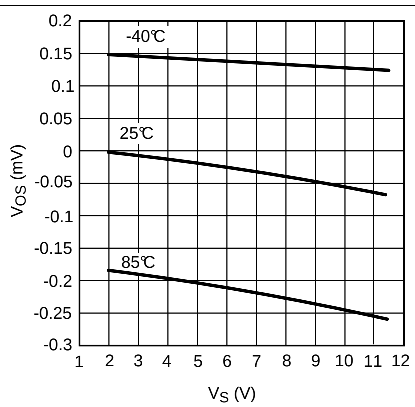
Receive CH.: A_V = +2
$R_f = R_g$ = 510

Figure 21. Crosstalk Rejection vs. Frequency (Output to Output, LMH6646)



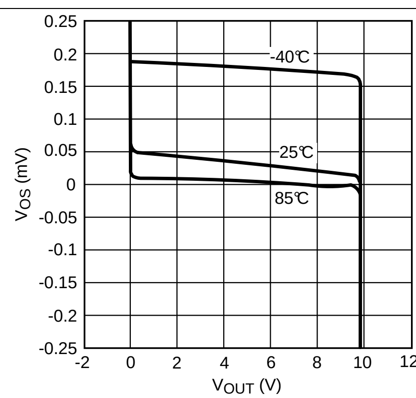
V_S = ±5 V N = 19k UNITS σ = 4.6 mV

Figure 22. V_{OS} Distribution



V_{CM} = 0.5 V

Figure 23. V_{OS} vs. V_S (a Typical Unit)

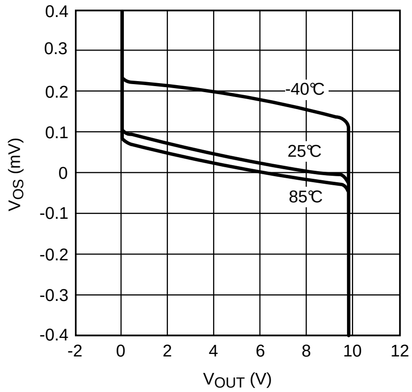


V_S = 10 V R_L = 10 kΩ to V_S/2

Figure 24. V_{OS} vs. V_{OUT} (a Typical Unit)

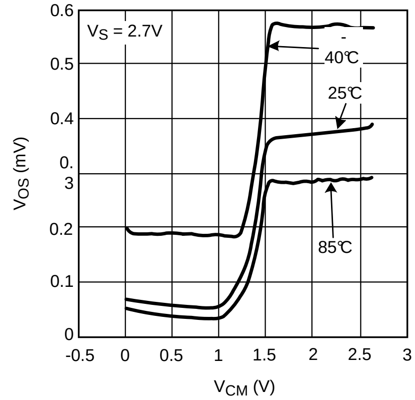
Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.



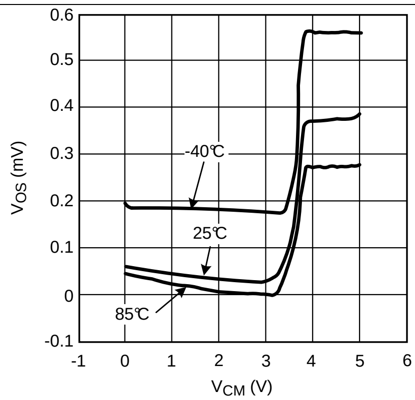
V_S = 10 V R_L = 1 kΩ to V_S/2

Figure 25. V_{OS} vs. V_{OUT} (a Typical Unit)



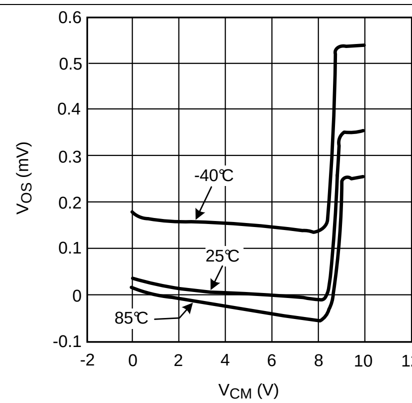
V_S = 2.7 V

Figure 26. V_{OS} vs. V_{CM} (a Typical Unit)



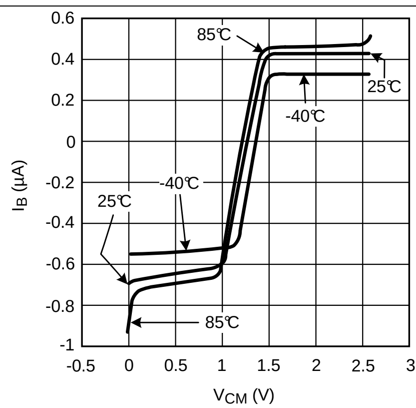
V_S = 5 V

Figure 27. V_{OS} vs. V_{CM} (a Typical Unit)



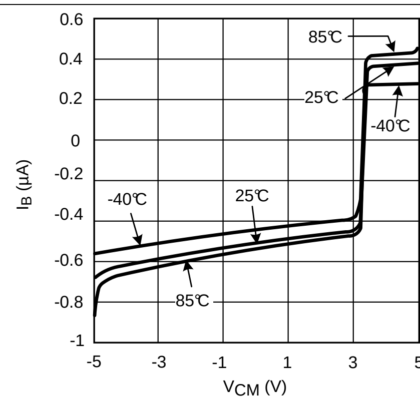
V_S = 10 V

Figure 28. V_{OS} vs. V_{CM} (a Typical Unit)



V_S = 2.7 V

Figure 29. I_B vs. V_{CM}

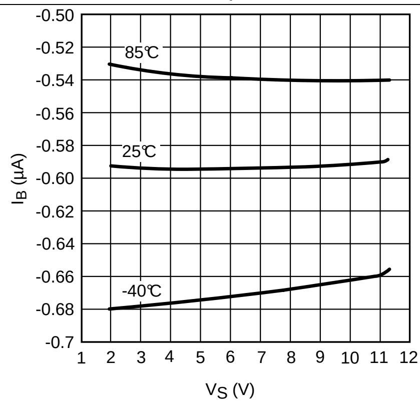


V_S = ±5 V

Figure 30. I_B vs. V_{CM}

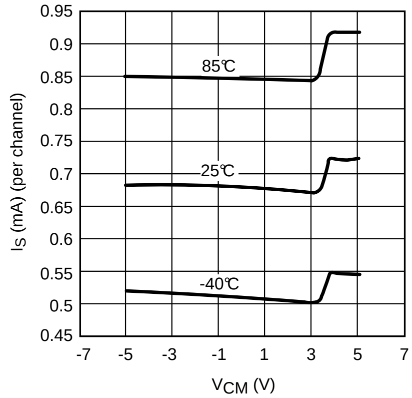
Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.



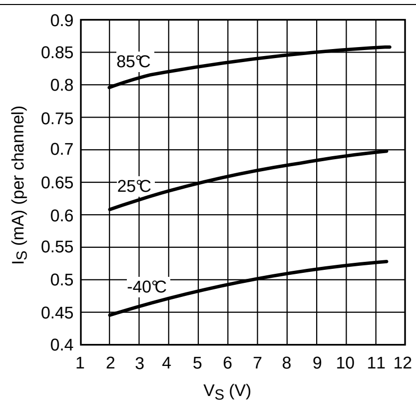
V_{CM} = 0.2 V

Figure 31. I_B vs. V_S



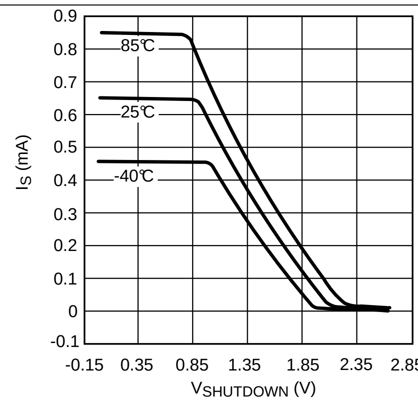
V_S = ±5 V

Figure 32. I_S vs. V_{CM}



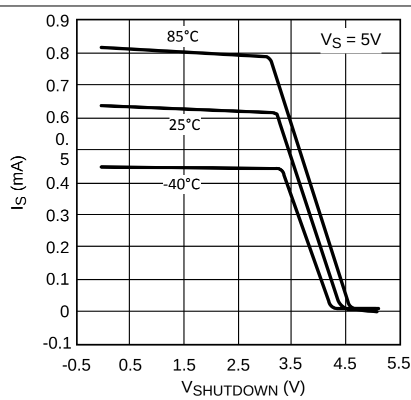
V_S = ±5 V V_{CM} = 0.2 V

Figure 33. I_S (mA) vs. V_s(V)



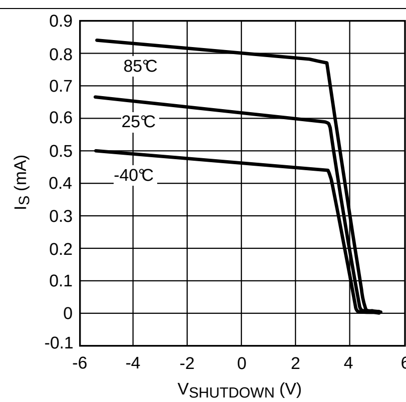
V_S = 2.7 V

Figure 34. I_S vs. $V_{SHUTDOWN}$ (LMH6647)



V_S = 5 V

Figure 35. I_S vs. $V_{SHUTDOWN}$ (LMH6647)

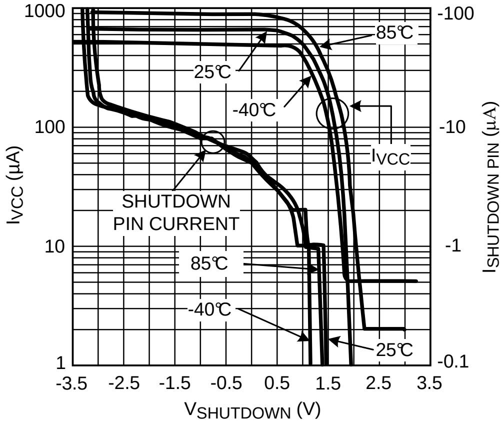


V_S = ±5 V

Figure 36. I_S vs. $V_{SHUTDOWN}$ (LMH6647)

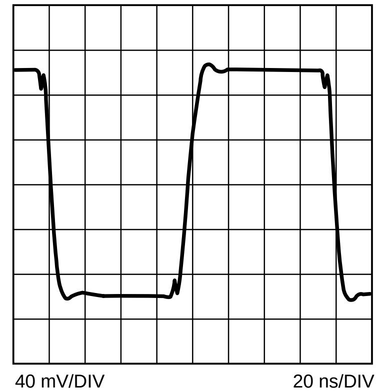
Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.



V_S = ±2.5 V

Figure 37. Shutdown Pin and Supply Current vs. Shutdown Voltage (LMH6647)

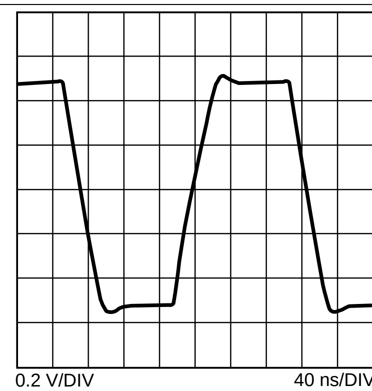


V_S = ±5 V R_L = 1kΩ A_V = +1
V_{OUT} = 0.2 Vpp

Figure 38. Small Signal Step Response

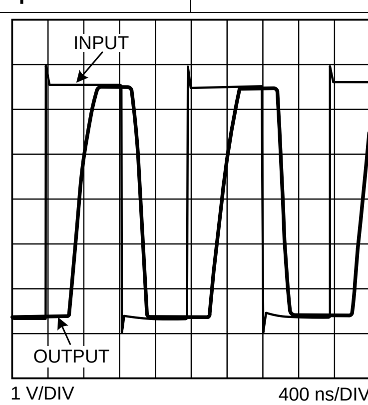
V_S = 2.7 V R_L = 1 kΩ V_{OUT} = 1 Vpp
A_V = +1

Figure 39. Large Signal Step Response



V_S = 5 V R_L = 1 kΩ V_{OUT} = 1 Vpp
A_V = -1

Figure 40. Large Signal Step Response



A_V = +2 R_L = 1 kΩ
V_S = ±2.5 V R_f= R_g = 2 kΩ

Figure 41. Output Overload Recovery

8 Detailed Description

8.1 Overview

The LMH664x family is based on proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7 V) and low Collector bias current.
- Rail-to-Rail input which allows the input common mode voltage to go beyond either rail by about 0.5 V typically.
- A class A-B “turn-around” stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-pull output stage capable of 20 mA output current (at 0.5 V from the supply rails) while consuming only ~700 µA of total supply current per channel. This architecture allows output to reach within mV of either supply rail at light loads.
- Consistent performance from any supply voltage (2.7 V to 10 V) with little variation with supply voltage for the most important specifications (BW, SR, I_{OUT}, for example)

8.2 Functional Block Diagram

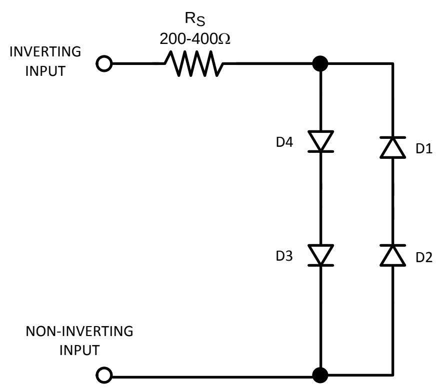


Figure 42. LMH6647 Equivalent Input in Shutdown Mode

During shutdown, the input stage has an equivalent circuit as shown below in Figure 42.

8.3 Feature Description

8.3.1 LMH6647 Micro-power Shutdown

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch (transistor) could be used to shunt the output to ground. Figure 43 shows a circuit where a NPN bipolar is used to keep the output near ground (~ 80 mV):

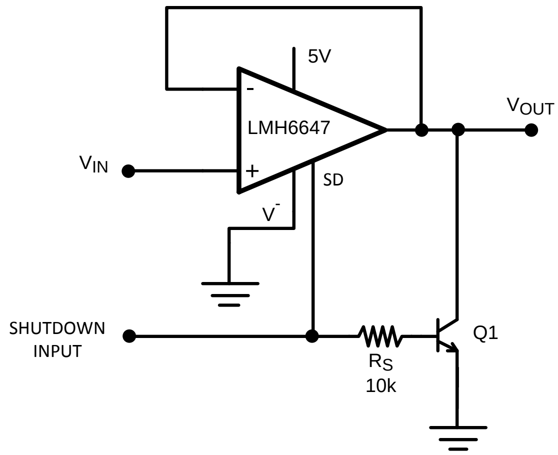


Figure 43. Active Pull-Down Schematic

Figure 44 shows the output waveform.

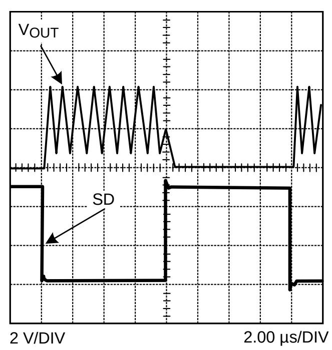


Figure 44. Output Held Low by Active Pull-Down Circuit

NOTE

For normal operation, tie the SD pin to V^-.

If bipolar transistor power dissipation is not tolerable, the switch could be by a N-channel enhancement mode MOSFET.

8.4 Device Functional Modes

The LMH6647 can be shutdown to save power and reduce its supply current to less than 50 μA ensured, by applying a voltage to the SD pin. The SD pin is "active high" and needs to be tied to V^- for normal operation. This input is low current (< 20 μA, 4 pF equivalent capacitance) and a resistor to V^- (≤ 20 kΩ) will result in normal operation. Shutdown is ensured when SD pin is 0.4V or less from V^+ at any operating supply voltage and temperature.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into Hi-Z (high impedance) mode. Complete device Turn-on and Turn-off times vary considerably relative to the output loading conditions, output voltage, and input impedance, but is generally limited to less than 1μs (see tables for actual data).

As seen in Figure 42 in shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is "forced" by another device such as in a multiplexer, the other device will need to conduct the current described in order to maintain the output potential.

The total input common mode voltage range, which extends from below V^- to beyond V^+, is covered by both an NPN and a PNP stage. The NPN stage is switched on whenever the input is less than 1.2 V from V^+ and the PNP stage covers the rest of the range. In terms of the input voltage, there is an overlapping region where both stages are processing the input signal. This region is about 0.5 V from beginning to the end. As far as the device application is concerned, this transition is a transparent operation. However, keep in mind that the input bias current value and direction will depend on which input stage is operating (see Figure 29). For low distortion applications, it is best to keep the input common mode voltage from crossing this transition point. Low gain settling applications, which generally encounter larger peak-to-peak input voltages, could be configured as inverting stages to eliminate common mode voltage fluctuations.

In terms of the output, when the output swing approaches either supply rail, the output transistor will enter a quasi-saturated state. A subtle effect of this operational region is that there is an increase in supply current in this state (up to 1 mA). The onset of Quasi-saturation region is a function of output loading (current) and varies from 100 mV at no load to about 1 V when output is delivering 20 mA, as measured from supplies. Both input common mode voltage and output voltage level affect the supply current (see Figure 32).

With 2.7V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH664x family is well suited to many low voltage/low power applications. Even with 2.7 V supplies, the -3dB BW (@ A_V = +1) is typically 55 MHz with a tested limit of 45 MHz. Production testing guarantees that process variations will not compromise speed.

This device family is designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). Figure 45, below, shows the input and output voltage when the input voltage significantly exceeds the supply voltages.

The output does not exhibit any phase reversal as some op amps do. However, if the input voltage range is exceeded by more than a diode drop beyond either rail, the internal ESD protection diodes will start to conduct. The current flow in these ESD diodes should be externally limited.

Device Functional Modes (continued)

Figure 45 demonstrates that the output is well behaved and there are no spikes or glitches due to the switching. Switching times are approximately around 500 ns based on the time when the output is considered “valid”.

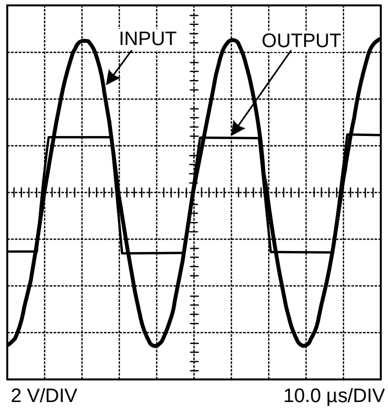


Figure 45. Input/Output Shown with Exceeded Input CMVR

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMH664x family is well suited to many low voltage/low power applications and is designed to avoid output phase reversal. Figure 45, for example, depicts the Input/Output Shown with Exceeded Input CMVR and functions as a 2:1 MUX operating on a single 2.7-V power supply by utilizing the shutdown feature of the LMH6647.

9.2 Typical Application

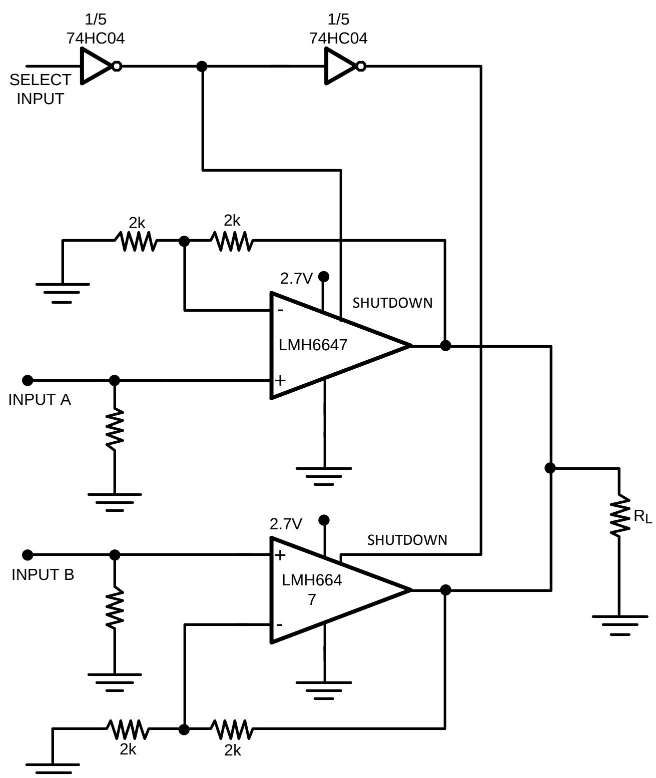


Figure 46. 2:1 MUX Operating off a 2.7V Single Supply

9.2.1 Design Requirements

This application requires fast, glitch-less transition between selected channels. The LMH6647 turn on and turn off times are 250 ns and 560 ns respectively. Transition between channels is devoid of any excessive glitches.

9.2.2 Detailed Design Procedure

In this application, the LMH6647 output pins are directly tied to each other. The shutdown pin of each LMH6647 is driven in-opposite sense of the other (that is, “Low” on 1st LMH6647 with “High” on the 2nd LMH6647, and vice versa). When shutdown is invoked, the device output enters Hi-Z state, while the alternate LMH6647 is being powered on simultaneously. This way, the shutdown function serves the dual purpose of allowing only the input associated with device which is not in shutdown to be selected and to appear at the output.

Typical Application (continued)

9.2.3 Application Curve

Figure 47 shows the MUX output when selecting between a 1 MHz sine and a 250 KHz triangular waveform.

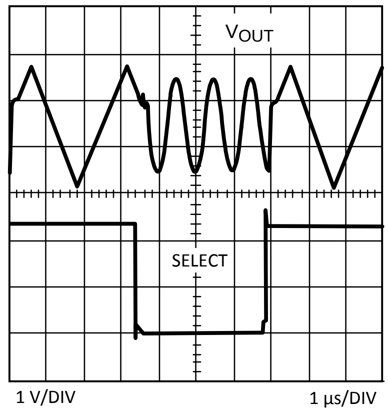


Figure 47. 2:1 MUX Output

10 Power Supply Recommendations

The LMH664x device family can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends covers the entire supply voltage range for maximum flexibility. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

11 Layout

11.1 Layout Guidelines

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. For more information, see Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* (SNOA367).

Another important parameter in working with high speed/high performance amplifiers is the component values selection. Choosing large valued external resistors will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

11.2 Layout Example

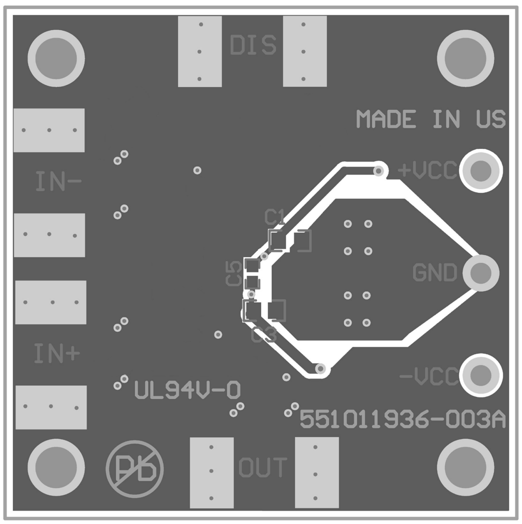


Figure 48. Layer2 Silk (SOT-23 Board Layout)

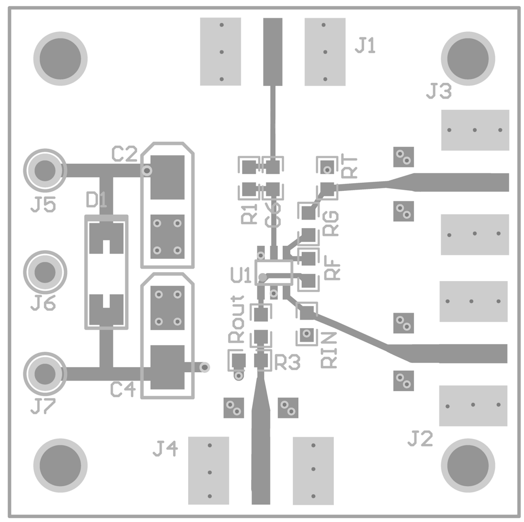


Figure 49. Layer1 Silk (SOT-23 Board Layout)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers,* Application Note OA-15 (SNOA367)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6645	Click here	Click here	Click here	Click here	Click here
LMH6646	Click here	Click here	Click here	Click here	Click here
LMH6647	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6645MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 45MA	Samples
LMH6645MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 45MA	Samples
LMH6645MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A68A	Samples
LMH6645MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A68A	Samples
LMH6646MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 46MA	Samples
LMH6646MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 46MA	Samples
LMH6646MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A70A	
LMH6646MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A70A	Samples
LMH6646MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A70A	Samples
LMH6647MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 47MA	Samples
LMH6647MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 47MA	Samples
LMH6647MF	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 85	A69A	
LMH6647MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A69A	Samples
LMH6647MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A69A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

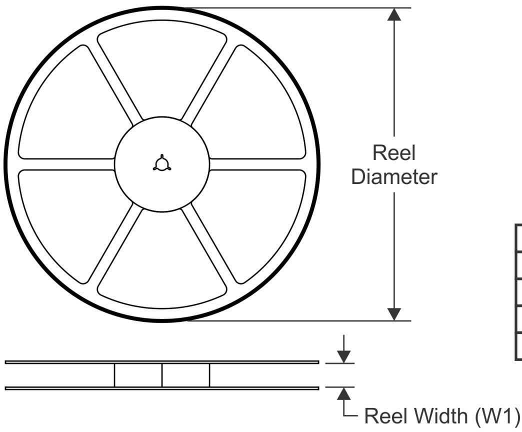
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

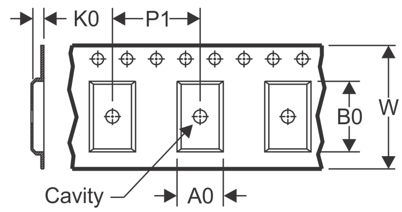
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

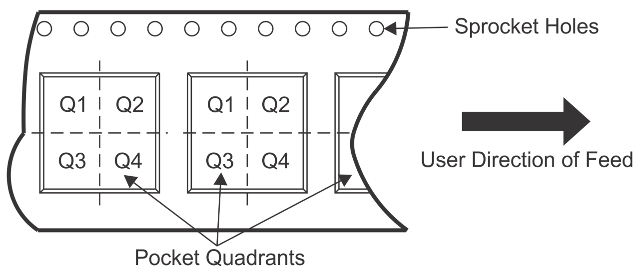
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

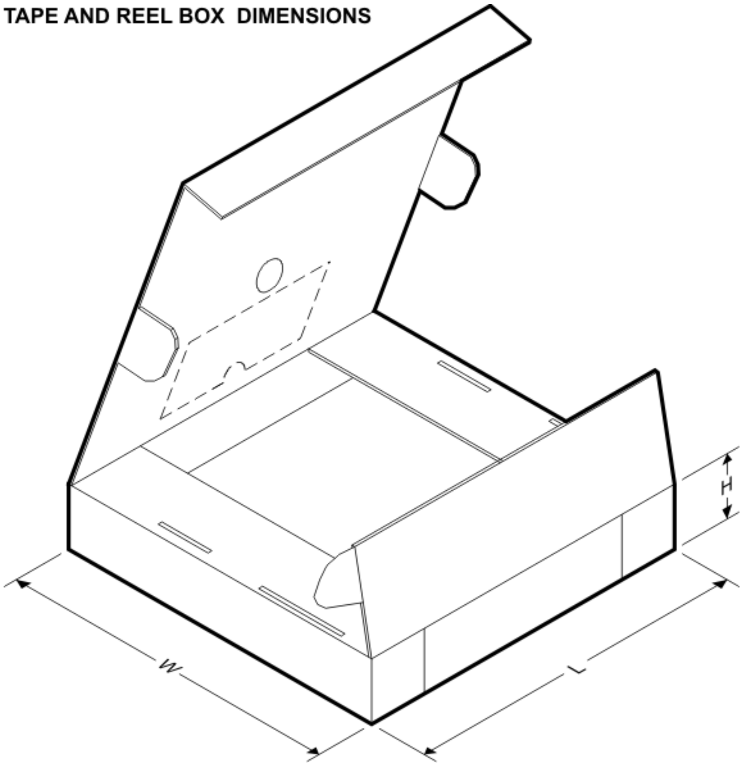
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6645MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6645MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6645MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6646MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6646MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6646MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6646MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6647MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6647MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6647MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6647MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

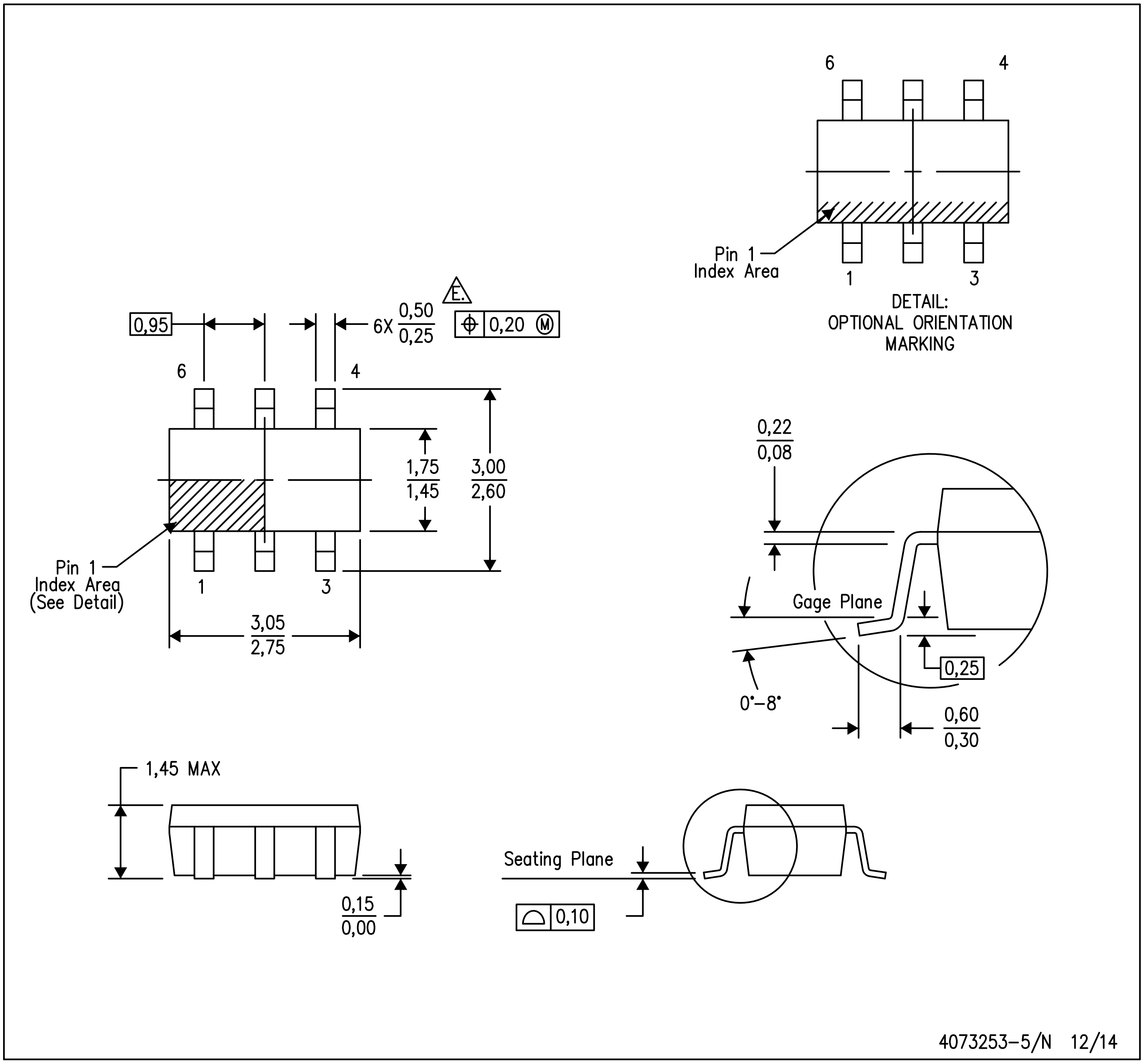
TAPE AND REEL BOX DIMENSIONS



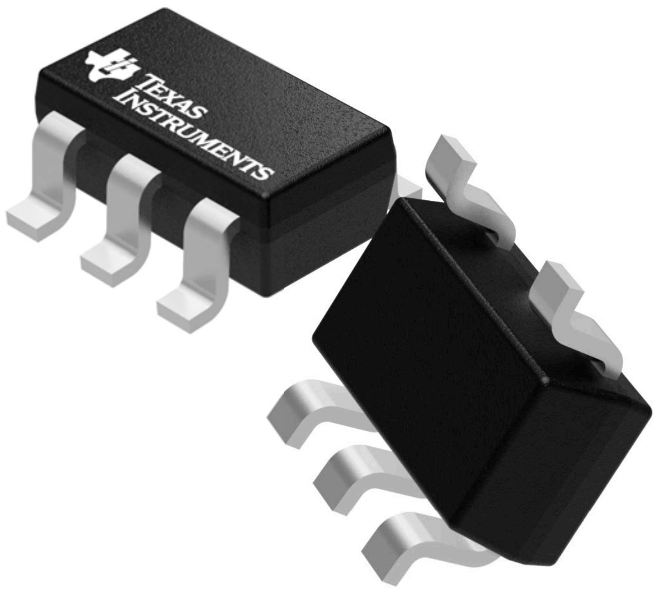
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6645MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6645MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6645MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6646MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6646MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6646MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6646MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6647MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6647MF	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6647MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6647MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

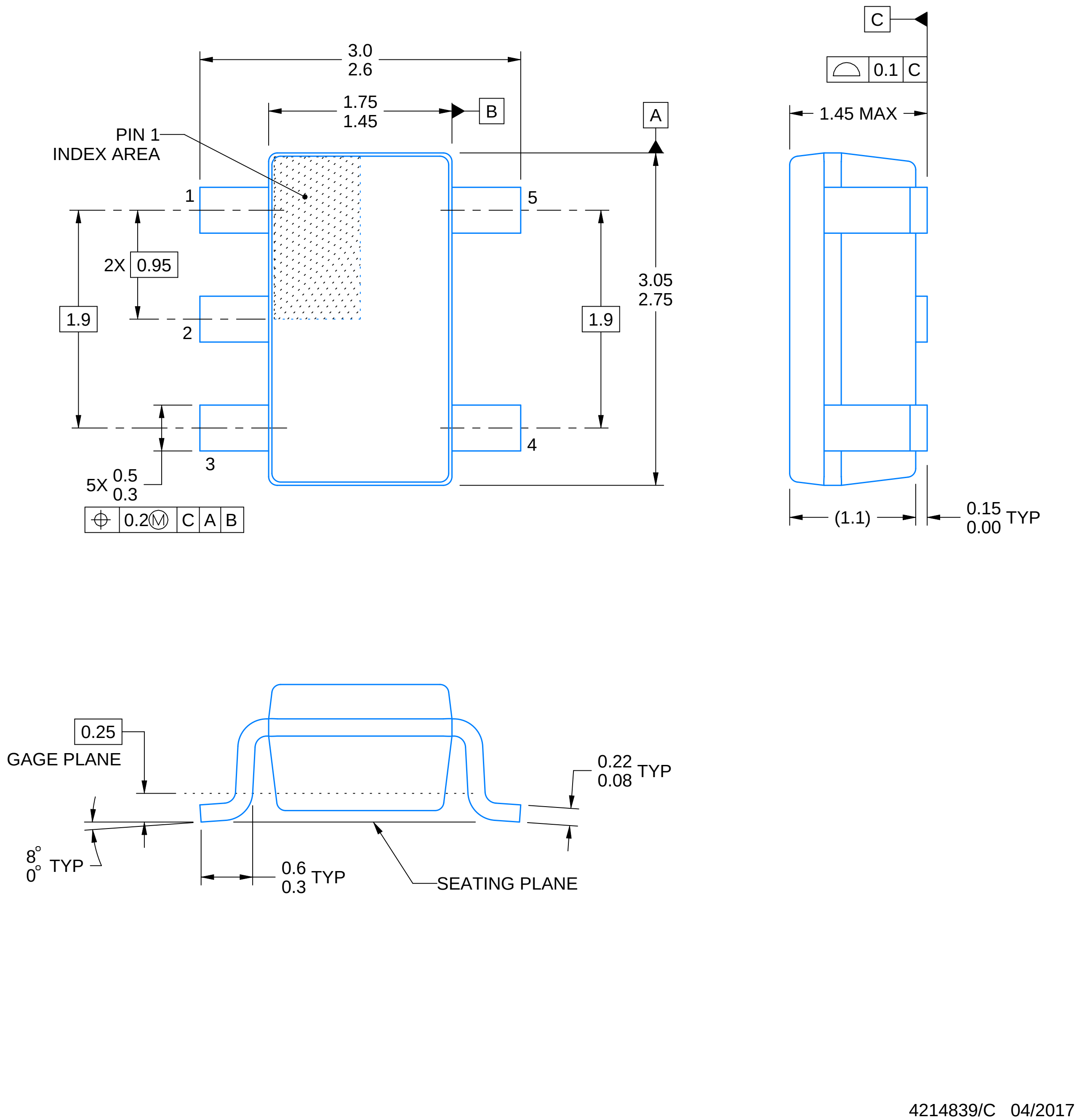
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

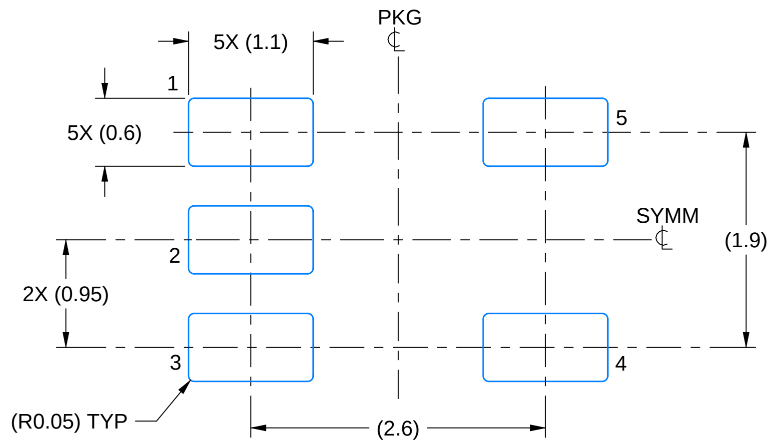


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

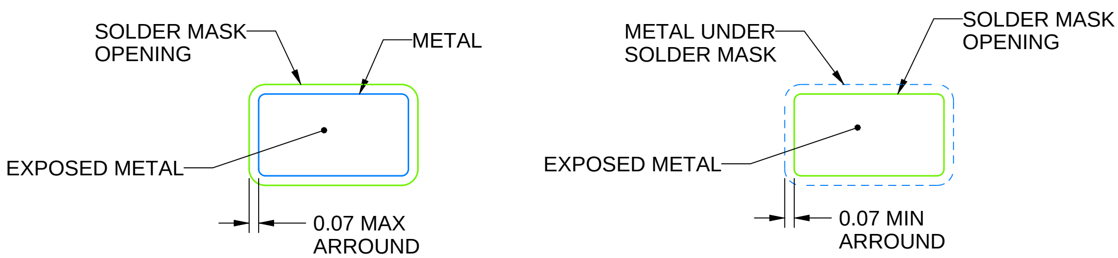


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

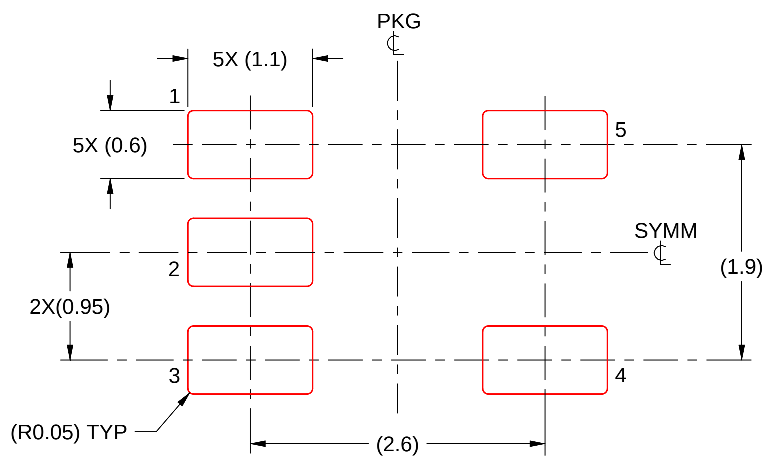


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



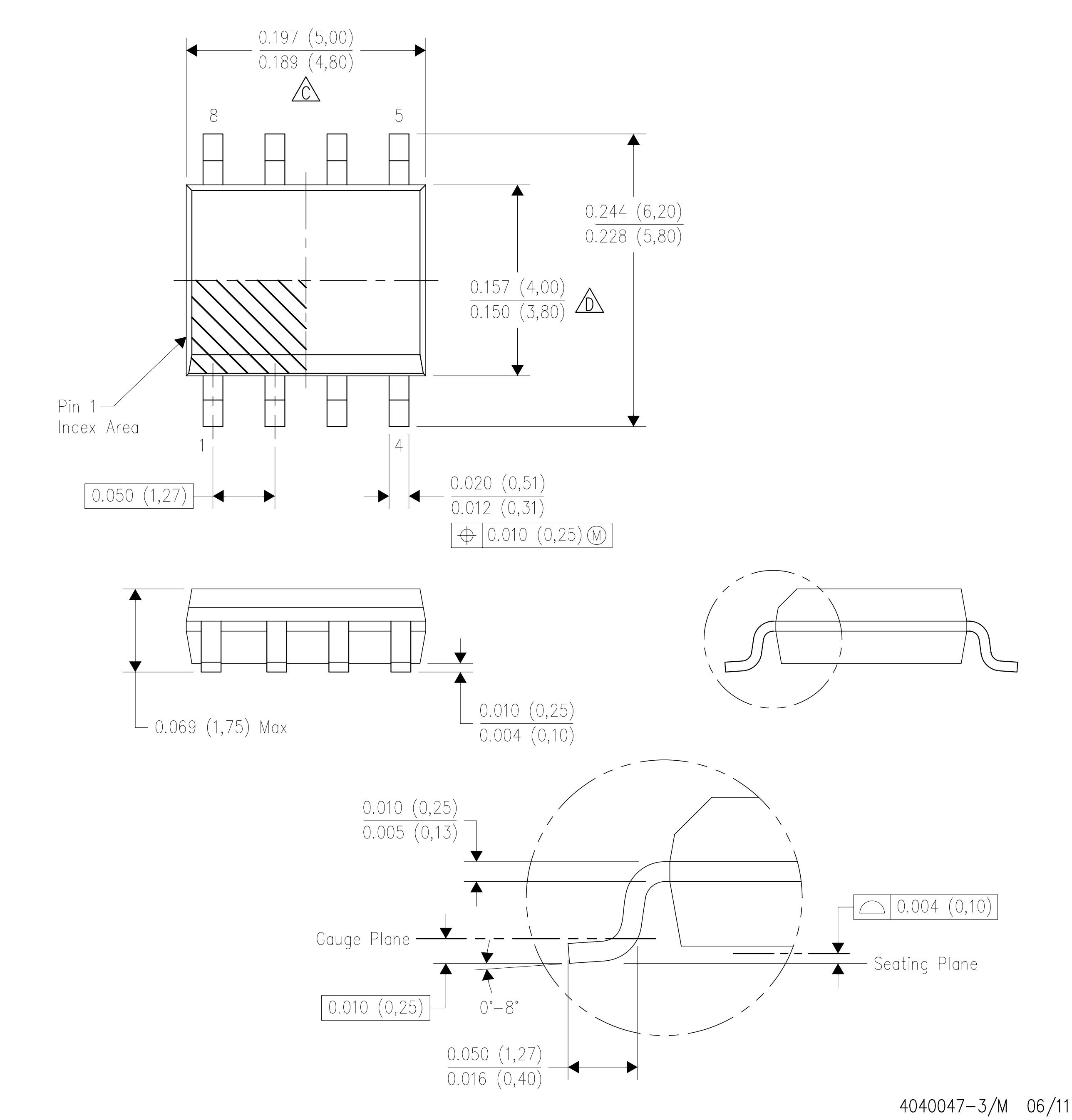
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

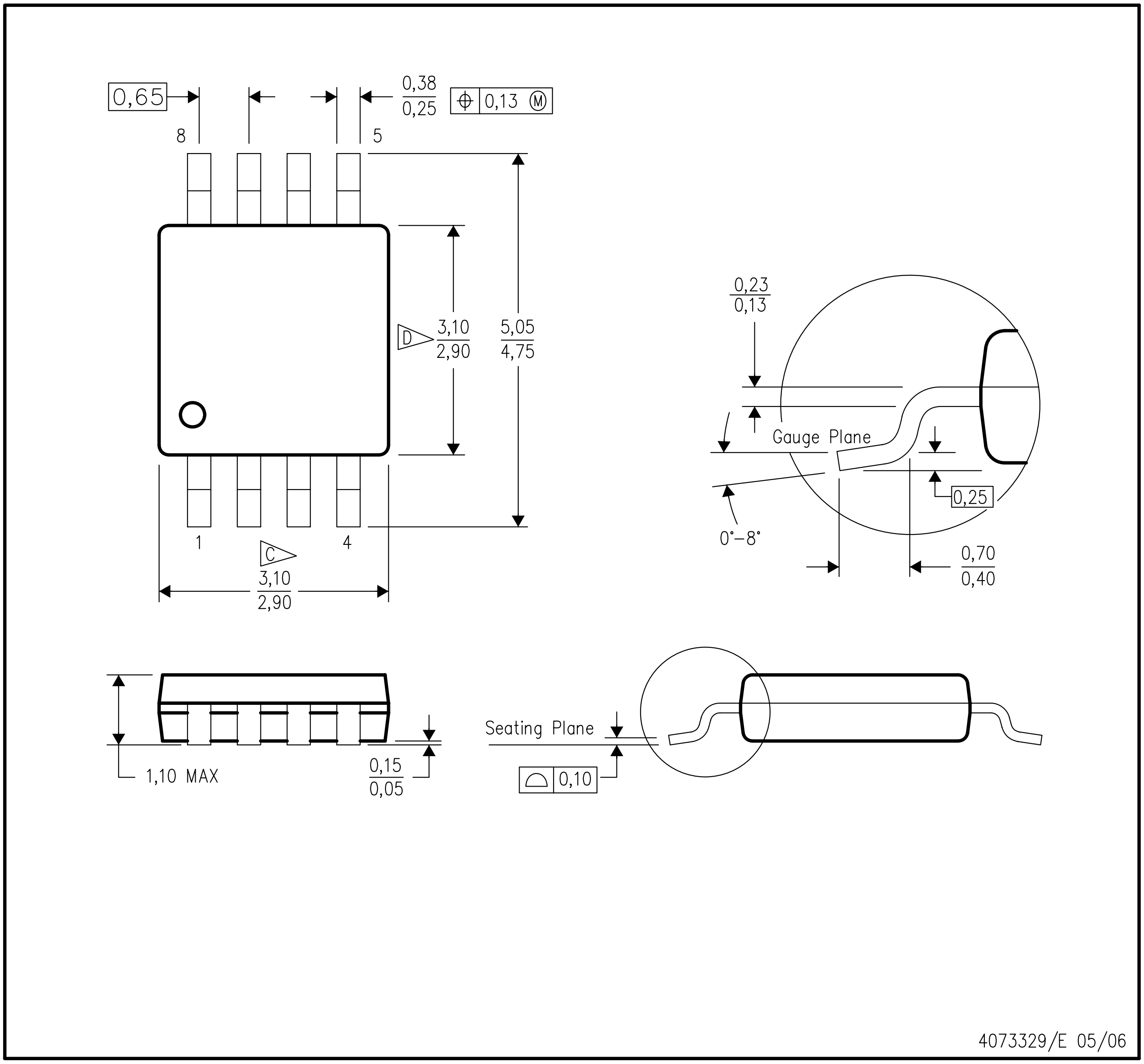
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



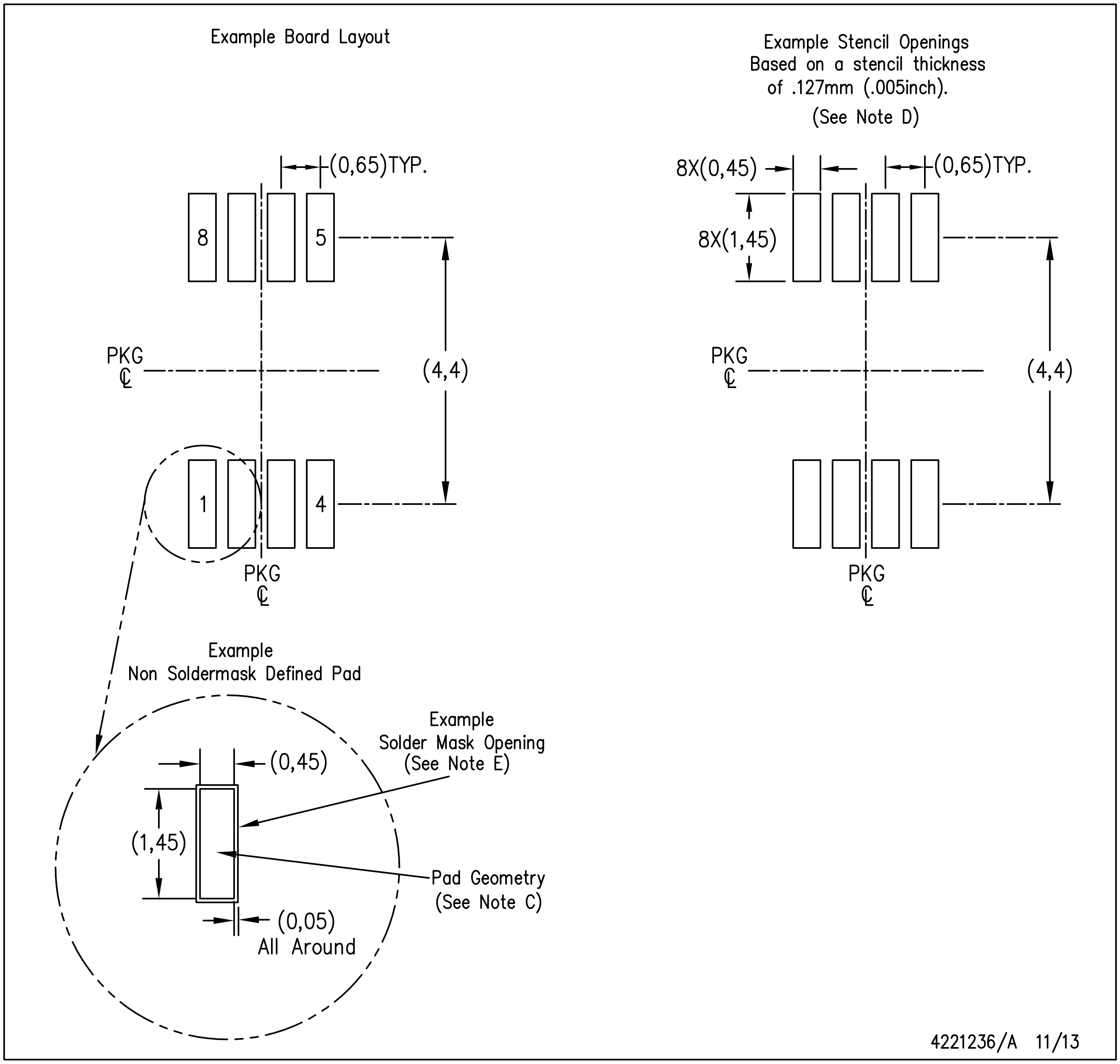
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265