LMS4684 0.5Ω Low-Voltage, Dual SPDT Analog Switch

Check for Samples: LMS4684

FEATURES

- NC Switch R_{ON} 0.5Ω max @ 2.7V
- NO Switch R_{ON} 0.8Ω max @ 2.7V
- 5 nA (typ) Supply Current T_A = 25°C
- 1.8 to 5.5V Single Supply Operation
- 12-Bump DSBGA Package
- WSON-10 Package, 3x4mm

APPLICATIONS

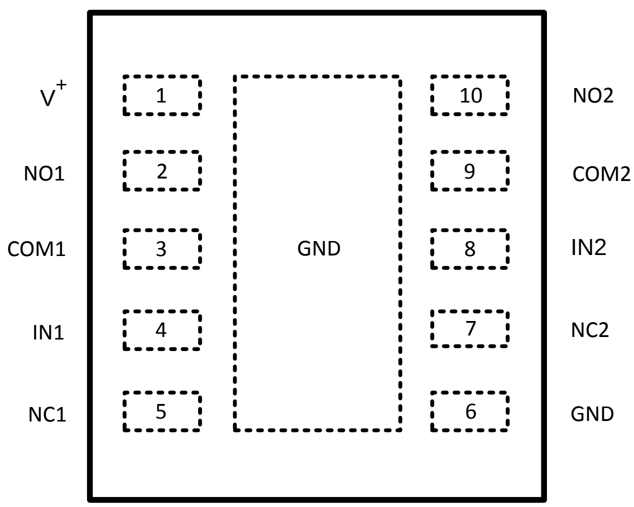
- Power Routing
- Battery-Operated Equipment
- Communications Circuits
- Modems
- Cell Phones

DESCRIPTION

The LMS4684 is a low on-resistance, low voltage dual SPDT (Single-Pole/Double-Throw) analog switch that operates from a 1.8V to 5.5V supply. The LMS4684 features a 0.5Ω R_{ON} for its NC switch and 0.8Ω R_{ON} for its NO switch at a 2.7V supply. The digital logic inputs are 1.8V logic-compatible with a 2.7V to 3.3V supply and features break-before-make switching action.

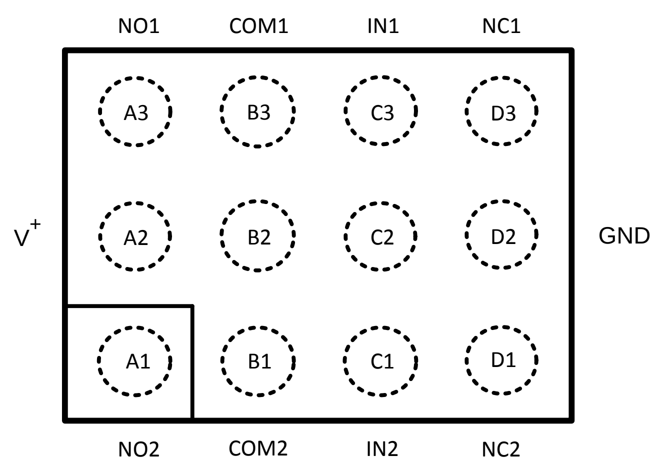
The LMS4684 is available in the 12-bump DSBGA and the 10-lead WSON miniature packages. These PCB real estate saving packages offer extreme performance while saving money with small footprints.

Connection Diagram



Exposed pad on back of package needs to be connected to pin 6 on the board

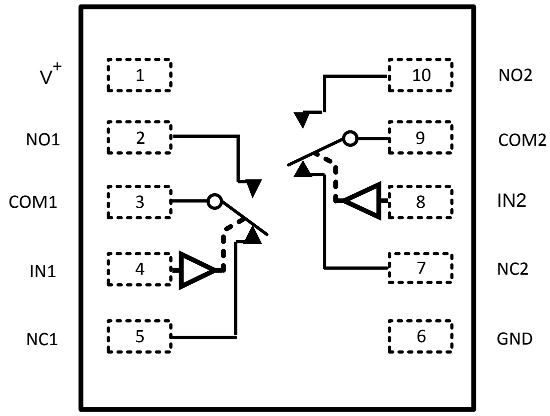
Figure 1. 10-WSON Package-Top View



Center Bumps B2 and C2 are Not Electrically Connected

Figure 2. 12-Bump DSBGA Package-Top View (Bumped Side Down)

SCHEMATIC DIAGRAM



IN	NO	NC
0	Off	On
1	On	Off
Switches shown for Logic "0" input		

PIN DESCRIPTIONS

Name	Pin ID		Description
	WSON	DSBGA	
NC	5, 7	D3, D1	Analog switch normally closed terminal
IN	4, 8	C3, C1	Digital control input
COM	3, 9	B3, B1	Analog switch common terminal
NO	2, 10	A3, A1	Analog switch normally open terminal
V^+	1	A2	Positive supply voltage
GND	6	D2	Ground
		B2, C2	Not electrically connected. Can be used to help dissipate heat by connecting to GND pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V^+		−0.3V to 6.0V
IN		−0.3V to 6.0V
COM, NO, NC		−0.3V to (V^+ + 0.3V)
Continuous Switch Current		±400 mA
ESD Tolerance (4)	Human Body Model	2000V
	Machine Model	200V
Storage Temperature Range		−65°C to 150°C
Junction Temperature (5)		150°C Max

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed.
(2) All voltages are with respect to GND, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human body model: 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF.
(5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A.

OPERATING RATINGS

Nominal Supply Voltage	1.8V to 5.5V
IN Voltage (regardless of supply)	−0.3V to 5.5V
Temperature Range	−40°C to 85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed.
(2) All voltages are with respect to GND, unless otherwise specified.

PACKAGE THERMAL RESISTANCE

Package	θ_{J-A}
WSON-10	43°C / W
DSBGA-12	57°C / W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V^+ = 2.7 to 3.3V, V_{IH} = 1.4V, V_{IL} = 0.5V. Typical values are measured at 3V, and T_J = 25°C. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{NO}, V_{NC}, V_{COM}	Analog Signal Range		0		V^+	V
$R_{ON\ (NC)}$	NC On-Resistance (1)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} =0 to V^+		0.3	**0.5**	Ω
$R_{ON\ (NO)}$	NO On-Resistance (1)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NO} =0 to V^+		0.45	**0.8**	Ω
ΔR_{ON}	On-Resistance Match Between Channels (1), (2)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} or V_{NO} =1.5V		1.11	**60**	mΩ
$R_{FLAT(NC)}$	NC-On-Resistance Flatness (3)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} = 0 to V^+; WSON T_J = -40°C to 85°C		0.1	0.25	Ω
		DSBGA T_J = -40°C to 85°C		0.1	0.25	
$R_{FLAT(NO)}$	NO On-Resistance Flatness (3)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NO} = 0 to V^+		0.18	**0.35**	Ω
$I_{NO(OFF)}$ or $I_{NC(OFF)}$	NO or NC Off Leakage Current	V^+ = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V; V_{COM} = 0.3V, 3V	−1	0.014	1	nA
			−10		**10**	
I_{COM} (ON)	COM On Leakage Current	V^+ = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V, or floating; V_{COM} = 3V, or floating	−2		2	nA
			−20		**20**	
Dynamic Characteristics						
t_{ON}	Turn-On Time	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;		38	60	ns
					70	
t_{OFF}	Turn-Off Time	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;		22	40	ns
					50	
t_{BBM}	Break-Before-Make Delay	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;	**2**	15		ns
Q	Charge Injection	COM = 0; R_S = 0; C_L= 1 nF;		200		pC
V_{ISO}	Off-Isolation (4)	R_L = 50Ω; C_L= 5 pF; f = 100 kHz		-68		dB
V_{CT}	Crosstalk			-72		dB
Digital I/O						
V_{IH}	Input Logic High		**1.4**			V
V_{IL}	Input Logic Low				**0.5**	V

(1) Guaranteed by design.
(2) ΔR_{ON} is equal to the difference between NC1/NC2 R_{ON} or NO1/NO2 R_{ON} at a specified voltage.
(3) Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
(4) Off-isolation = 20 $\log_{10}(V_{COM}/ V_{NO})$, where V_{COM} = output, V_{NO} = input switch off.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, V^+ = 2.7 to 3.3V, V_{IH} = 1.4V, V_{IL} = 0.5V. Typical values are measured at 3V, and T_J = 25°C. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	IN Input Leakage Current	V_{IN} = 0 or V^+	**−1**		**1**	µA
Power Supply						
V^+	Power-Supply Range		**1.8**		**5.5**	V
I+	Supply Current	V+ = 5.5V		5		nA

PARAMETRIC MEASUREMENT INFORMATION

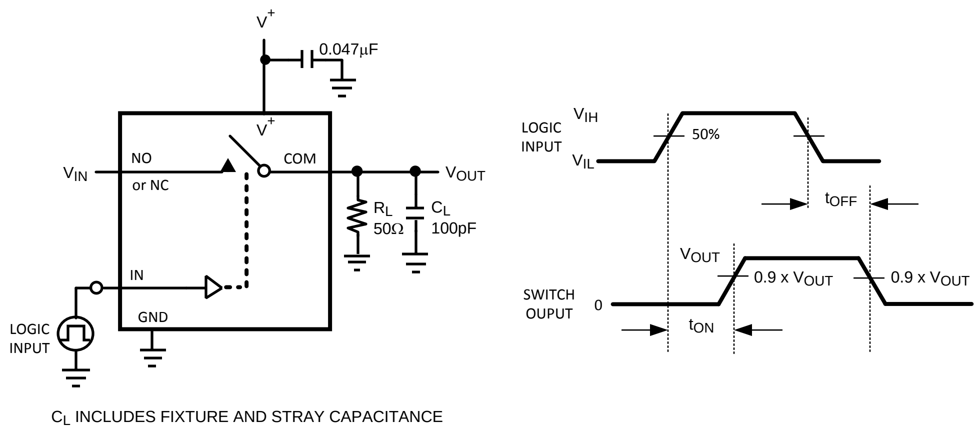


Figure 3. t_{ON} / t_{OFF} Time

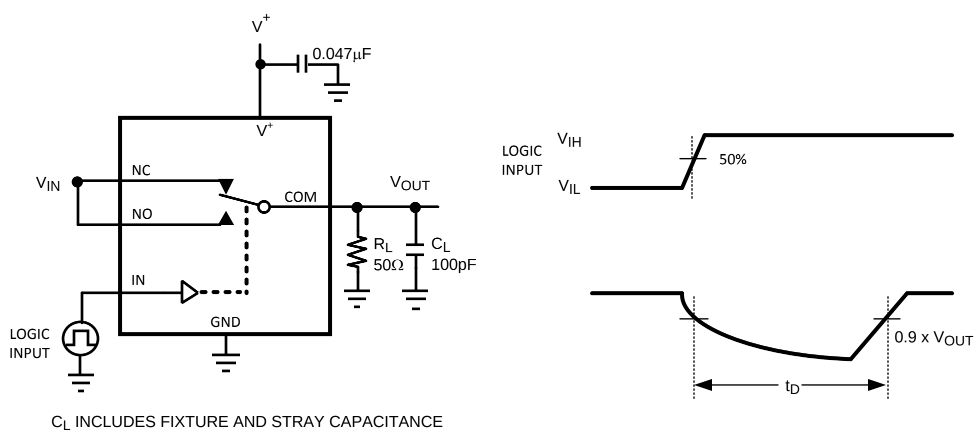


Figure 4. Break-Before Make Delay

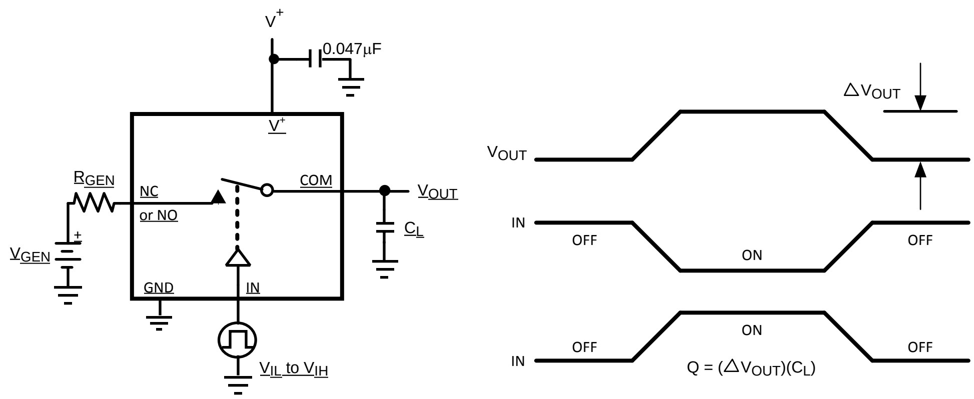


Figure 5. Charge Injection

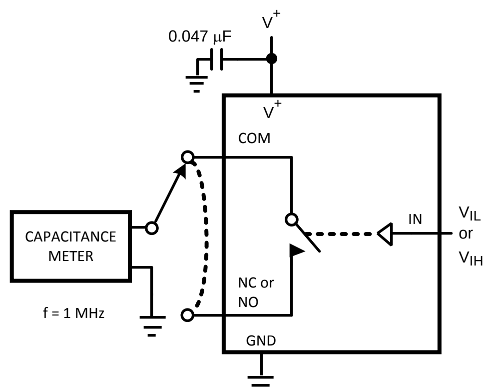


Figure 6. Channel Capacitance

TYPICAL PERFORMANCE CHARACTERISTICS

NO ON Resistance vs. COM Voltage

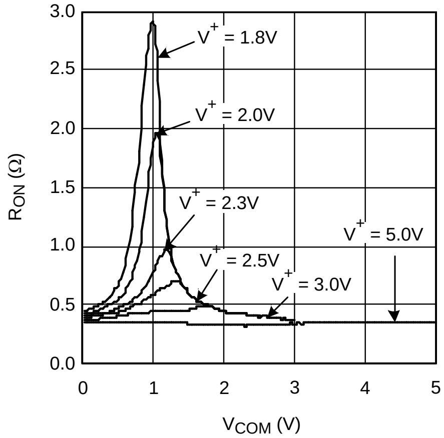


Figure 7.

NC ON Resistance vs. COM Voltage

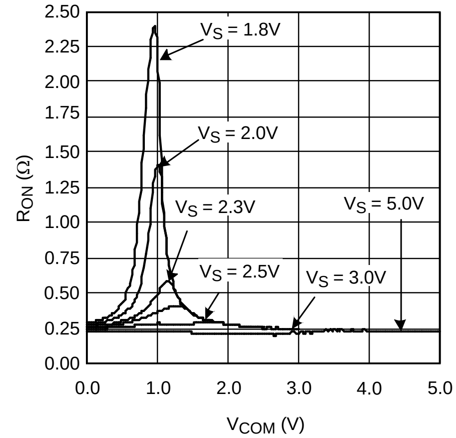


Figure 8.

Logic Threshold Voltage vs. Supply Voltage

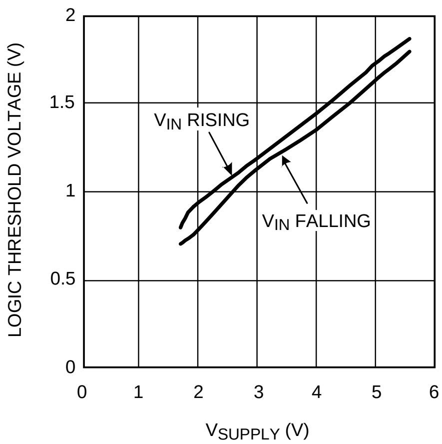


Figure 9.

Turn-on / Turn-off Times vs. Temperature

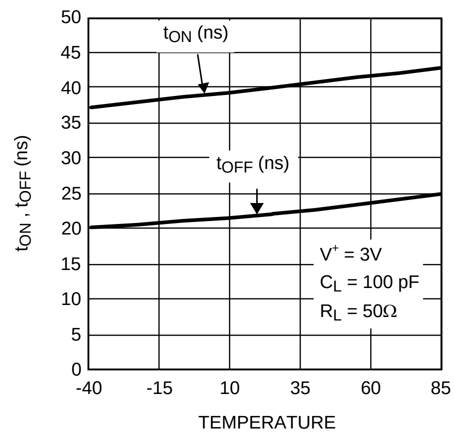


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Charge Injection vs. COM Voltage

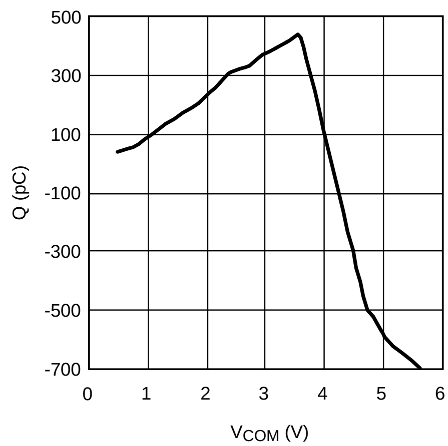


Figure 11.

NC On-Resistance vs. COM Voltage

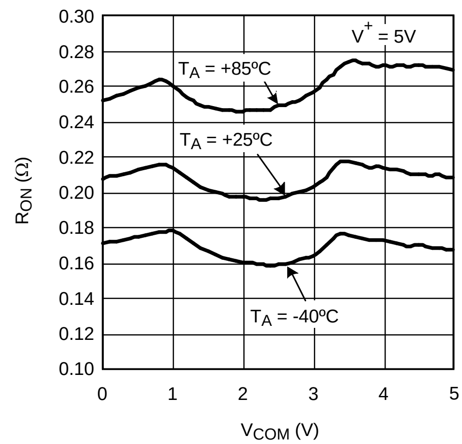


Figure 12.

NC On-Resistance vs. COM Voltage

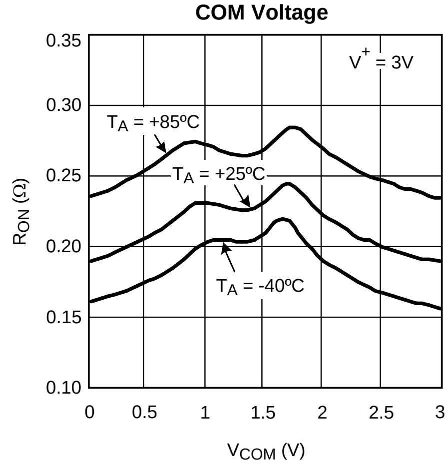


Figure 13.

NO On-Resistance vs. COM Voltage

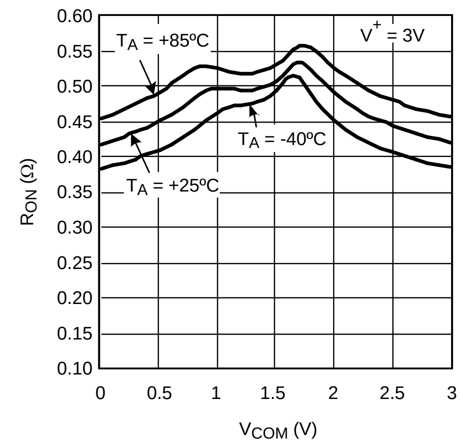


Figure 14.

NO On-Resistance vs. COM Voltage

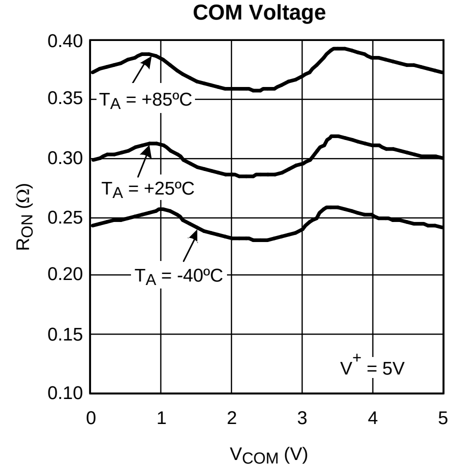


Figure 15.

FUNCTIONAL DESCRIPTION

The LMS4684 is a low voltage dual, extremely low On-Resistance analog switch that can operate over a supply voltage range of 1.8V to 5.5V. The LMS4684 has been fully characterized to operate in applications with 3V nominal supply voltage and features very low on resistance and fast Turn-Off and Turn-On times with break-before-make switching.

The switch operates asymmetrically; one terminal is normally closed (NC) and the other terminal normally open (NO).

Both NC and NO terminals are connected to a common terminal (COM). This configuration is ideal for applications with asymmetric loads such as speaker handsets and internal speakers.

Applications Information

ANALOG INPUT SIGNAL

Analog input signals can range from GND to V^+ and are passed through the switch with very little change. Each switch is bidirectional so any pin can be an input or output.

Exercise care when making connection to an inductive load, such as a motor. As is true with any analog switch used with an inductive load, the back emf produced when the switch is turned off can damage the LMS4684 by electrical overstress. For such applications, a diode should be connected across the motor to prevent damage to the switch, as indicated in Figure 16. Be sure the diode has adequate current carrying capabilities.

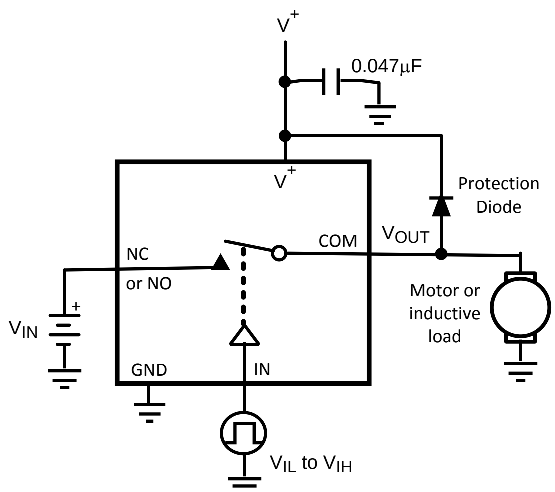


Figure 16. Inductive Load Over-Voltage Protection

DIGITAL CONTROL INPUTS

The IN pin can be driven to 5.5V regardless of the voltage level of the supply pin V^+. For example, if the LMS4684 is operated with a supply of 2V, the digital control input could still be driven to 5V. Power consumption is increased when the control pin is driven rail-to-rail.

SUPPLY VOLTAGE

It is good general practice to first apply the supply voltage to a CMOS device before sriving any other pins. This is also true for the LMS4684 analog switch, which is a CMOS device.

However, if it is necessary to have an analog signal applied before the supply voltage is applied and the analog signal source is not limited to 20 mA max, a diode connected between the supply voltage and the V^+ pin as shown in Figure 17 will provide input protection. This will limit the max analog voltage to a diode drop below V^+. This diode, D1, will also provide protection against some over voltage situations.

It is also good practice to provide adequate supply bypassing to all analog circuits. We recommend a that minimum bypass capacitor value of 0.047µF be provided for the LMS4684. An inadequate bypass capacitor can lead to excessive supply current.

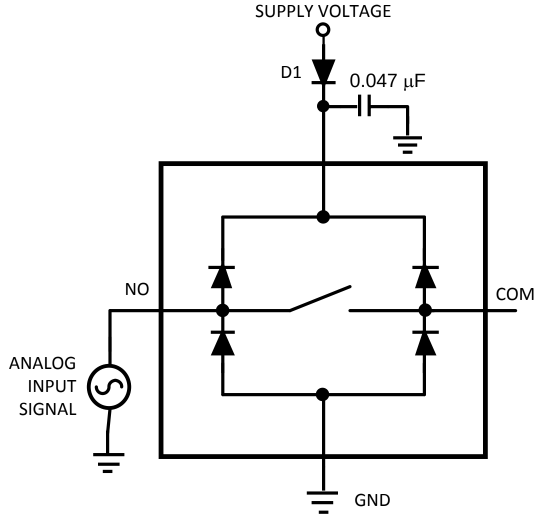


Figure 17. Input Over Voltage Protection Circuitry

OFF-ISOLATION

Analog switches are composed of FETs (field Effect Transistors). The channel resistance is low when the pass transistors are "on" and that resistance is high when the pass transistors are "off". However, when the pass transistors are "off", the source to drain capacitance of the pass transistors will pass some energy. This capacitance is inversely proportional to the switch "on" resistance, so a switch with a low "on" resistance may not be suitable for some high frequency applications.

Figure 18 shows the equivalent circuit of an analog switch. Unless the load impedance after the switch is relatively low, the switch capacitance will couple excessive energy across the "open" switch at higher frequencies, degrading off isolation performance. Off Isolation of the LMS4684 is specified with a 50Ω load. Higher load impedances will degrade off isolation performance compared with what is specified.

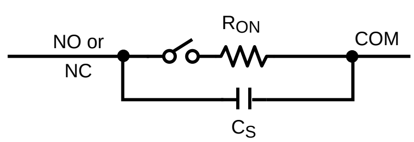


Figure 18. Equivalent Circuit of an Analog Switch

Off isolation may be improved by decreasing the LMS4684 load impedance below 50Ω. When doing this, be sure that the LMS4684 maximum current rating is not exceeded. Also, decreasing the load impedance too much can result in excessive signal distortion because the channel resistance variation with input signal voltage would then be a greater percentage of the load impedance.

If it is desired to extend the usable bandwidth of the LMS4684 while maintaining reasonable off-isolation is through the use of the circuit of Figure 19.

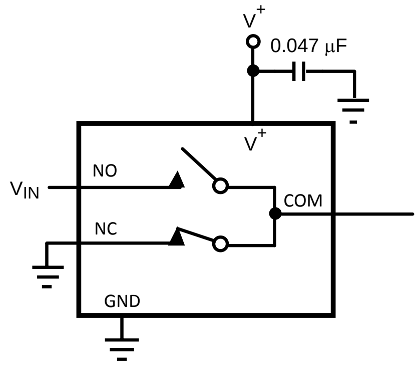


Figure 19. Using the LMS4684 at higher frequencies

PCB LAYOUT AND THERMAL CONSIDERATIONS

Both the WSON and DSBGA packages offer enhanced board real estate savings because of their small footprints. These tiny packages are capable of handling high continuous currents because of the advanced package thermal handling capabilities.

The WSON package has the exposed die attach pad internally connected to the internal circuit GND. When this pad is soldered to copper on the PCB board according to Application Note AN-1187, the full thermal capability of the WSON package can be achieved without additional bulky heat sinks to dissipate the heat generated. The DSBGA package has a similar capability to dissipate heat through Bumps B2 and C2, which are not electrically connected. To enhance heat dissipation of the DSBGA package B2 and C2 could be connected to the GND pin through copper traces on the board.

See Application Note AN-1112 for DSBGA package considerations.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMS4684ITL/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F09A	Samples
LMS4684ITLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F09A	Samples
LMS4684LD/NOPB	ACTIVE	WSON	NGZ	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L4684	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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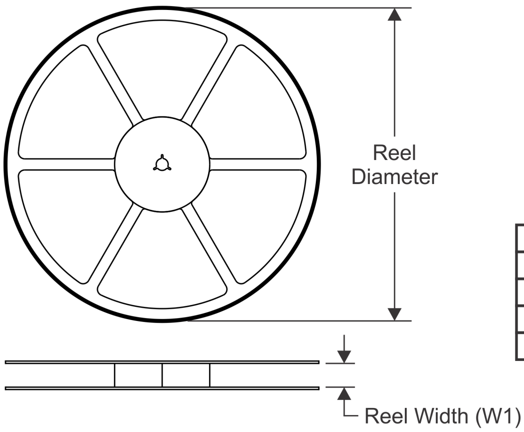
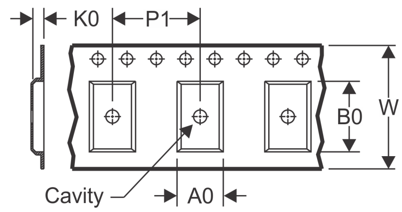
TAPE AND REEL INFORMATION

REEL DIMENSIONS

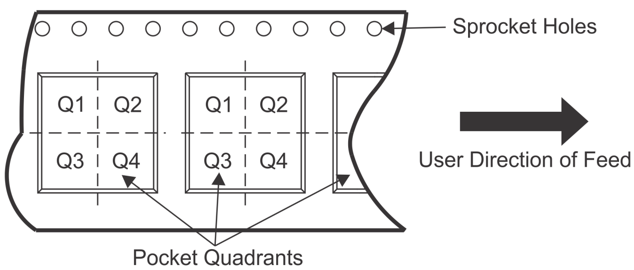


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

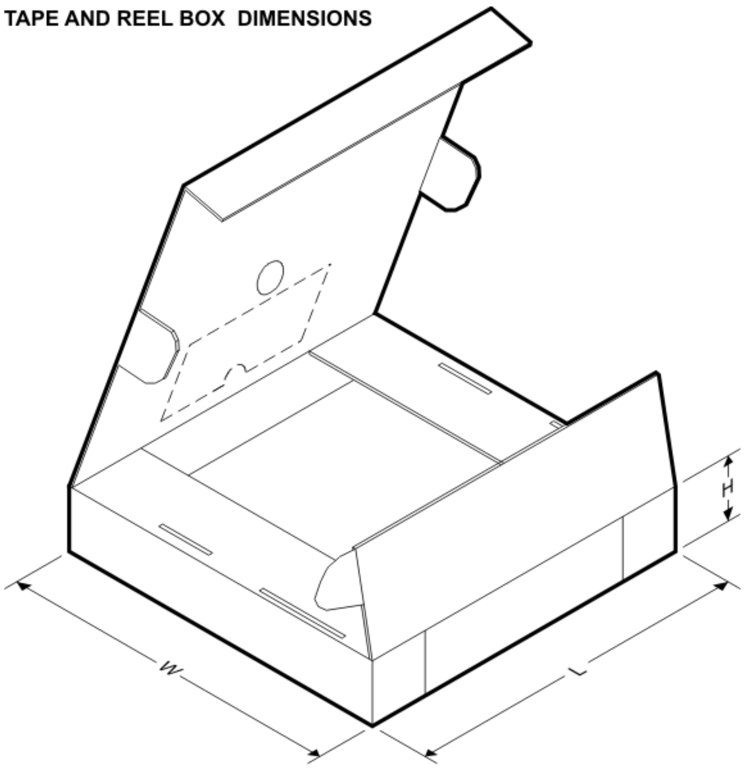
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

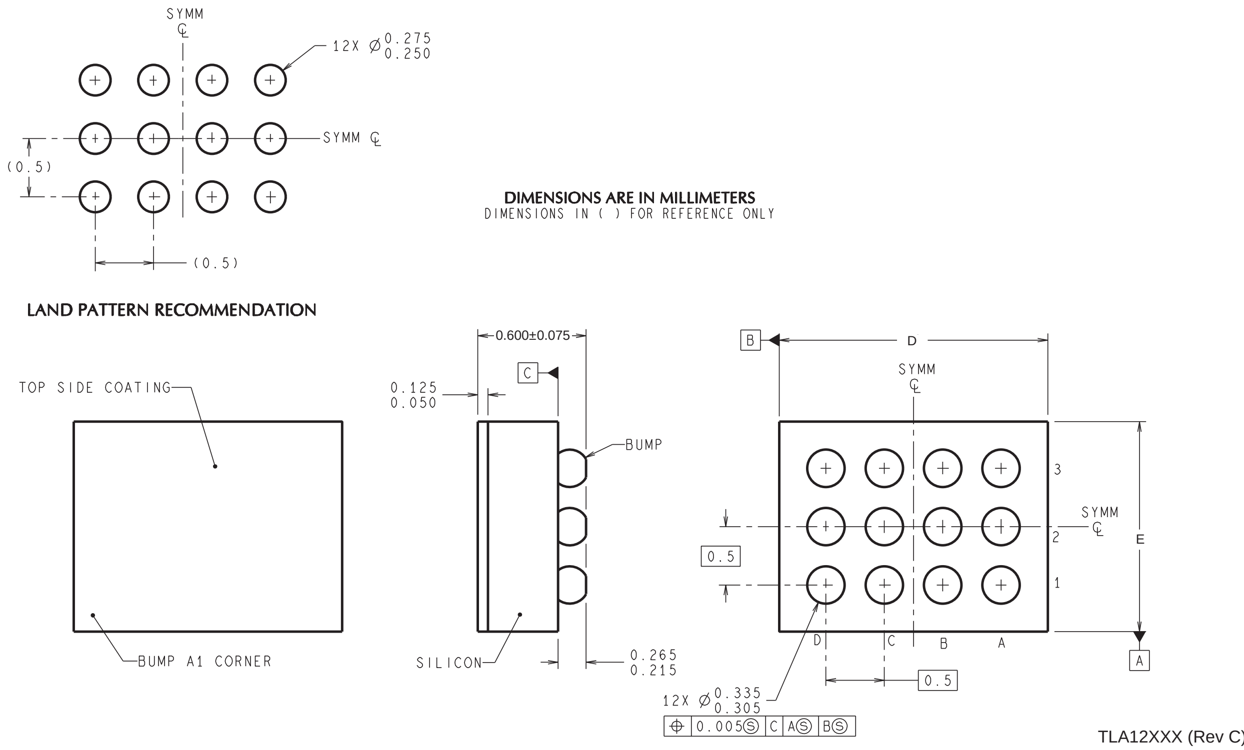
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMS4684ITL/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.73	2.46	0.76	4.0	8.0	Q1
LMS4684ITLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.73	2.46	0.76	4.0	8.0	Q1
LMS4684LD/NOPB	WSON	NGZ	10	1000	178.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMS4684ITL/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LMS4684ITLX/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0
LMS4684LD/NOPB	WSON	NGZ	10	1000	210.0	185.0	35.0



TLA12XXX (Rev C)

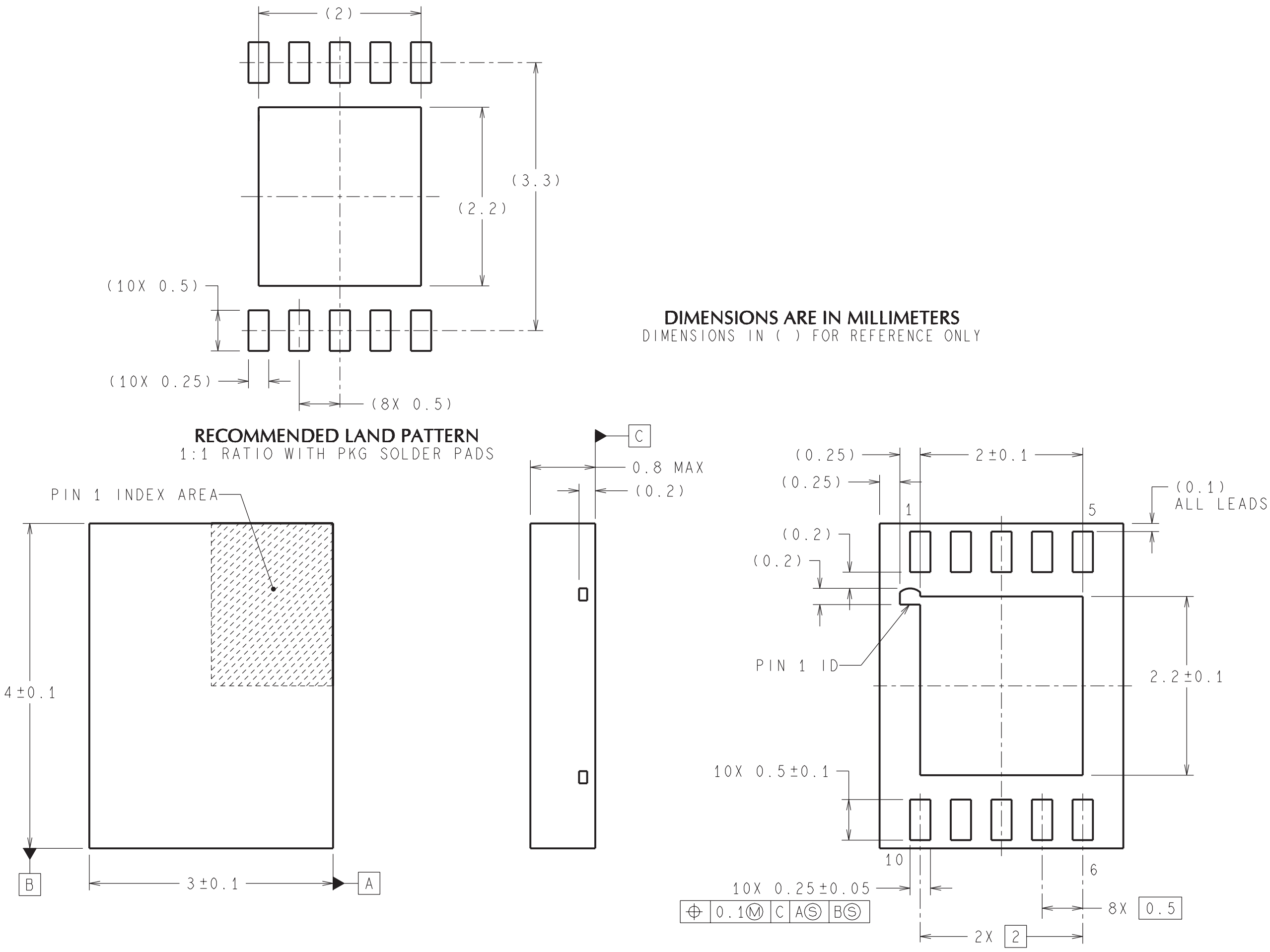
D: Max = 2.378 mm, Min =2.317 mm

E: Max = 1.641 mm, Min =1.581 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

NGZ0010B



LDA10B (Rev B)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265