Ultra Low Noise, 200 mA Linear Regulator for RF/Analog Circuits - Requires No Bypass Capacitor

Check for Samples: LP5904

FEATURES

- **Stable with 1.0 µF Ceramic Input and Output Capacitors**
- **No Noise Bypass Capacitor Required**
- **Remote Output Capacitor Placement**
- **Thermal-overload and Short-circuit Protection**
- **–40°C to +125°C Junction Temperature Range for Operation**

APPLICATIONS

- **Cellular Phones**
- **PDA Handsets**
- **Wireless LAN Devices**

KEY SPECIFICATIONS

- **Input Voltage Range … 2.2V to 5.5V**
- **Output Voltage Range … 1.2V to 4.4V**
- **Output Current … 200 mA**
- **Low Output Voltage Noise at 200 mA … 6.5µVRMS**
- **PSRR … 78 dB at 1kHz**
- **Output Voltage Tolerance … ± 2%**
- **Virtually Zero IQ (Disabled) … <1 µA**
- **Very Low IQ (Enabled) … 11 µA**
- **Startup Time … 85 µs**
- **Low Dropout … 95 mV typ**

PACKAGE

- **4-Bump DSBGA (lead free)**
  0.815 mm × 0.815 mm × 0.600 mm

DESCRIPTION

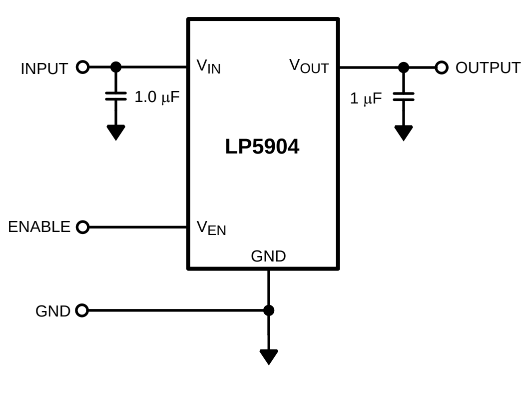
The LP5904 is a linear regulator capable of supplying 200 mA output current. Designed to meet the requirements of RF/ Analog circuits, the LP5904 device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5904 offers class-leading device noise performance without a noise bypass capacitor and the ability for remote output capacitor placement. An active pulldown circuit with a 280Ω resistor is wired from the output to ground pins to quickly discharge output when the device is disabled (VEN = low).

The device is designed to work with a 1.0 µF input and a 1.0 µF output ceramic capacitor. (No Bypass Capacitor is required.)

The device is available in a DSBGA package. For other package options contact your local TI sales office.

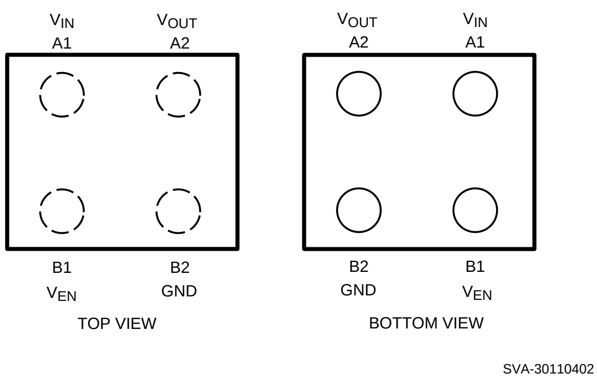
This device is available between 1.2V and 4.4V in 25 mV steps. Please contact Texas Instruments Sales for specific voltage option needs.

TYPICAL APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAMS



Note: The actual physical placement of the package marking will vary from part to part. The package marking “A” designates the date code, and will vary in production.

Figure 1. 4-Bump Thin DSBGA Package
Package Number YFQ0004AAA

PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
A1	VIN	Input voltage supply. A 1.0 µF capacitor should be connected at this input.
A2	VOUT	Output voltage. A 1.0 µF Low ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 280Ω discharge resistor prevents a charge remaining on V_{OUT} when disabled.
B1	VEN	Enable input; disables the regulator when ≤ 0.4V. Enables the regulator when ≥ 1.2V. An internal 1MΩ pulldown resistor connects this input to ground.
B2	GND	Common ground.

ORDERING INFORMATION

DSBGA PACKAGE (LEAD FREE)(1)		
OUTPUT VOLTAGE (V)	SUPPLIED AS	
	250 TAPE AND REEL	3000 TAPE AND REEL
1.2	LP5904TME-1.2/NOPB	LP5904TMX-1.2/NOPB
1.8(2)	LP5904TME-1.8/NOPB	LP5904TMX-1.8/NOPB
2.5(2)	LP5904TME-2.5/NOPB	LP5904TMX-2.5/NOPB
2.6(2)	LP5904TME-2.6/NOPB	LP5904TMX-2.6/NOPB
2.8	LP5904TME-2.8/NOPB	LP5904TMX-2.8/NOPB
2.85	LP5904TME-2.85/NOPB	LP5904TMX-2.85/NOPB
3.0(2)	LP5904TME-3.0/NOPB	LP5904TMX-3.0/NOPB
3.1	LP5904TME-3.1/NOPB	LP5904TMX-3.1/NOPB
3.2(2)	LP5904TME-3.2/NOPB	LP5904TMX-3.2/NOPB
3.4(2)	LP5904TME-3.4/NOPB	LP5904TMX-3.4/NOPB

(1) Contact your local TI Sales Office for availability of other voltage options.
(2) Not yet released — contact TI sales office for sample availability.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input Voltage		–0.3	6.0	V
V_{OUT}	Output Voltage		–0.3 to (V_{IN} + 0.3V)	6.0	V
V_{EN}	Enable Input Voltage		–0.3 to (V_{IN} + 0.3V)	6.0	V
	Continuous Power Dissipation(4)		Internally Limited		
	Junction Temperature (T_{JMAX})			150	°C
	Storage Temperature Range		–65	150	°C
	Maximum Lead Temperature (Soldering, 10 sec.)			260	°C
	ESD Rating(5)	Human Body Model		2	kV
		Machine Model		200	V

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) All voltages are with respect to the potential at the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

OPERATING RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage Range	2.2		5.5	V
V_{EN}	Enable Voltage Range	0 to (V_{IN} + 0.3)		5.5	V
	Recommended Load Current(3)	0		200	mA
T_J	Junction Temperature Range	–40		+125	°C
T_A	Ambient Temperature Range(3)	–40		+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$. See applications section.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction to Ambient Thermal Resistance(1)	JEDEC Board (DSBGA)(2)			119.6	°C/W
		4L Cellphone Board (DSBGA)			186.5	°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Detailed description of the board can be found in JESD51-7

ELECTRICAL CHARACTERISTICS(1)(2)

Limits in standard typeface are for T_A = 25°C. Limits in boldface type apply over the full operating junction temperature range (–40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5904 Typical Application Circuit with: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{EN} = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, I_{OUT} = 1.0 mA.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage			2.2		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1mA to 200 mA		**–2**		**2**	%
	Line Regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.0V, I_{OUT} = 1 mA			0.06		%/V
		V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.5V, I_{OUT} = 1 mA			0.16		
	Load Regulation	I_{OUT} = 1mA to 200 mA			0.002		%/mA
I_{LOAD}	Load Current	See (3)		0		200	mA
	Maximum Output Current			**200**			
I_Q	Quiescent Current(4)	V_{EN} = 1.2V, I_{OUT} = 0 mA			11	**20**	µA
		V_{EN} = 1.2V, I_{OUT} = 200 mA			250	**325**	
		V_{EN} = 0.3V (Disabled)			0.2	**1.0**	
I_G	Ground Current(5)	I_{OUT} = 0 mA (V_{EN} = 1.2V)			12.2		µA
V_{DO}	Dropout Voltage(6)	I_{OUT} = 100 mA			45		mV
		I_{OUT} = 200 mA			95	**150**	
I_{SC}	Short Circuit Current Limit	See (7)		220	450		mA
PSRR	Power Supply Rejection Ratio(8)	f = 100 Hz, I_{OUT} = 10 mA			88		dB
		f = 1 kHz, I_{OUT} = 10 mA			80		
		f = 10 kHz, I_{OUT} = 10 mA			70		
		f = 100 kHz, I_{OUT} = 10 mA			50		
		f = 2MHz, I_{OUT} = 10 mA			30		
e_N	Output Noise Voltage(8)	BW = 10 Hz to 100 kHz	I_{OUT} = 1mA		10		μV_{RMS}
			I_{OUT} = 200 mA		6.5		
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature			160		°C
		Hysteresis			15		
LOGIN INPUT THRESHOLDS							
V_{IL}	Low Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V				**0.4**	V
V_{IH}	High Input Threshold (V_{EN})	V_{IN} = 2.2V to 5.5V		**1.2**			V
I_{EN}	Input Current at V_{EN} Pin(9)	V_{EN} = 5.5V and V_{IN} = 5.5V			5.5		µA
		V_{EN} = 0.0V and V_{IN} = 5.5V			0.001		

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not specified, but do represent the most likely norm.
(3) The device maintains a stable, regulated output voltage without a load current.
(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. This specification does not apply for input voltages below 2.2V.
(7) Short Circuit Current is measured with V_{OUT} pulled to 0V and V_{IN} worst case = 5.5V.
(8) This specification is ensured by design.
(9) There is a 1MΩ resistor between V_{EN} and ground on the device.

ELECTRICAL CHARACTERISTICS[1][2] (continued)

Limits in standard typeface are for T_A = 25°C. Limits in boldface type apply over the full operating junction temperature range (–40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP5904 Typical Application Circuit with: $V_{IN} = V_{OUT(NOM)}$ + 1.0V, V_{EN} = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, I_{OUT} = 1.0 mA.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line Transient[10]	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to ($V_{OUT(NOM)}$ + 1.6V) in 30 µs, I_{OUT} = 1mA	**–2**			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6V) to ($V_{OUT(NOM)}$ + 1.0V) in 30 µs, IOUT = 1mA			**2**	
	Load Transient[10]	I_{OUT} = 1mA to 200 mA in 10 µs	**–50**			mV
		I_{OUT} = 200 mA to 1mA in 10 µs			**50**	
	Overshoot on Startup[10]	Stated as a percentage of nominal VOUT			**2**	%
	Turn-on Time	To 95% of $V_{OUT(NOM)}$		85	300	µs

(10) This specification is ensured by design.

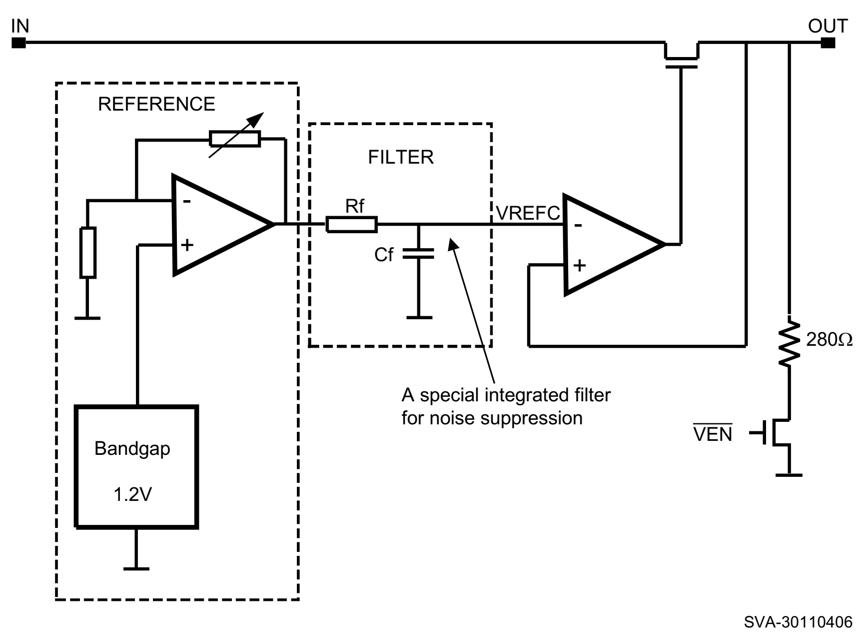
OUTPUT AND INPUT CAPACITORS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[1]	TYP	MAX	UNIT
C_{IN}	Input Capacitance[2]	Capacitance for stability	0.5	1.0		µF
C_{OUT}	Output Capacitance[2]		0.5	1.0	10	
ESR	Output/Input Capacitance[2]		5		500	mΩ

(1) Note: The minimum capacitance should be greater than 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
(2) This specification is ensured by design.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

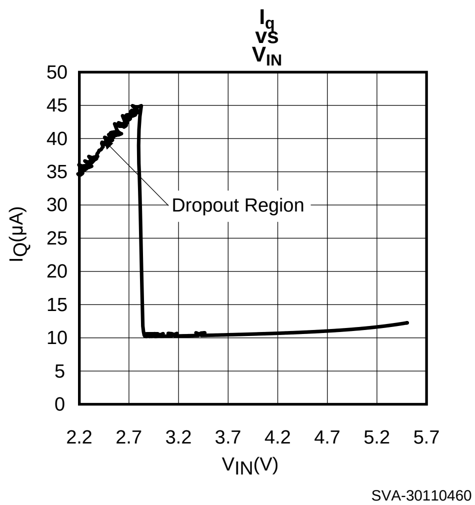


Figure 2.

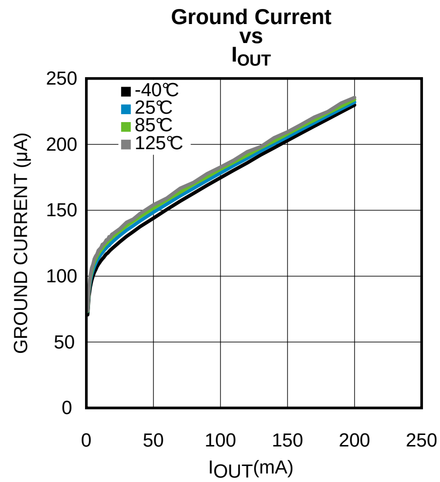


Figure 3.

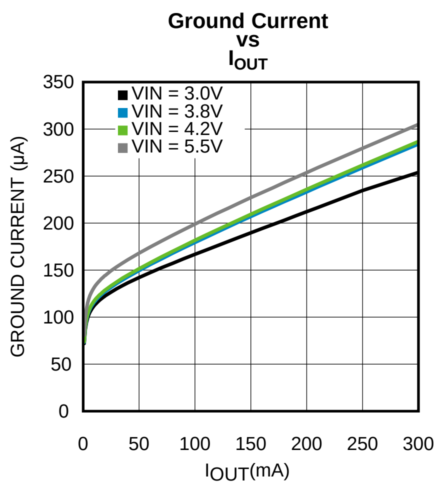


Figure 4.

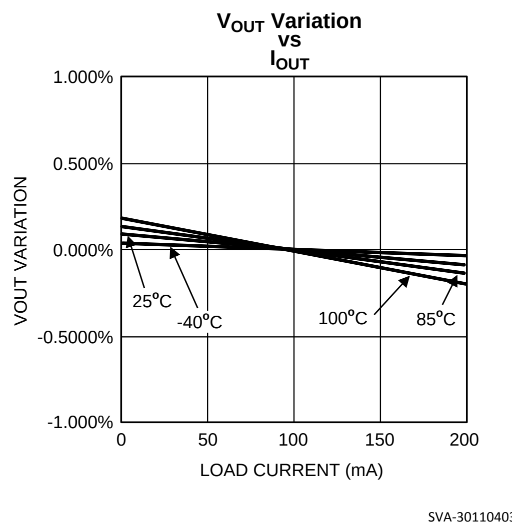


Figure 5.

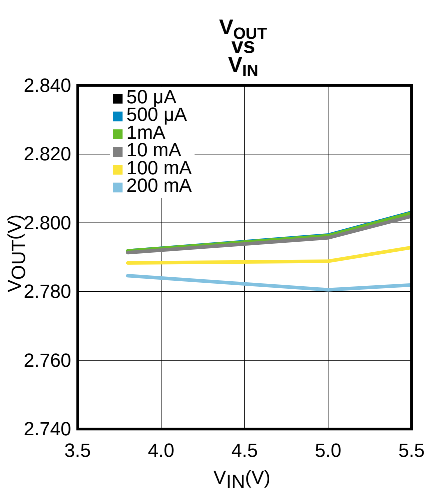


Figure 6.

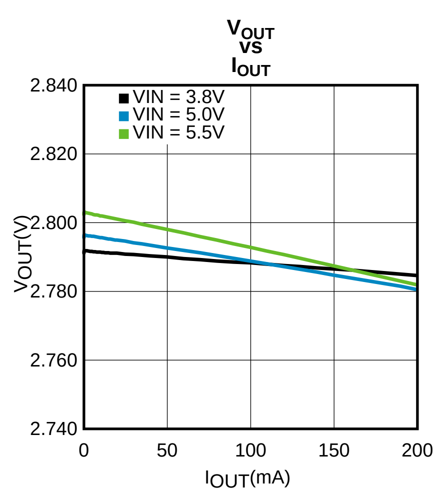


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

VOUT vs IOUT

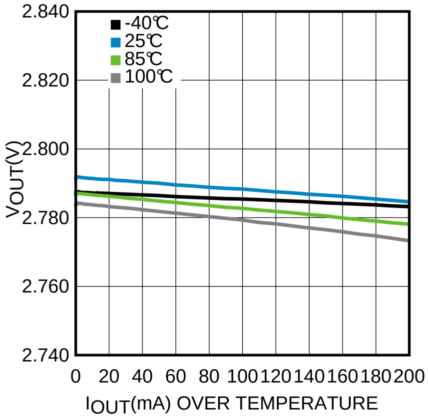


Figure 8.

Startup, No Load

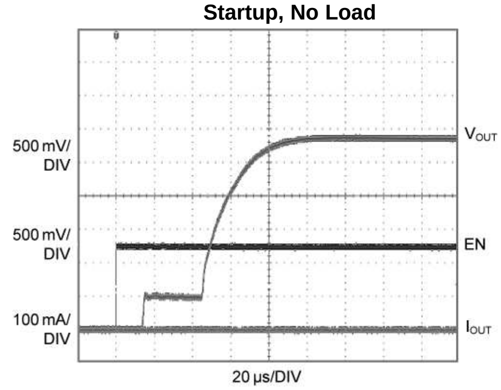


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Figure 9.

Startup, Load = 28Ω

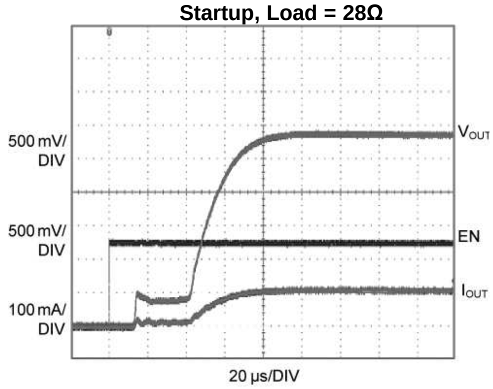

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Figure 10.

Startup, Load = 14Ω

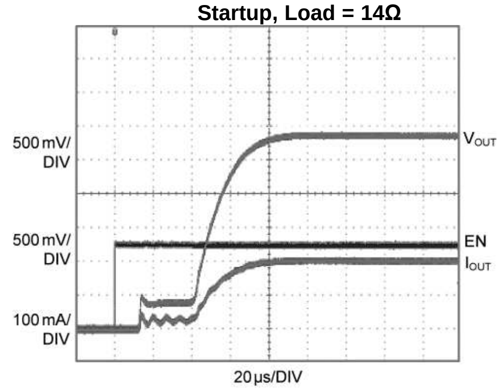

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Figure 11.

Load Transient, Load = 1mA to 200mA, V_{OUT} = 2.8V

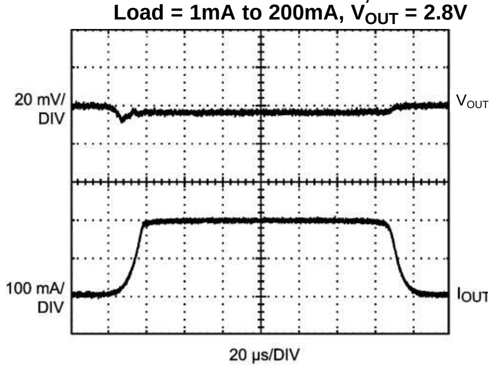

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Figure 12.

Line Transient Load = 1mA, V_{OUT} = 2.8 at V_{IN} Rising Edge

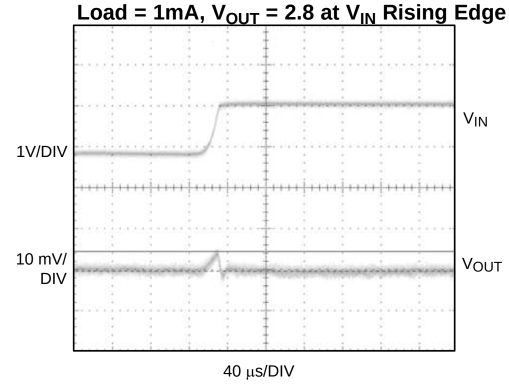

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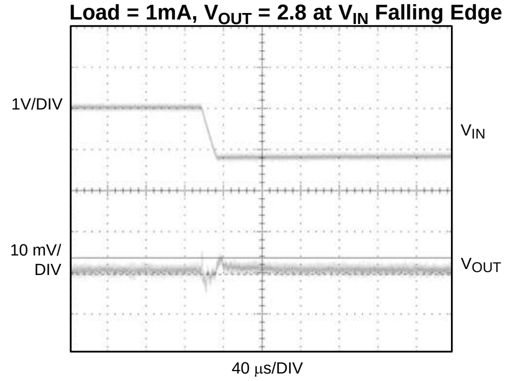
Figure 13.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

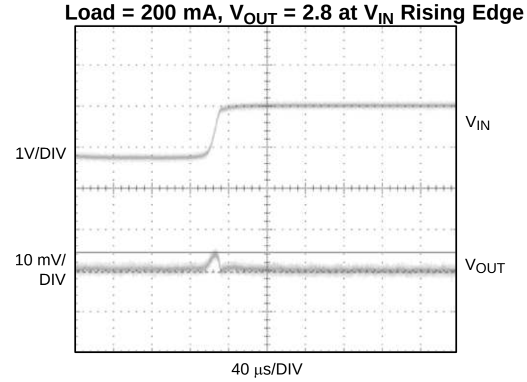
Line Transient
Load = 1mA, V_{OUT} = 2.8 at V_{IN} Falling Edge



SVA-30110413

Figure 14.

Line Transient
Load = 200 mA, V_{OUT} = 2.8 at V_{IN} Rising Edge



SVA-30110414

Figure 15.

Line Transient
Load = 200 mA, V_{OUT} = 2.8 at V_{IN} Falling Edge

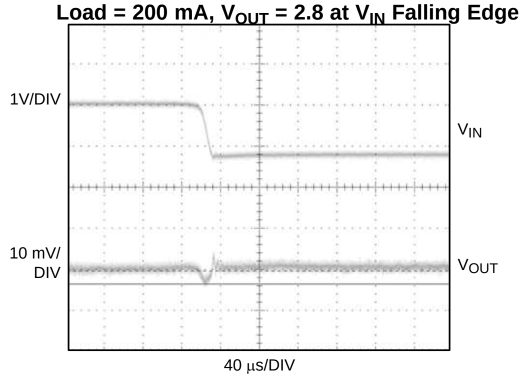


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Figure 16.

Dropout Voltage vs Load Current

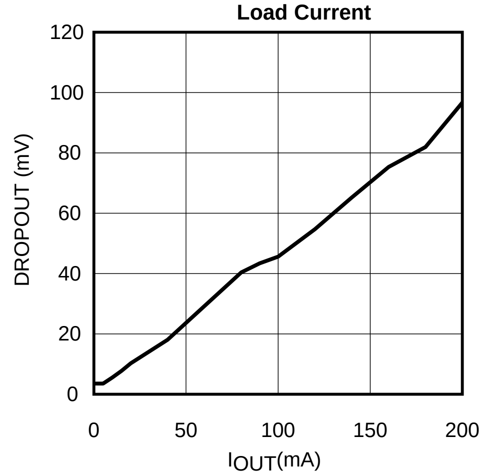

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Figure 17.

PSRR

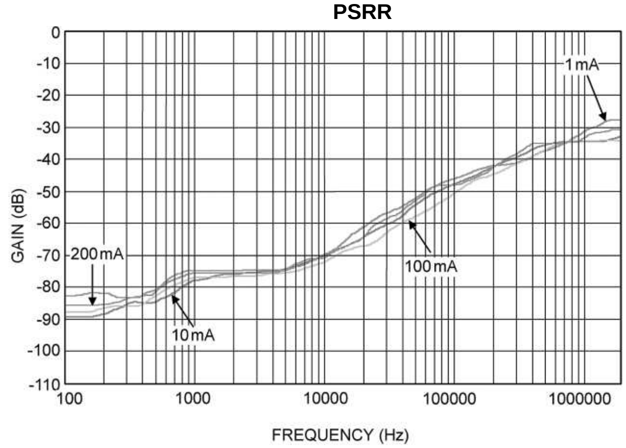

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Figure 18.

Output Noise Spectral Density, V_{OUT} = 2.8V

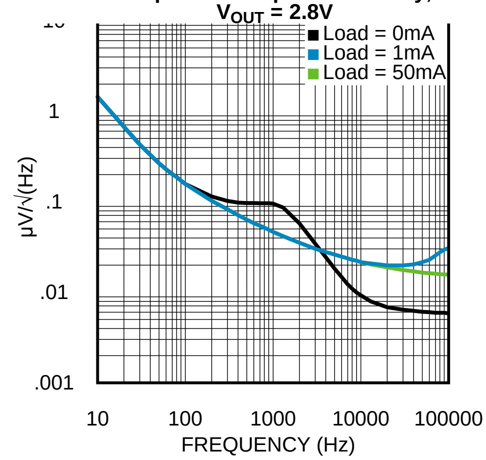

Figure 19.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

Turn On Time, 1 mA Load
V_{OUT} = 2.8V, V_{IN} = 3.93V (Battery)

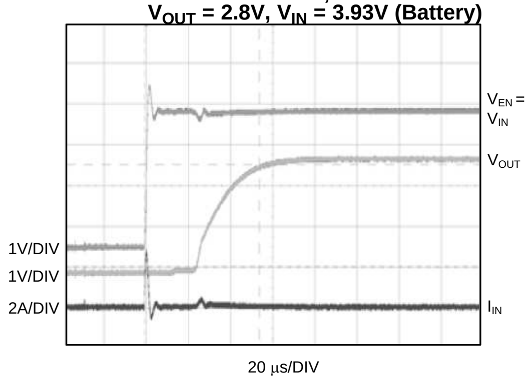

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Figure 20.

Turn OFF Time, no Load,
V_{OUT} = 3.3V

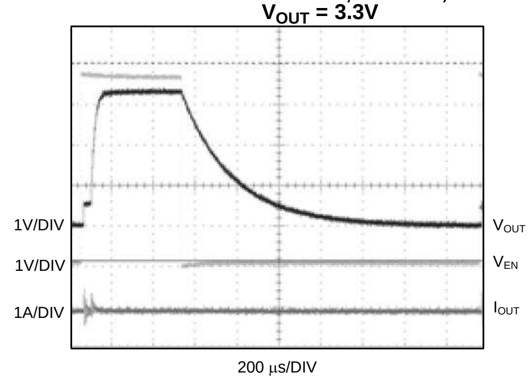

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Figure 21.

Turn OFF Time, 1 mA Load
V_{OUT} = 3.3V

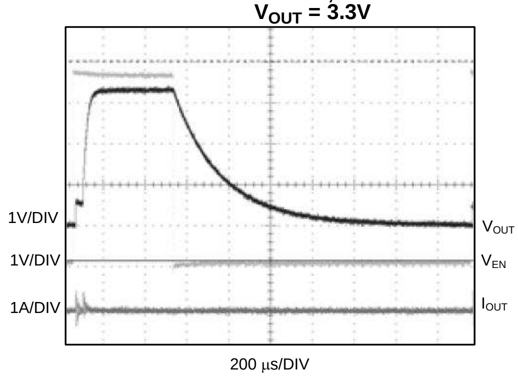

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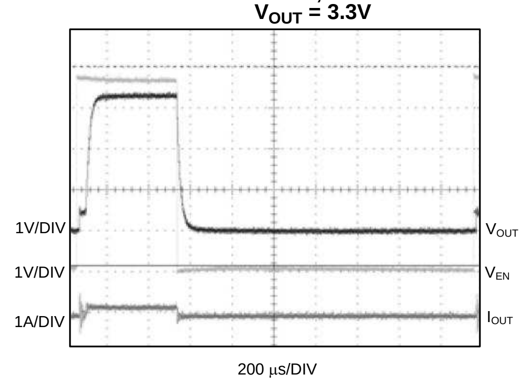
Figure 22.

Turn OFF Time, 200 mA Load
V_{OUT} = 3.3V



SVA-30110420

Figure 23.

Turn OFF Time, V_{EN} = V_{IN} at No Load
V_{OUT} = 3.3V

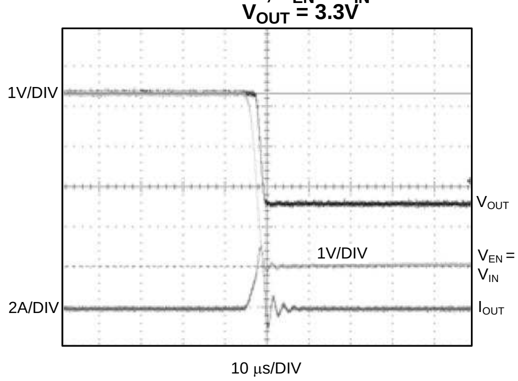


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Figure 24.

Turn OFF Time, V_{EN} = V_{IN} at 200 mA
V_{OUT} = 3.3V

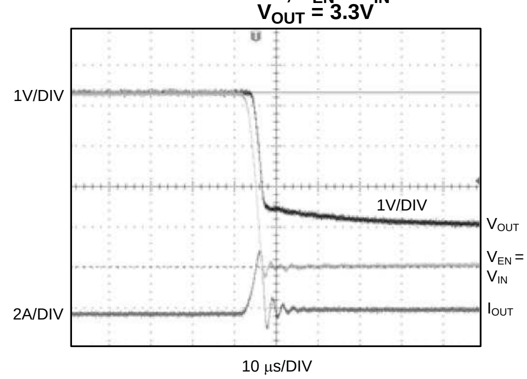

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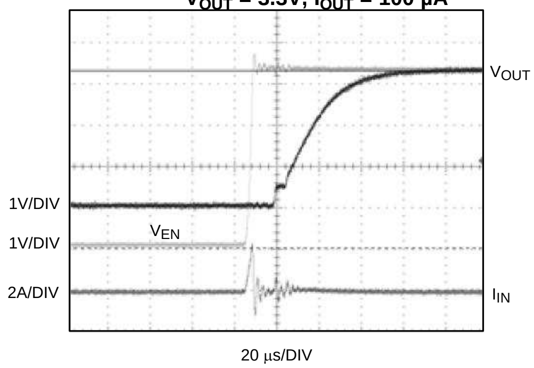
Figure 25.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

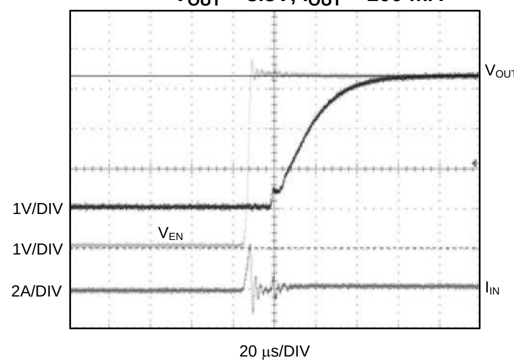
Inrush, V_{IN} = ($V_{OUT(NOM)}$) + 1V, V_{OUT} = 3.3V, I_{OUT} = 100 µA



SVA-30110423

Figure 26.

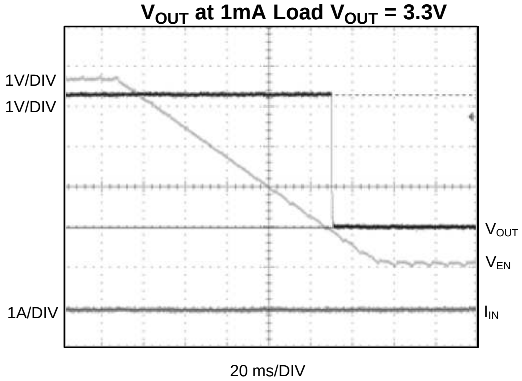
Inrush, V_{IN} = ($V_{OUT(NOM)}$) + 1V, V_{OUT} = 3.3V, I_{OUT} = 200 mA



SVA-30110424

Figure 27.

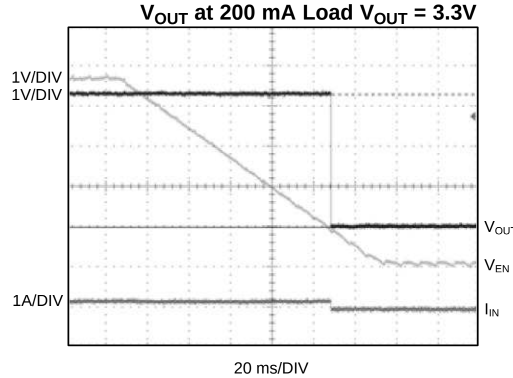
V_{EN} Ramp Down vs V_{OUT} at 1mA Load V_{OUT} = 3.3V



SVA-30110425

Figure 28.

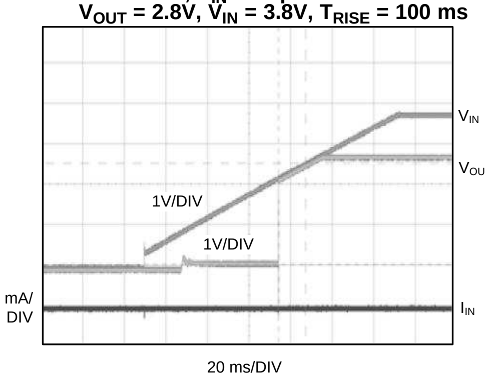
VEN Ramp Down vs V_{OUT} at 200 mA Load V_{OUT} = 3.3V



SVA-30110426

Figure 29.

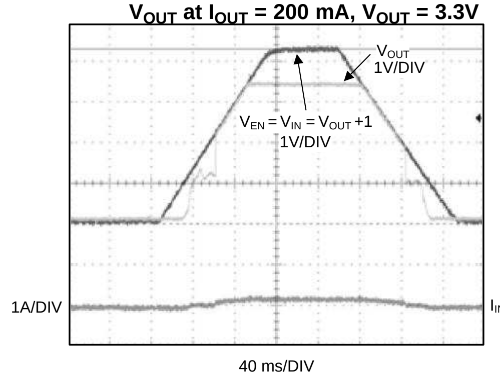
Inrush, V_{IN} Ramp at 1mA Load V_{OUT} = 2.8V, V_{IN} = 3.8V, T_{RISE} = 100 ms



SVA-30110417

Figure 30.

Supply Ramping V_{EN} = V_{IN} = (V_{OUT} + 1V) vs V_{OUT} at I_{OUT} = 200 mA, V_{OUT} = 3.3V



SVA-30110427

Figure 31.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{OUT} = 2.8V, V_{IN} = 3.8V, E_N = 1.2V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, T_A = 25°C.

Supply Ramping $V_{EN} = V_{IN} = (V_{OUT} + 1V)$ vs V_{OUT} at I_{OUT} = 100 µA, V_{OUT} = 3.3V

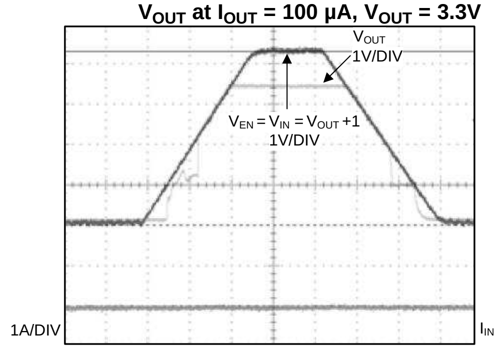


Figure 32.

V_{EN} Ramping vs V_{OUT} at I_{OUT} = 100 µA, VIN = (V_{OUT} + 1V), V_{OUT} = 3.3V

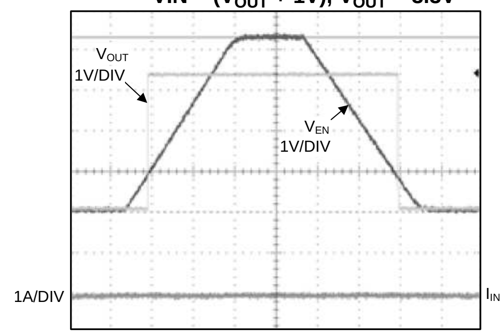


Figure 33.

V_{EN} Ramping vs V_{OUT} at I_{OUT} = 200 mA, V_{IN} = (V_{OUT} + 1V), V_{OUT} = 3.3V

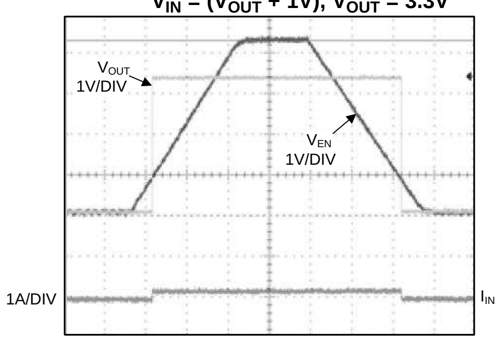


Figure 34.

High Inrush due to Fast Power-On (V_{IN} = V_{EN}) Such as in Hot-Plug

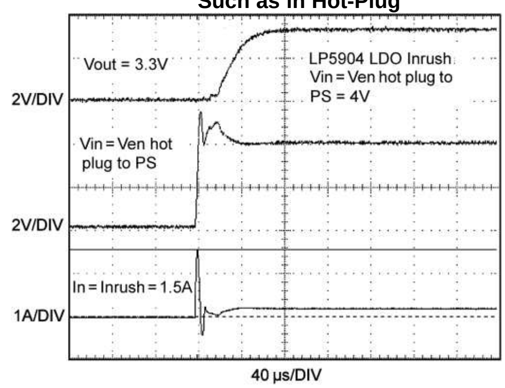


Figure 35.

No Inrush Current in Normal Power-On due to System Capacitance Showing V_{IN} Ramping

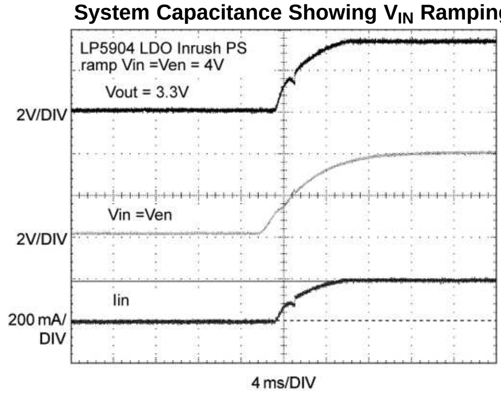


Figure 36.

APPLICATION INFORMATION

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in the Operating Ratings [(1)], the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{JMAX} - T_A}{\theta_{JA}} \quad (1)$$

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN}) - V_{OUT} \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP5904 requires external capacitors for regulator stability. The LP5904 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1.0 µF capacitor has to be connected between the LP5904 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1.0 µF.

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5904, then it is recommended to increase the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 1.0 µF ±30% over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5904 is designed specifically to work with a very small ceramic output capacitor, typically 1.0 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 0.5 µF to 10 µF range, and with ESR between 5mΩ to 500 mΩ, is suitable in the LP5904 application circuit. For this device the output capacitor should be connected between the V_{OUT} pin and a good ground connection.

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application θJA), as given by the following equation: TA-MAX = TJ-MAX-OP – (θJA × PD-MAX). See APPLICATION INFORMATION.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *CAPACITOR CHARACTERISTICS* below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5mΩ to 500 mΩ for stability.

REMOTE CAPACITOR OPERATION

The LP5904 requires at least a 1µF capacitor at output pin, but there is no strict requirements about the location of the capacitor in regards the LDO output pin. In practical designs the output capacitor may be located some 5-10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitor(s) in the system (like a capacitor at the input of supplied part). The Remote Capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitor(s), keeping the LDO trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

CAPACITOR CHARACTERISTICS

The LP5904 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 0.5 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5904.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.5 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

NO-LOAD STABILITY

The LP5904 will remain stable and in regulation with no external load.

ENABLE CONTROL

The LP5904 may be switched ON or OFF by a logic input at the ENABLE pin. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3nA. However, if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator output permanently on.

A 1MΩ pulldown resistor ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112 (SNVA009).

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5904TME-1.2/NOPB	NRND	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		
LP5904TME-2.8/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5904TME-2.85/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5904TME-3.1/NOPB	ACTIVE	DSBGA	YFQ	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5904TMX-1.2/NOPB	NRND	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		
LP5904TMX-2.8/NOPB	NRND	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		
LP5904TMX-2.85/NOPB	NRND	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		
LP5904TMX-3.1/NOPB	NRND	DSBGA	YFQ	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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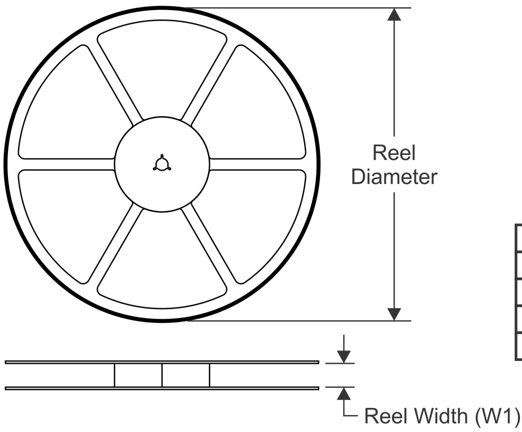
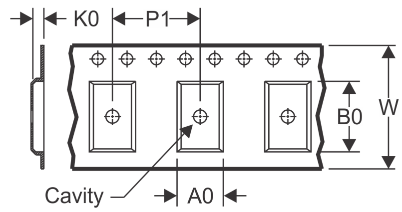
TAPE AND REEL INFORMATION

REEL DIMENSIONS

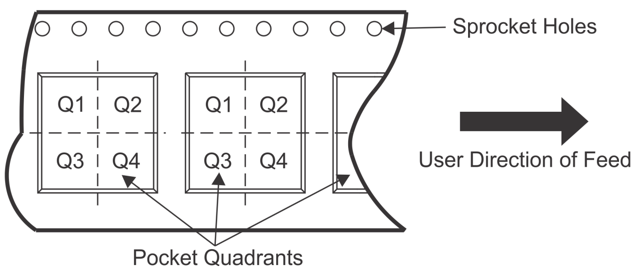


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

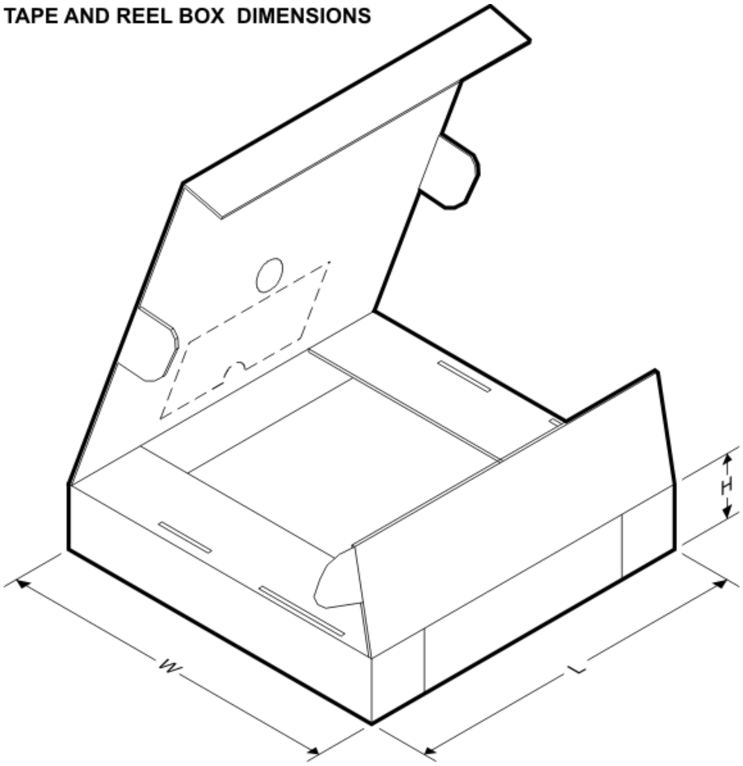
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

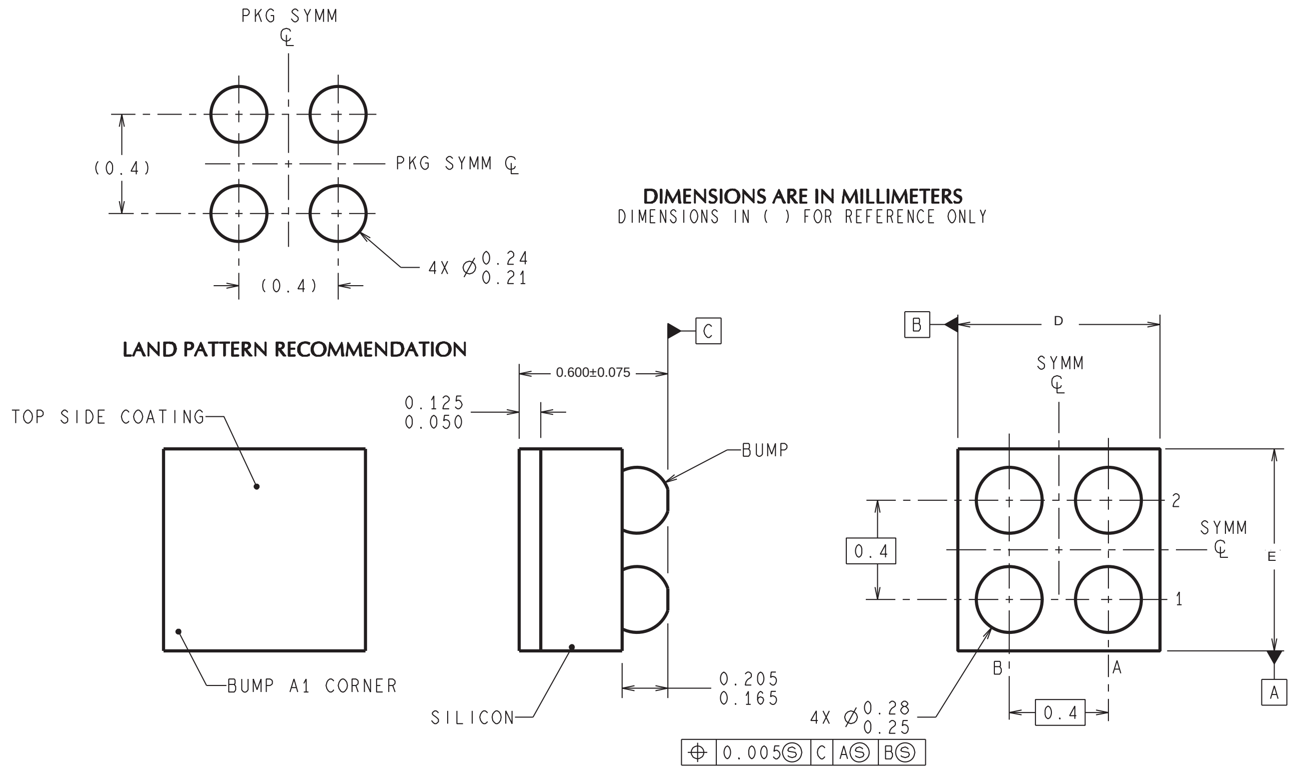
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5904TME-1.2/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TME-2.8/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TME-2.85/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TME-3.1/NOPB	DSBGA	YFQ	4	250	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TMX-1.2/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TMX-2.8/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TMX-2.85/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1
LP5904TMX-3.1/NOPB	DSBGA	YFQ	4	3000	178.0	8.4	0.89	0.89	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5904TME-1.2/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5904TME-2.8/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5904TME-2.85/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5904TME-3.1/NOPB	DSBGA	YFQ	4	250	210.0	185.0	35.0
LP5904TMX-1.2/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5904TMX-2.8/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5904TMX-2.85/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0
LP5904TMX-3.1/NOPB	DSBGA	YFQ	4	3000	210.0	185.0	35.0



TMD04XXX (Rev A)

D: Max = 0.84 mm, Min = 0.78 mm

E: Max = 0.84 mm, Min = 0.78 mm

4215073/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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