- ESD Protection for RS-232 Bus Pins
 ±15-kV Human-Body Model
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V V_{CC} Supply
- Operates Up To 200 kbit/s
- Low Supply Current in Shutdown Mode . . . 2 μA Typical
- External Capacitors . . . 4 × 0.1 μF
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DW OR N PACKAGE (TOP VIEW) NC [18 SHDN C1+ ∏ 17 VCC V+ **∏** 3 16 GND C1- Π 4 15 DOUT1 С2+ Г 14 RIN1 C2-6 13 ROUT1 V- **1** 7 12**∏** DIN1 DOUT2 Π 8 11 ∏ DIN2 10 ROUT2 RIN2

description/ordering information

The MAX222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/μs driver output slew rate. By using SHDN, all receivers can be disabled.

ORDERING INFORMATION

TA	PACI	KAGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP (N)	Tube of 20	MAX222CN	MAX222CN
0°C to 70°C	0010 (DW)	Tube of 20	MAX222CDW	MAYOOO
	SOIC (DW)	Reel of 1000	MAX222CDWR	MAX222C
	PDIP (N)	Tube of 20	MAX222IN	MAX222IN
-40°C to 85°C	SOIC (DW)	Tube of 20	MAX222IDW	MAX222I
	301C (DVV)	Reel of 1000	MAX222IDWR	IVIAAZZZI

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

EACH DRIVER

INPUT D _{IN}	OUTPUT DOUT
L	Н
Н	L

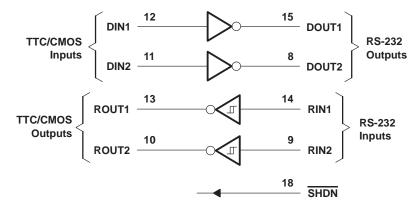
H = high level, L = low level

EACH RECEIVER

INPUT R _{IN}	OUTPUT ROUT
L	Н
Н	L
Open	Н

H = high level, L = low level, Open = input disconnected or connected driver off

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

–0.3 V to 6 V
\dots -0.3 V to V _{CC} - 0.3 V
±30 V
±15 V
$-0.3 \text{ V to V}_{CC} + 0.3 \text{ V}$
Continuous
TBD°C/W
TBD°C/W
150°C
–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
 - 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

		MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	V	
.,	Driver high-level input voltage DIN	2			V	
VIH	Shutdown high-level input voltage SHDN	2			V	
,,	Driver low-level input voltage DIN			0.8	V	
VIL	Shutdown low-level input voltage SHDN			8.0	V	
.,	Driver input voltage D _{IN}	0		5.5	.,	
VI	Receiver input voltage	-30		30	V	
т.	MAX222C	0		70	°C	
TA	Operating free-air temperature MAX222I	-40		85	<u>"</u>	

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 5 V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER		MIN	TYP	MAX	UNIT		
laa	Owner has a supposed	.,	OUDN V	No load		4	10	4
Icc	Supply current	$V_{CC} = 5 V$	SHDN = V _{CC}	$3~k\Omega$ on both inputs	15			mA
	Shutdown supply current					2	50	μΑ
SHDN	Shutdown input leakage current						±1	μΑ

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 5 V \pm 0.5 V.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	ETER TEST CONDITIONS				MAX	UNIT
Vон	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	$D_{IN} = GND$	5	8		V
VOL	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	$D_{IN} = V_{CC}$	-5	-8		V
	Driver high-level input current	DIN = V _{CC}			5	40	
ΙΗ	Control high-level input current	SHDN = V _{CC}			0.01	1	μΑ
	Driver low-level input current	DIN = 0 V			-5	-40	
IIL	Control low-level input current	SHDN = 0 V			-0.01	-1	μΑ
los‡	Short-circuit output current	V _{CC} = 5.5 V,	VO = 0 V	±7	±22		mA
l _{off}	Output leakage current	$V_{CC} = 5.5 \text{ V}, \overline{SHDN} = GND,$	V _O = ±10 V		±0.01	±10	μΑ
r _O	Output resistance	V_{CC} , V+, and V- = 0 V,	V _O = ±2 V	300	10 M		Ω

[†] All typical values are at $V_{CC} = 5$ V, and $T_A = 25$ °C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 5 V \pm 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CO	ONDITIONS	MIN	TYP†	MAX	UNIT
	Data rate	C _L = 1000 pF, One D _{OUT} switching,	$R_L = 3 \text{ k}\Omega$, See Figure 1	200			kbit/s
^t PLH (D)	Propagation delay time, low- to high-level output	See Figure 1			1.5	3.5	μs
^t PHL (D)	Propagation delay time, high- to low-level output	See Figure 1		1.3	3.5	μs	
tPHL (D) - tPLH (D)	Driver (+ to –) propagation delay difference				300		ns
tsk(p)	Pulse skew§	C _L = 150 pF to 2500 pF	$R_L = 3 kΩ$ to $7 kΩ$, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	$R_L = 3 kΩ$ to 7 kΩ, $V_{CC} = 5 V$	C _L = 50 pF to 2500 pF	6	12	30	V/µs
^t ET	Driver output enable time (after SHDN goes high)				250		μs
^t DT	Driver output disable time (after SHDN goes low)				300	·	ns

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 5 V \pm 0.5 V.



^{\$} Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

[§] Pulse skew is defined as |tplh - tphl| of each channel of the same device.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
Vон	High-level output voltage	I _{OH} = −1 mA	3.5	V _{CC} – 0.2 V		V
VOL	Low-level output voltage	I _{OL} = 3.2 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V		1.7	2.4	V
VIT-	Negative-going input threshold voltage	V _{CC} = 5 V	0.8	1.3		V
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})		0.2	0.5	1	V
rį	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

[†] All typical values are at V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 5 V \pm 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
^t PLH (R)	Propagation delay time, low- to high-level output	C _L = 150 pF		0.6	1	μs
tPHL (R)	Propagation delay time, high- to low-level output	C _L = 150 pF		0.5	1	μs
tPHL (R) - tPLH (R)	Receiver (+ to -) propagation delay difference			100		ns
t _{sk(p)}	Pulse skew [‡]			100		ns

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.

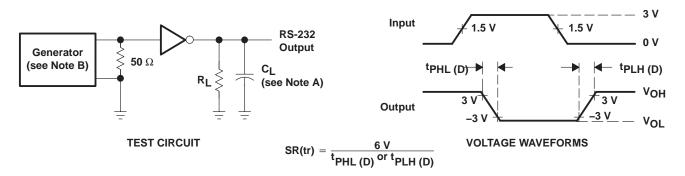
ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
D _{OUT} , R _{IN}	Human-Body Model	±15	kV



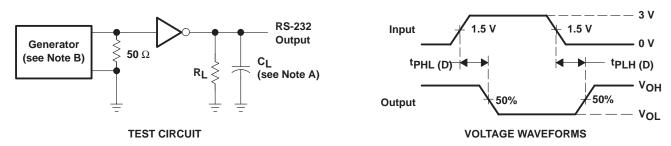
[‡] Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device. NOTE 4: Test conditions are C1–C4 = 0.1 μ F, at V_{CC} = 5 $V \pm 0.5$ V.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \ \Omega$, 50% duty cycle, $t_\Gamma \le 10 \ ns$.

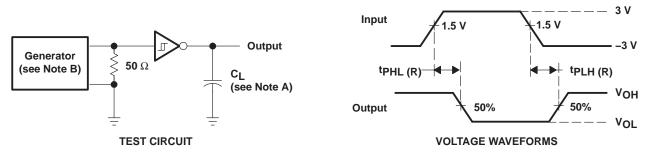
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_f \le 10$ ns. $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



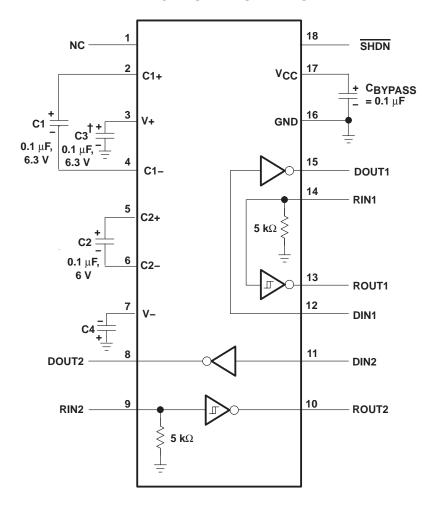
NOTES: A. CL includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω , 50% duty cycle, $t_f \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times



APPLICATION INFORMATION



†C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

capacitor selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX222 requires 0.1- μ F capacitors, although capacitors up to 10 μ F can be used without harm. Ceramic dielectrics are suggested for the 0.1- μ F capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V₊ and V₋.

Use larger capacitors (up to 10 μ F) to reduce the output impedance at V₊ and V₋.

Bypass V_{CC} to ground with at least 0.1 μ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

ESD protection

TI MAX222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

ESD test conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k Ω resistor.

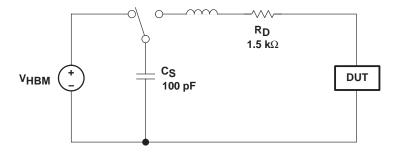


Figure 5. HBM ESD Test Circuit



APPLICATION INFORMATION

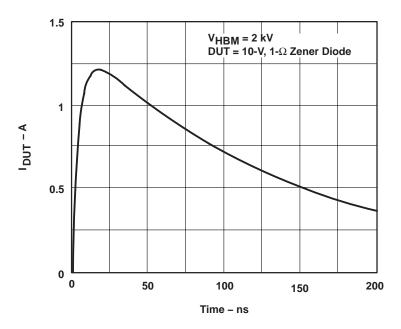


Figure 6. Typical HBM Current Waveform

Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.







10-Apr-2017

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins			Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
MAYOOODNA	(1)	0010		40	Qty	(2)	(6)	(3)	0.1- 70	(4/5)	
MAX222CDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	Samples
MAX222CDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	Samples
MAX222CDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	Samples
MAX222CDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	Samples
MAX222IDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	Samples
MAX222IDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	Samples
MAX222IDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	Samples
MAX222IDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

10-Apr-2017

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX222CDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
MAX222IDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
MAX222CDWR	SOIC	DW	18	2000	370.0	355.0	55.0	
MAX222IDWR	SOIC	DW	18	2000	370.0	355.0	55.0	

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



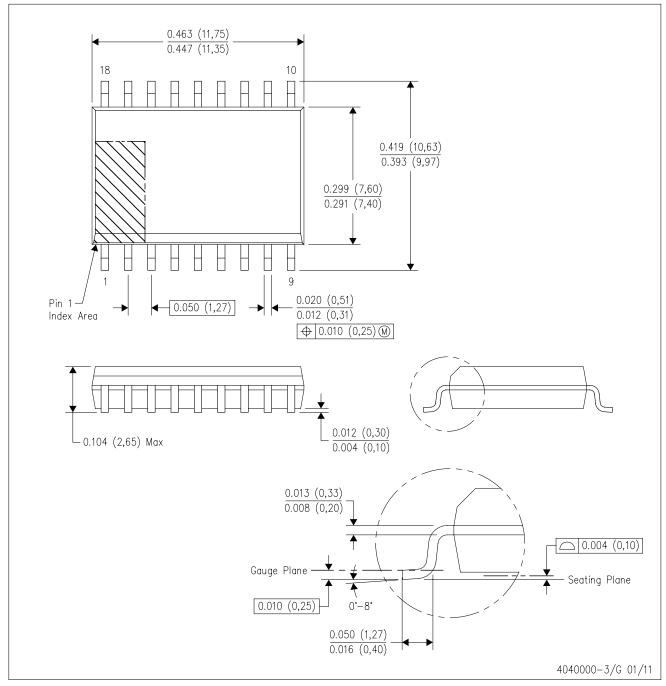
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G18)

PLASTIC SMALL OUTLINE



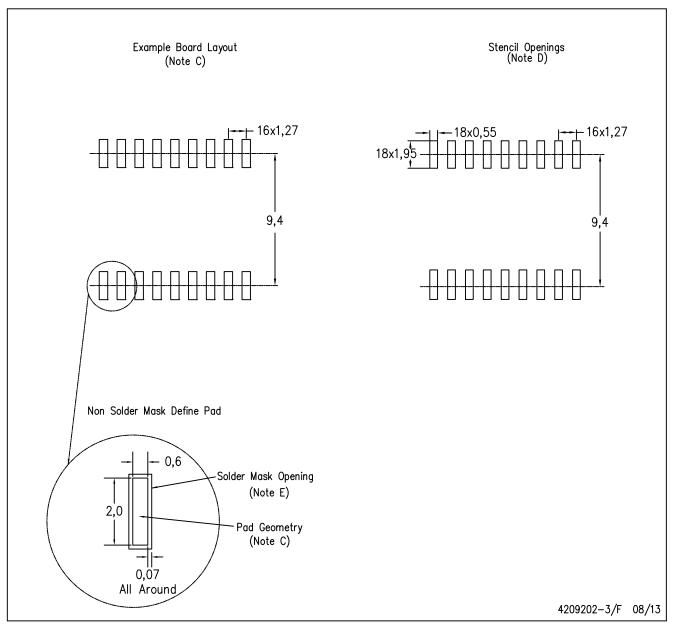
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AB.



DW (R-PDSO-G18)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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