TEXAS INSTRUMENTS

OPA373, OPA374
OPA2373, OPA2374, OPA4374

SBOS279F – SEPTEMBER 2003 – REVISED SEPTEMBER 2016

OPAx373, OPAx374 6.5-MHz, 585-µA, Rail-to-Rail I/O CMOS Operational Amplifier

1 Features

- Low Offset: 5 mV (Maximum)
- Low I_B: 10 pA (Maximum)
- High Bandwidth: 6.5 MHz
- Rail-to-Rail Input and Output
- Single Supply: 2.3 V to 5.5 V
- Shutdown: OPAx373
- Specified up to 125°C
- *Micro*size Packages: 5-Pin SOT-23, 6-Pin SOT-23, 8-Pin SOT-23, and 10-Pin VSON

2 Applications

- Portable Equipment
- Battery-Powered Devices
- Active Filters
- Driving A/D Converters

3 Description

The OPA373 and OPA374 families of operational amplifiers are low power and low cost with excellent bandwidth (6.5 MHz) and slew rate (5 V/µs). The input range extends 200 mV beyond the rails and the output range is within 25 mV of the rails. The speed-power ratio and small size make them ideal for portable and battery-powered applications.

The OPA373 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is less than 1 µA.

The OPA373 and OPA374 families of operational amplifiers are specified for single or dual power supplies of 2.7 V to 5.5 V, with operation from 2.3 V to 5.5 V. All models are specified for –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA373	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (6)	2.90 mm × 1.60 mm
OPA374	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2373	VSON (10)	3.00 mm × 3.00 mm
	VSSOP (10)	3.00 mm × 3.00 mm
OPA2374	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (8)	2.90 mm × 1.63 mm
OPA4374	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

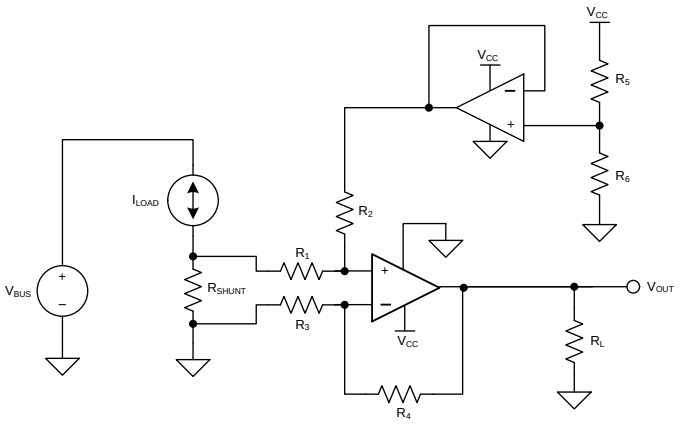


Table of Contents

4 Revision History

Changes from Revision E (May 2008) to Revision F **Page**

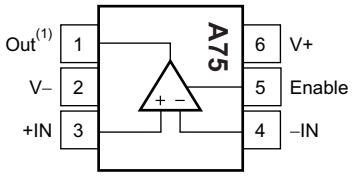
- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Package/Ordering Information* table; refer to *Package Option Addendum* at the end of this data sheet ... 4
- Deleted *lead temperature* specification from Absolute Maximum Ratings ... 7
- Changed values in the *Thermal Information* tables to align with JEDEC standards ... 7

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	SHUTDOWN	PACKAGE-PIN				
			SOIC	SOT-23	VSON	VSSOP	TSSOP
OPA373	1	Yes	8	6	—	—	—
OPA2373	2	Yes	—	—	10	10	—
OPA374	1	No	8	5	—	—	—
OPA2374	2	No	8	8	—	—	—
OPA4374	4	No	14	—	—	—	14

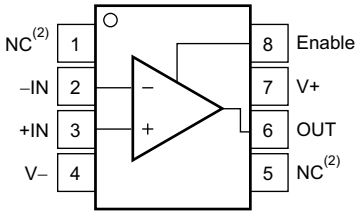
6 Pin Configuration and Functions

OPA373: DBV Package
6-Pin SOT-23
Top View



(1) Pin 1 of the 6-pin SOT-23 is determined by orienting the package marking as shown.

OPA373: D Package
8-Pin SOIC
Top View

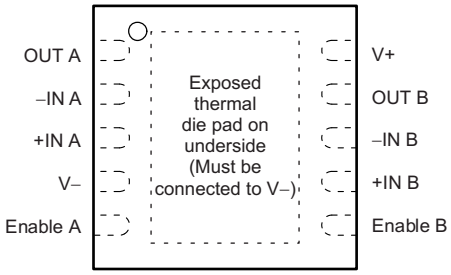


(2) NC indicates no internal connection.

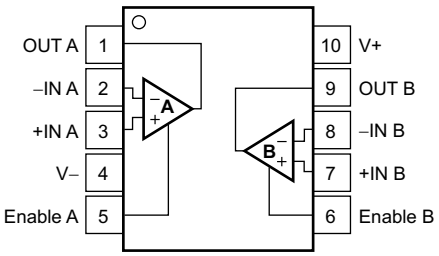
Pin Functions: OPA373

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
Enable	8	5	I	Enable
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	6	—	Positive (highest) power supply

OPA2373: DGS Package
10-Pin VSON
Top View



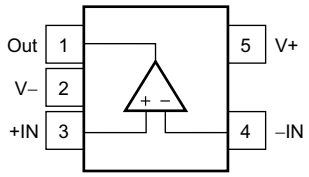
OPA2373: DRC Package
10-Pin VSSOP
Top View



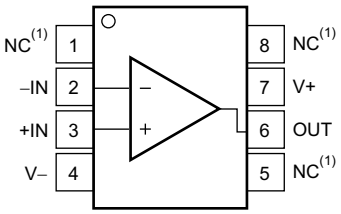
Pin Functions: OPA2373

PIN			I/O	DESCRIPTION
NAME	VSON	VSSOP		
Enable A	5	5	I	Enable A amplifier
Enable B	6	6	I	Enable B amplifier
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	8	8	I	Inverting input, channel B
+IN B	7	7	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	9	9	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	10	10	—	Positive (highest) power supply

OPA374: DBV Package
5-Pin SOT-23
Top View



OPA374: D Package
8-Pin SOIC
Top View

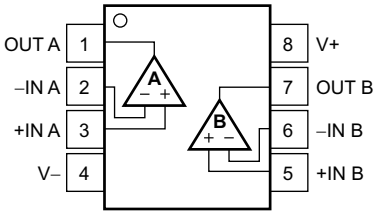


(1) NC indicates no internal connection.

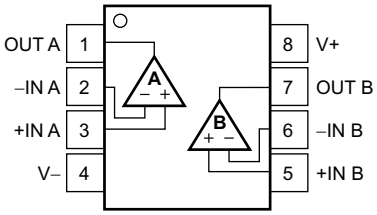
Pin Functions: OPA374

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2374: DCN Package
8-Pin SOT-23
Top View



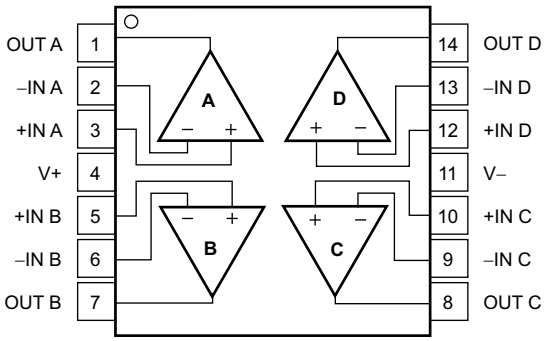
OPA2374: D Package
8-Pin SOIC
Top View



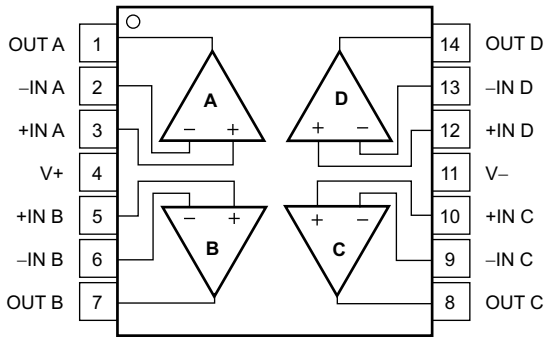
Pin Functions: OPA2374

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

OPA4374: PW Package
14-Pin TSSOP
Top View



OPA4374: D Package
14-Pin SOIC
Top View



Pin Functions: OPA4374

PIN			I/O	DESCRIPTION
NAME	SOIC	TSSOP		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
–IN C	9	9	I	Inverting input, channel C
+IN C	10	10	I	Noninverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply		7	V
	Signal input pin(2)	−0.5	(V+) + 0.5	
Current	Signal input pin(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage	±1.35 (2.7)	±2.75 (5.5)	V
T_A	Operating temperature	–40	125	°C

7.4 Thermal Information: OPA373

THERMAL METRIC(1)		OPA373		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.4	184.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.7	146.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.8	36.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.9	33.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.3	35.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA374

THERMAL METRIC(1)		OPA374		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.1	220.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.7	129	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.5	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.2	21	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65	45.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA2373

THERMAL METRIC(1)		OPA2373		UNIT
		DGS (VSON)	DRC (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.6	56.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.8	76.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.6	30.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Thermal Information: OPA2374

THERMAL METRIC(1)		OPA2374		UNIT
		D (SOIC)	DCN (SOT-23)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.8	171.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	73.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.4	106.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.3	15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	105.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.8 Thermal Information: OPA4374

THERMAL METRIC(1)		OPA4374		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	112.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.8	56.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.9 Electrical Characteristics: V_S = 2.7 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			1	5	mV
	Input offset voltage versus temperature	T_A = –40°C to 125°C				6.5	mV
dV_{OS}/dT	Input offset voltage versus drift	T_A = –40°C to +125°C			3		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 2.7 V to 5.5 V, V_{CM} < (V+) – 2 V	T_A = 25°C		25	100	µV/V
			T_A = –40°C to 125°C			150	
	Channel separation, DC				0.4		µV/V
		At f = 1 kHz			128		dB
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 2 V	T_A = 25°C	80	90		dB
			T_A = –40°C to 125°C	70			
		V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V	T_A = 25°C	66			dB
			T_A = –40°C to 125°C	60			dB
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
I_{OS}	Input offset current				±0.5	±10	pA
INPUT IMPEDANCE							
	Differential				10^{13} || 3		Ω || pF
	Common-mode				10^{13} || 6		Ω || pF
NOISE							
	Input voltage noise	V_{CM} < (V+) – 2 V, f = 0.1 Hz to 10 Hz			10		μV_{PP}
e_n	Input voltage noise density	V_{CM} < (V+) – 2 V, f = 10 kHz			15		nV/√Hz
i_n	Input current noise density	V_{CM} < (V+) – 2 V, f = 10 kHz			4		fA/√Hz
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V	T_A = 25°C	94	110		dB
			T_A = –40°C to 125°C	80			
		V_S = 5 V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V	T_A = 25°C	94	106		dB
			T_A = –40°C to 125°C	80			
OUTPUT							
	Voltage output swing from rail	R_L = 100 kΩ	T_A = 25°C		18	25	mV
			T_A = –40°C to 125°C			25	mV
		R_L = 5 kΩ	T_A = 25°C		100	125	mV
			T_A = –40°C to 125°C			125	mV
I_{SC}	Short-circuit current			See *Typical Characteristics*			
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
R_O	Open-loop output impedance	f = 1 MHz, I_O = 0 mA			220		Ω

Electrical Characteristics: V_S = 2.7 V to 5.5 V (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF			6.5		MHz
SR	Slew rate	C_L = 100 pF, G = +1			5		V/µs
t_S	Settling time	0.1%, C_L = 100 pF, V_S = 5 V, 2-V step, G = +1			1		µs
		0.01%, C_L = 100 pF, V_S = 5 V, 2-V step, G = +1			1.5		µs
	Overload recovery time	C_L = 100 pF, V_{IN} ● Gain > V_S			0.3		µs
THD+N	Total harmonic distortion + noise	C_L = 100 pF, V_S = 5 V, V_O = 3 V_{PP}, G = +1, f = 1 kHz			0.0013%		
ENABLE OR SHUTDOWN							
t_{OFF}	Turnoff time				3		µs
t_{ON}	Turnon time				12		µs
V_L	Logic low threshold	Shutdown		V–		(V–) + 0.8	V
V_H	Logic high threshold	Amplifier is active		(V–) + 2		V+	V
	Input bias current of Enable pin				0.2		µA
$I_{Q(sd)}$	Quiescent current at shutdown (per amplifier)				< 0.5	1	µA
POWER SUPPLY							
V_S	Specified voltage range			2.7		5.5	V
	Operating voltage range				2.3 to 5.5		V
I_Q	Quiescent current (per amplifier)	I_O = 0 mA	T_A = 25°C		585	750	µA
			T_A = –40°C to 125°C			800	µA
TEMPERATURE							
	Specified range			–40		125	°C
T_A	Operating range			–55		150	°C
T_{stg}	Storage range			–65		150	°C

7.10 Typical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

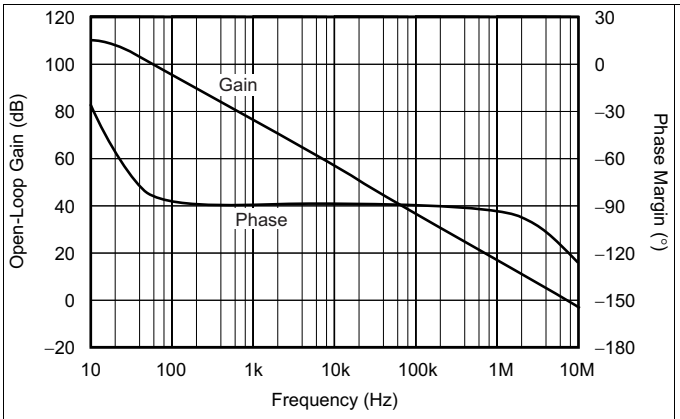


Figure 1. Open-Loop Gain and Phase vs Frequency

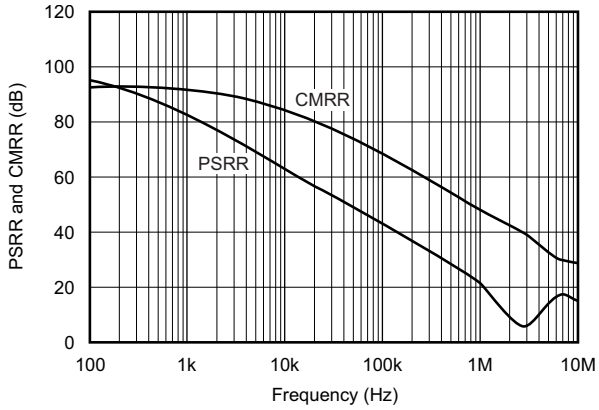


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

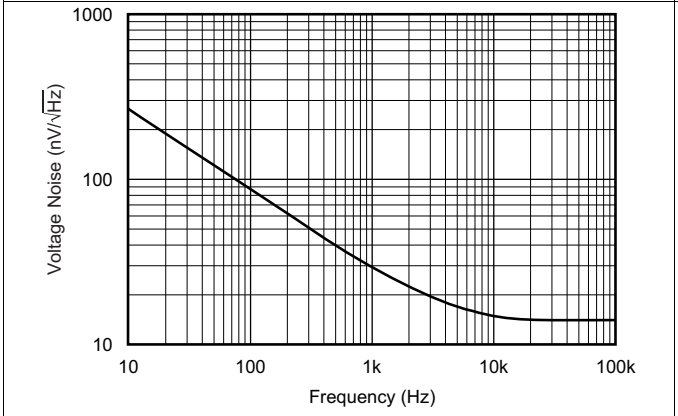


Figure 3. Input Voltage Noise Spectral Density vs Frequency

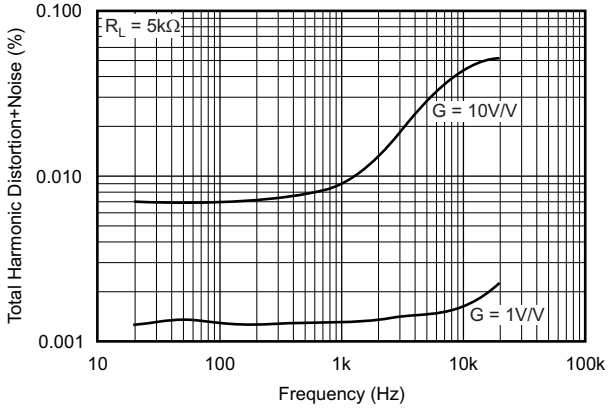


Figure 4. Total Harmonic Distortion + Noise vs Frequency

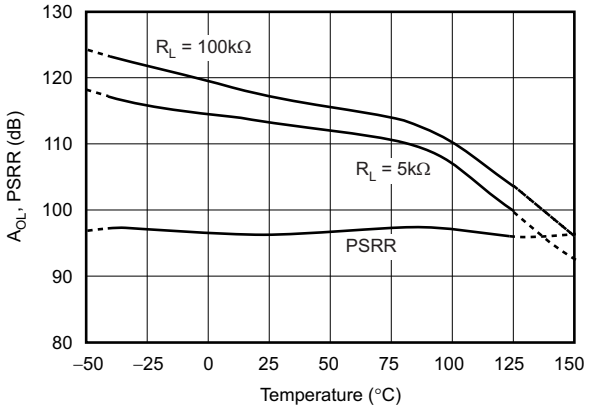


Figure 5. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

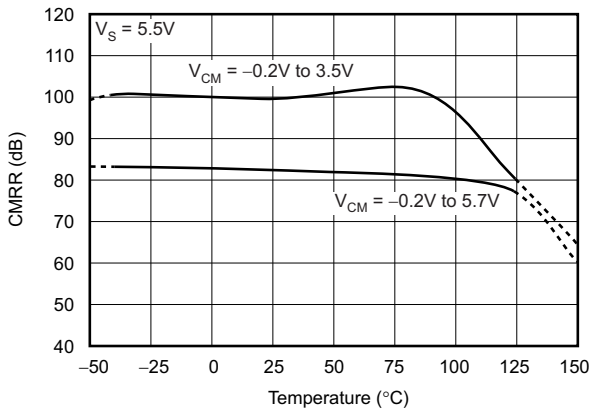


Figure 6. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$ (unless otherwise noted)

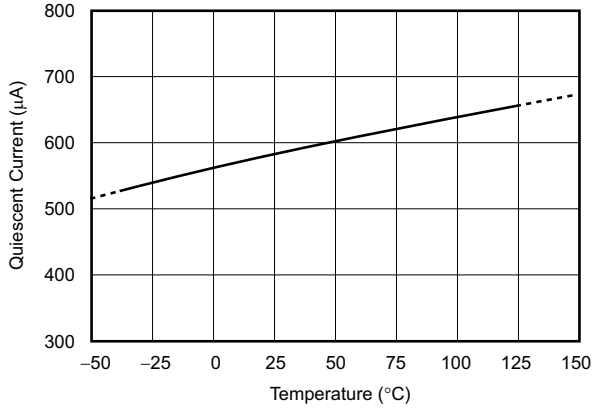


Figure 7. Quiescent Current vs Temperature

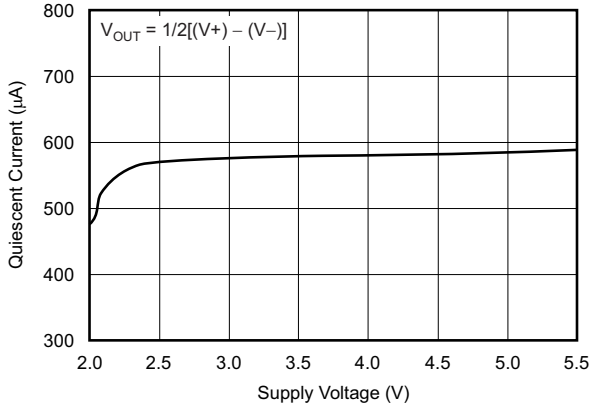


Figure 8. Quiescent Current vs Supply Voltage

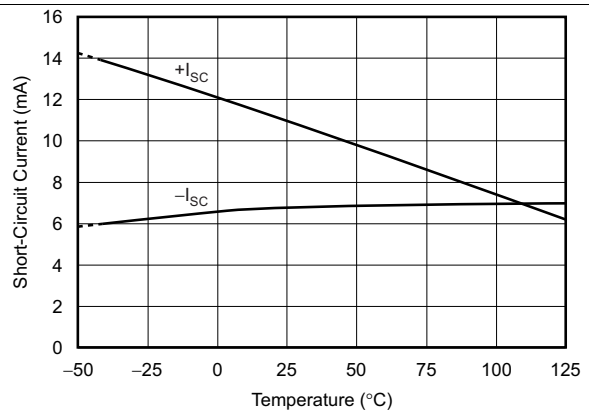


Figure 9. Short-Circuit Current vs Temperature

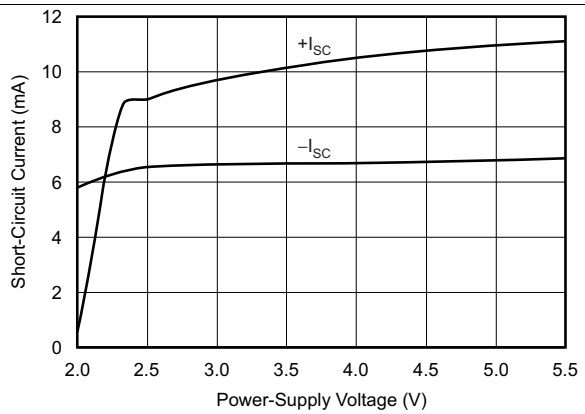


Figure 10. Continuous Short-Circuit Current vs Power-Supply Voltage

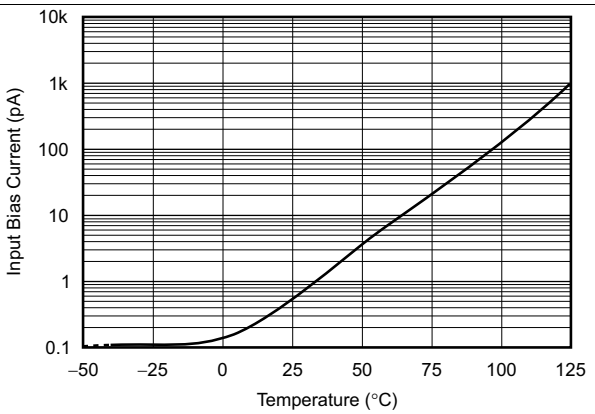


Figure 11. Input Bias Current vs Temperature

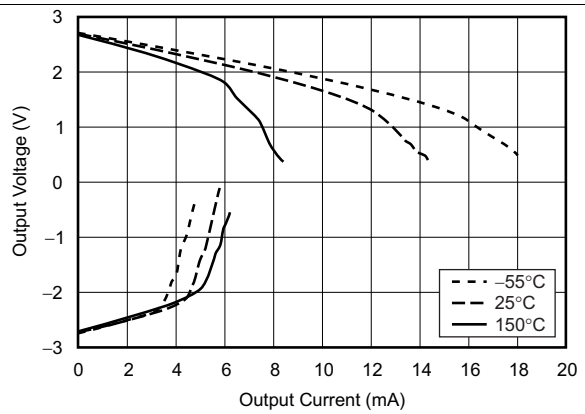


Figure 12. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

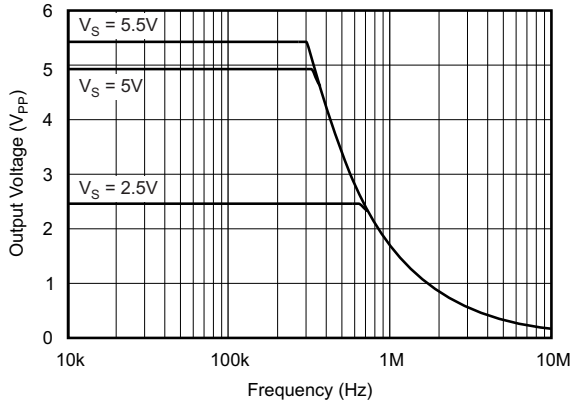


Figure 13. Maximum Output Voltage vs Frequency

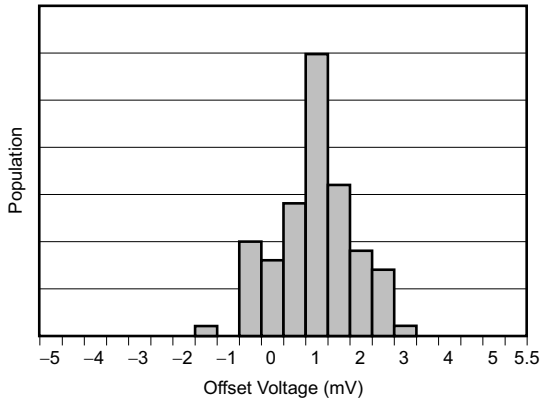


Figure 14. Offset Voltage Production Distribution

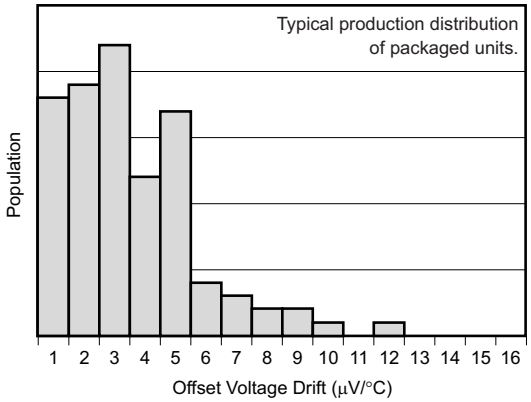


Figure 15. Offset Voltage Drift Magnitude Production Distribution

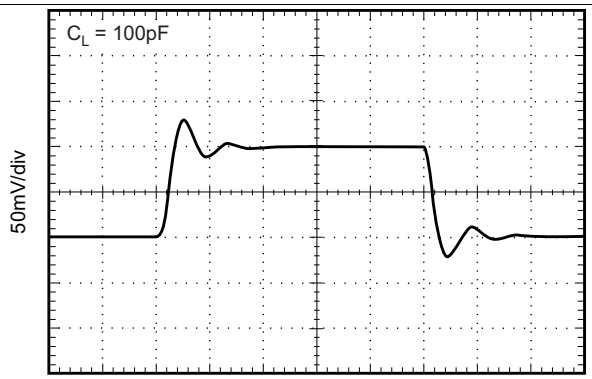


Figure 16. Small-Signal Step Response

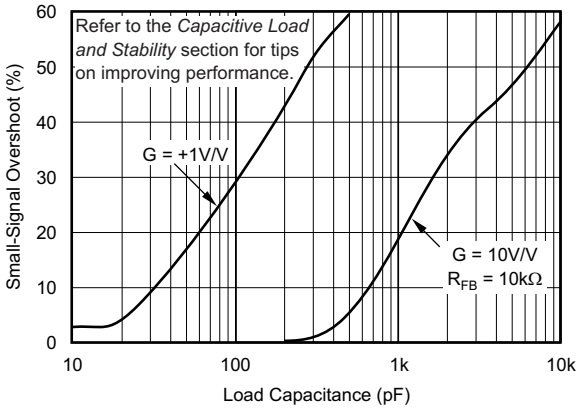


Figure 17. Small-Signal Overshoot vs Load Capacitance

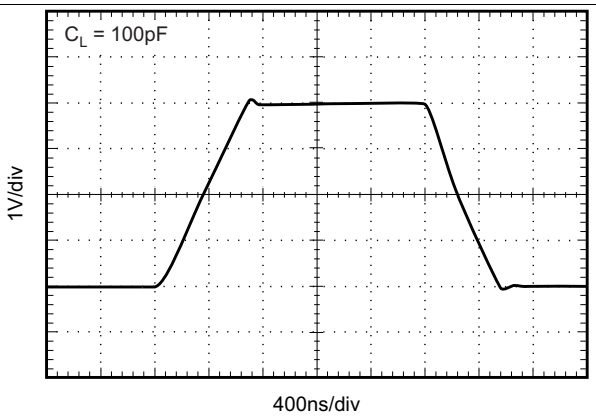


Figure 18. Large-Signal Step Response

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

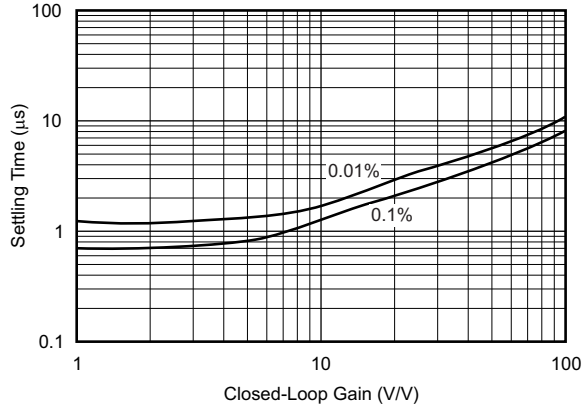


Figure 19. Settling Time vs Closed-Loop Gain

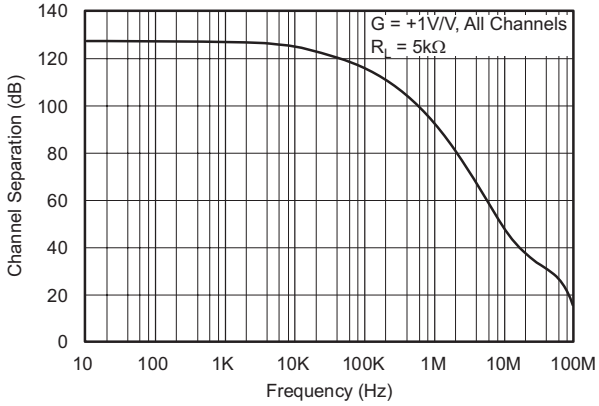


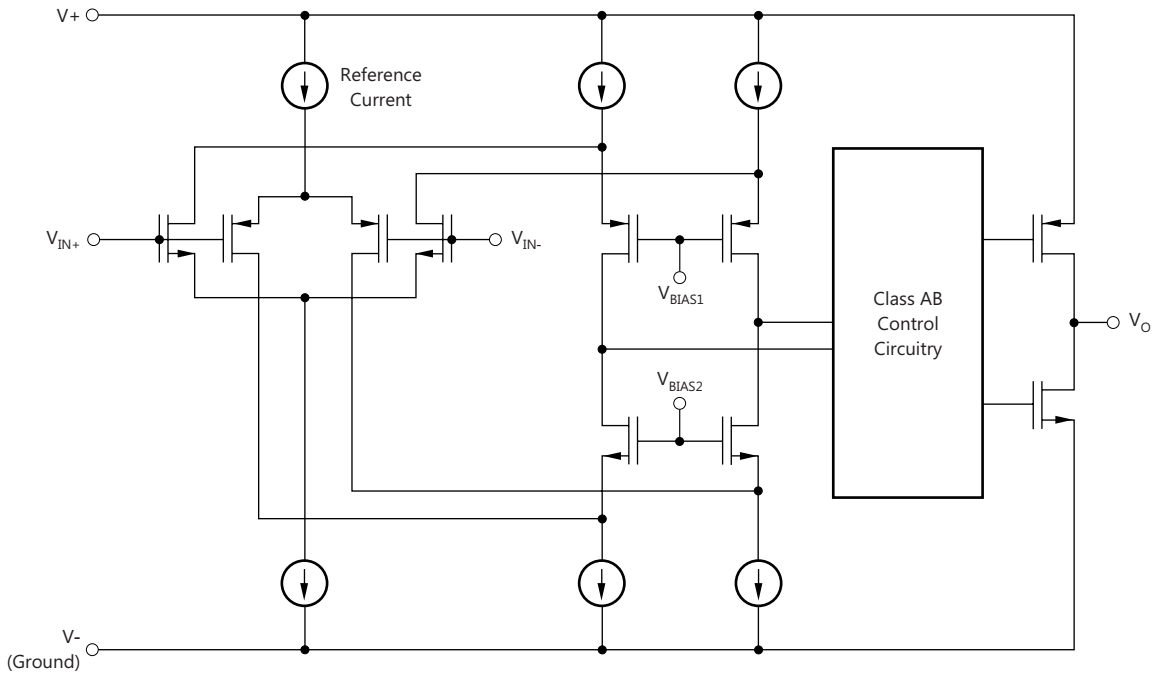
Figure 20. Channel Separation vs Frequency

8 Detailed Description

8.1 Overview

The OPAx373 and OPAx374 operational amplifiers (op amps) are suitable for a broad range of general-purpose applications. As unity-gain stable devices and outstanding AC performance, these op amps are ideal for audio applications. The class AB output stage is capable of driving 100-kΩ loads connected to any point between V+ and ground. These devices are well-suited for nearly any single-supply application up to a supply voltage of 5.5 V because the input common-mode voltage range includes both rails. Rail-to-rail input and output swing significantly increases the overall device dynamic range, especially in low-supply applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPA373 and OPA374 op amps are specified and tested over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.3 V to 5.5 V (±1.15 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics*.

Feature Description (continued)

8.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPA373 and OPA374 series extends 200 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.65 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) − 1.65 V. There is a 500-mV transition region, typically (V+) − 1.9 V to (V+) − 1.4 V, in which both pairs are on. This 500-mV transition region, shown in Figure 21, can vary ±300 mV with process variation. Thus, the transition region (that is, both stages on) can range from (V+) − 2.2 V to (V+) − 1.7 V on the low end, up to (V+) − 1.6 V to (V+) − 1.1 V on the high end. Within the 500-mV transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded, compared to device operation outside this region.

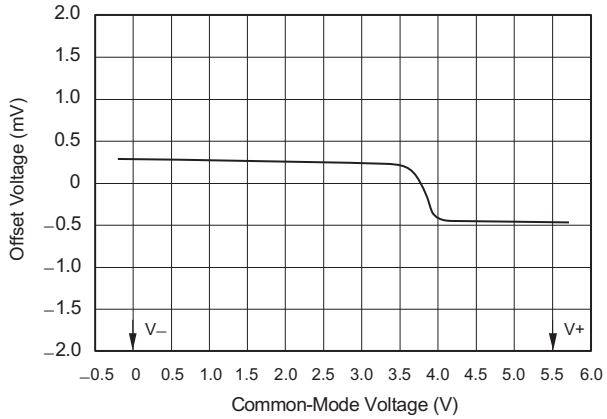


Figure 21. Behavior of Typical Transition Region at Room Temperature

8.3.3 Rail-to-Rail Input

The input common-mode range extends from (V−) − 0.2 V to (V+) + 0.2 V. For normal operation, inputs must be limited to this range. The absolute maximum input voltage is 500 mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, do not cause any damage to the op amp. Unlike some other op amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 22.

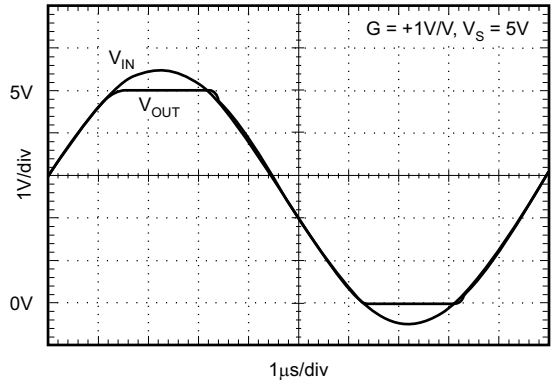


Figure 22. OPA373: No Phase Inversion With Inputs Greater Than the Power-Supply Voltage

Normally, input bias current is approximately 500 fA; however, input voltages exceeding the power supplies by more than 500 mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This limiting is easily accomplished with an input resistor; see Figure 23. Many input signals are inherently current-limited to less than 10 mA, therefore, a limiting resistor is not required.

Feature Description (continued)

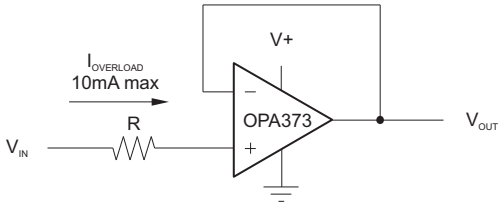


Figure 23. Input Current Protection for Voltages Exceeding the Supply Voltage

8.3.4 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 100 kΩ), the output voltage can typically swing to within 18 mV from the supply rails. With moderate resistive loads (5 kΩ to 50 kΩ), the output can typically swing to within 100 mV from the supply rails and maintain high open-loop gain. See Figure 12 for more information.

8.3.5 Capacitive Load and Stability

The OPA373 series op amps can drive a wide range of capacitive loads. However, under certain conditions, all op amps may become unstable. Op amp configuration, gain, and load value are some of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. The OPA373 series op amps perform well in unity-gain configuration, with a pure capacitive load up to approximately 250 pF. Increased gains allow the amplifier to drive more capacitance. See Figure 17 for further details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 24. This configuration significantly reduces ringing while maintaining DC performance for purely capacitive loads. When there is a resistive load in parallel with the capacitive load, R_S must be placed within the feedback loop as shown to allow the feedback loop to compensate for the voltage divider created by R_S and R_L.

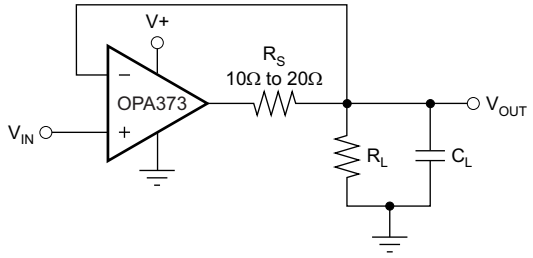


Figure 24. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

Feature Description (continued)

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small-valued resistors. However, when large-valued resistors cannot be avoided, a small (4-pF to 6-pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 25. This technique significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance and printed-circuit board (PCB) parasitic capacitance.

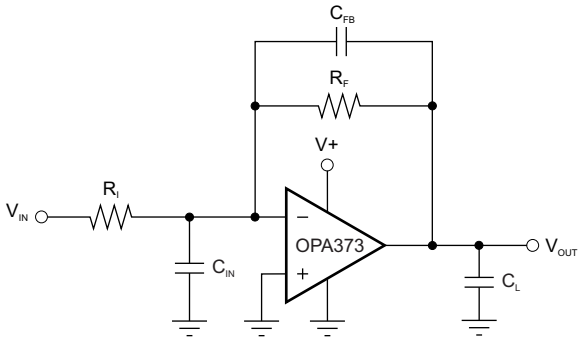


Figure 25. Improving Capacitive Load Drive

For example, when driving a 100-pF load in unity-gain inverter configuration, adding a 6-pF capacitor in parallel with the 10-kΩ feedback resistor decreases overshoot from 57% to 12%, as shown in Figure 26.

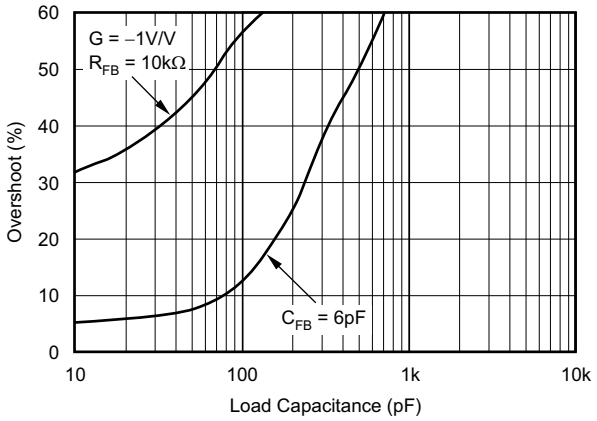


Figure 26. Improving Capacitive Load Drive

8.3.6 Enable or Shutdown

The OPA373 and OPA374 series op amps typically require 585-µA quiescent current. The enable or shutdown feature of the OPA373 allows the op amp to be shut off to reduce this current to less than 1 µA.

8.4 Device Functional Modes

The OPAx374 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx374 is 5.5 V (±2.75 V).

The OPAx373 has two functional modes: active and shutdown. When the voltage at the Enable pin is from V– to (V–) + 0.8 V, the device is in shutdown and consumes less than 0.5 µA of quiescent current (typical). To activate, or enable, the device, the voltage at the Enable pin must be from (V–) + 2 V to V+. When active, the power-supply requirements are the same as the OPAx374.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA373 and OPA374 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input and output make them ideal for driving sampling analog-to-digital converters (ADCs). Excellent AC performance makes them well-suited for audio applications. The class AB output stage is capable of driving 100-kΩ loads connected to any point between V+ and ground.

The input common-mode voltage range includes both rails, allowing the OPA373 and OPA374 series op amps to be used in virtually any single-supply application up to a supply voltage of 5.5 V. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

9.2 Typical Application

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1 A to 1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA2374 because of its rail-to-rail input and output range and cost compared to performance. One of the amplifiers is configured as a difference amplifier, and the other amplifier provides the reference voltage.

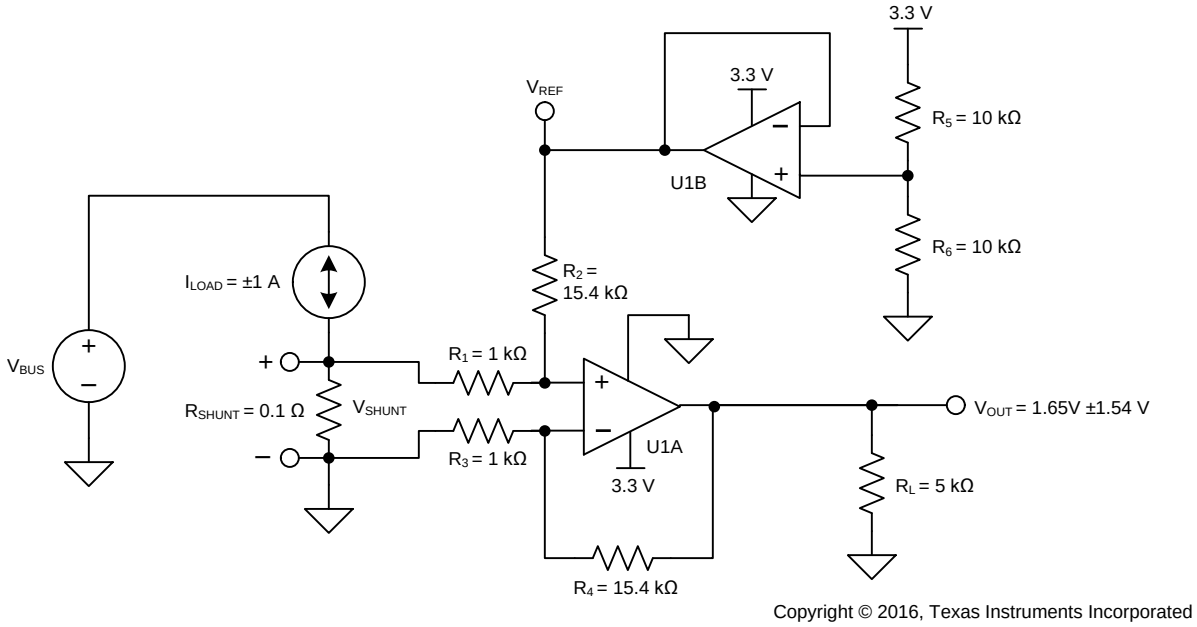


Figure 27. Single-Supply, Low-Side, Bidirectional Current-Sensing Solution

9.2.1 Design Requirements

This design has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

Typical Application (continued)

9.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

(1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches the ratio of R_2/R_1. The ratio of R_2/R_1 impacts the CMRR of the difference amplifier, which ultimately translates to an offset error.

This is a low-side measurement. Therefore, the value of V_{SHUNT} is the ground potential for the system load. Thus, it is important to place a maximum value on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT\_Max} = \frac{|V_{SHUNT\_Max}|}{|I_{LOAD\_Max}|} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

Because the load current is bidirectional, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the op amp, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device.

It is therefore important to use an op amp, such as the OPA374, that has a common-mode range that extends below the negative supply voltage.

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA374 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and output swing of the OPA374, given a 3.3-V supply.

$$–200\ mV < V_{CM} < 3.5\ V \quad (3)$$

$$100\ mV < V_{OUT} < 3.2\ V \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1\ A)]} = 15.5\ \frac{V}{V} \quad (5)$$

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

Because the gain error of the circuit primarily depends on R_1 through R_4, 0.1% resistors were selected. This value reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

Typical Application (continued)

9.2.3 Application Curve

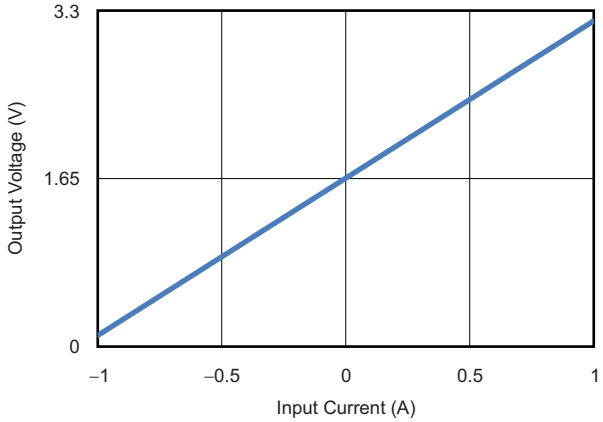


Figure 28. Output Voltage vs Input Current

9.3 System Examples

9.3.1 Driving ADCs

The OPA373 and OPA374 series op amps are optimized for driving medium-speed sampling ADCs. The OPA373 and OPA374 op amps buffer the ADC input capacitance and resulting charge injection, while providing signal gain.

The OPA373 is shown driving the ADS7816 in a basic noninverting configuration, as Figure 29 shows. The ADS7816 is a 12-bit, MicroPower sampling converter in the 8-pin VSSOP package. When used with the low-power, miniature packages of the OPA373, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide anti-aliasing filtering.

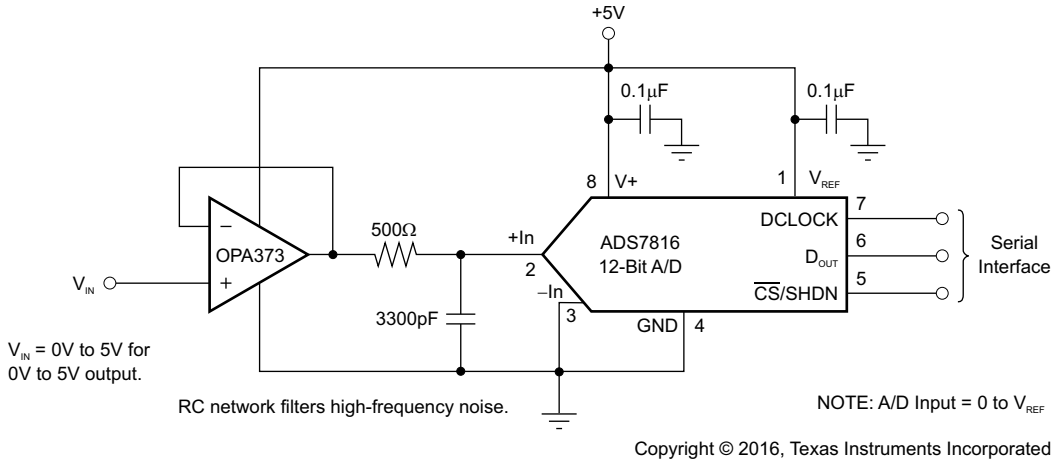


Figure 29. The OPA373 in Noninverting Configuration Driving the ADS7816

System Examples (continued)

Figure 30 shows the OPA373 driving the ADS7816 in a speech bypass-filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit operates with V_S = 2.7 V to 5 V.

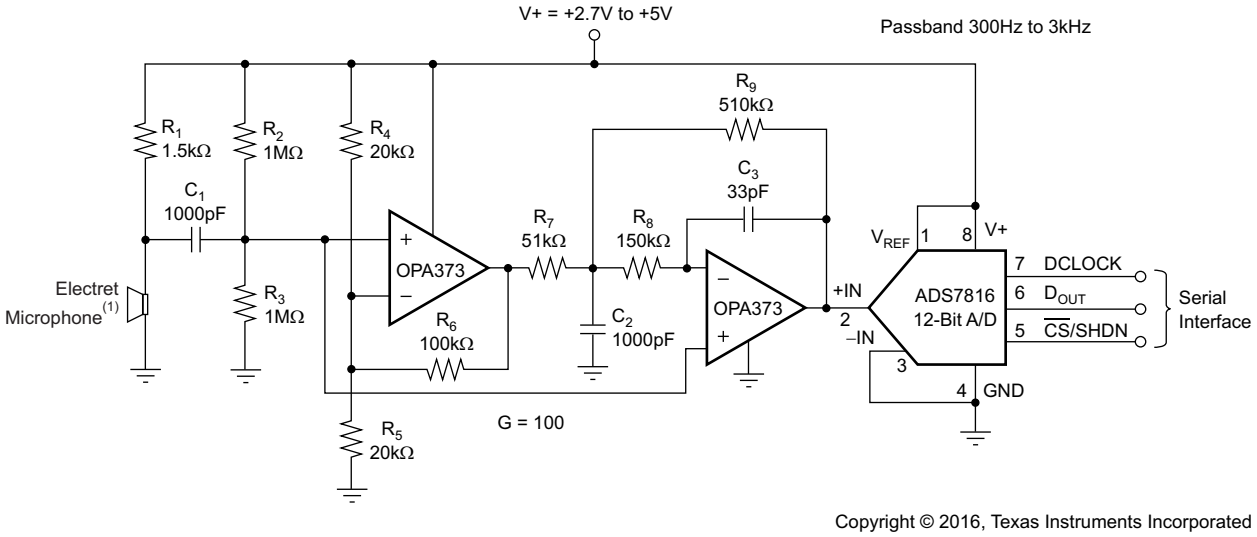


Figure 30. The OPA2373 as a Speech Bypass-Filtered Data Acquisition System

The OPA373 is shown in the inverting configuration described in Figure 31. In this configuration, filtering may be accomplished with the capacitor across the feedback resistor.

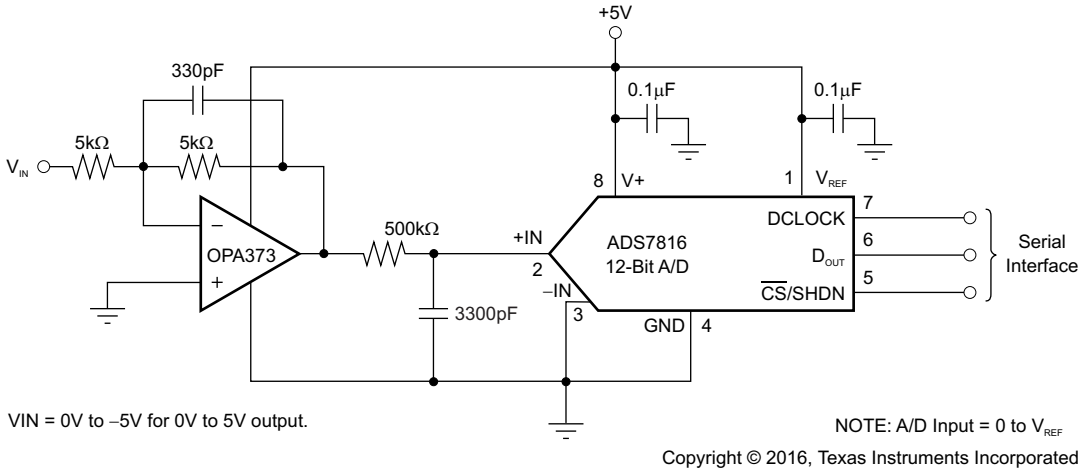


Figure 31. The OPA373 in Inverting Configuration Driving the ADS7816

Figure 32 shows the OPA373 configured as a three-pole, Sallen-Key, Butterworth low-pass filter.

System Examples (continued)

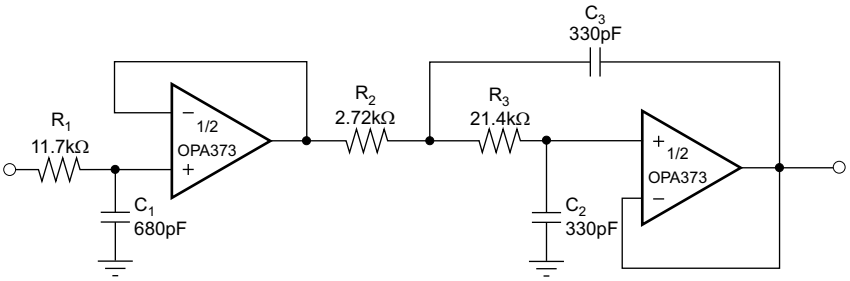


Figure 32. Three-Pole, Sallen-Key, Butterworth Low-Pass Filter

10 Power Supply Recommendations

The OPAx373 and OPAx374 are specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

The leadframe die pad must be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements.

Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat sink area on the PCB. Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests.

Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

11.1.1 VSON Package

The OPA2373 is available in a 10-pin VSON package, which is a VQFN package with lead contacts on only two sides of the bottom of the package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad. VSON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SOIC and VSSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The VSON package can be easily mounted using standard PCP assembly techniques. See *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages*, both available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package must be connected to V−.

11.2 Layout Example

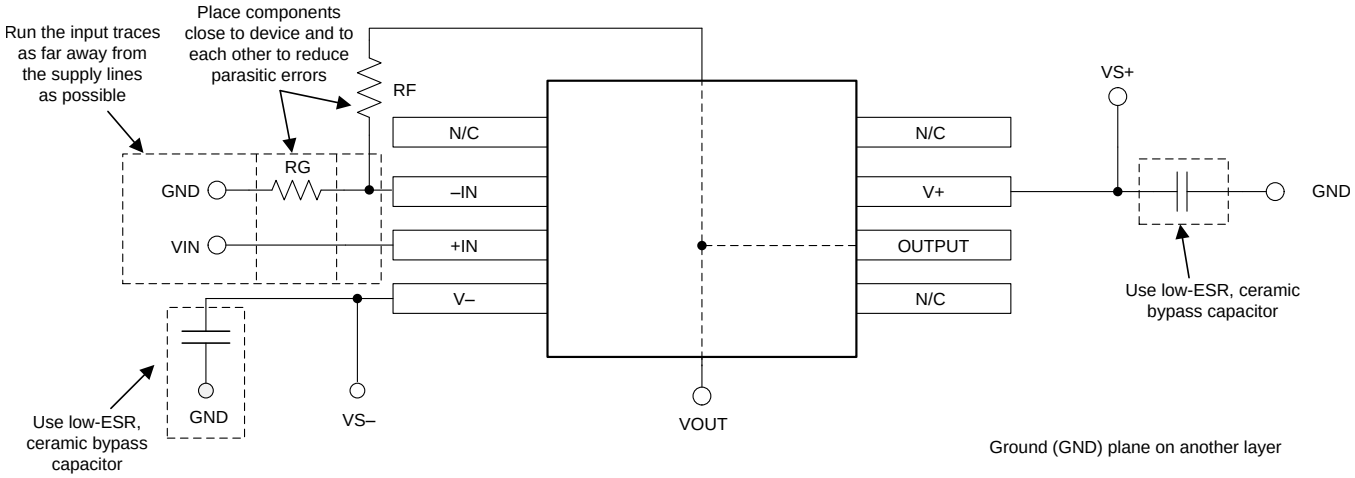


Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (8-pin SOIC), PW (8-pin TSSOP), DGK (8-pin MSOP), DBV (6-pin SOT-23, 5-pin SOT23, and 3-pin SOT-23), DCK (6-pin SC-70 and 5-pin SC-70), and DRL (6-pin SOT-563). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

12.1.1.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

The following documents are relevant to using the OPAx373, OPAx374, and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- *36-V, 1-kW Brushless DC Motor Drive With Stall Current Limit of < 1-µs Response Time Reference Design* (TIDU852)
- *OPA373 EMI Immunity Performance* (SBOZ009)
- *AB-045 Op Amp Performance Analysis* (SBOA054)
- *AB-067 Single-Supply Operation of Operational Amplifiers* (SBOA059)
- *AB-105 Tuning in Amplifiers* (SBOA067)
- *QFN/SON PCB Attachment* (SLUA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)

12.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA373	Click here	Click here	Click here	Click here	Click here
OPA2373	Click here	Click here	Click here	Click here	Click here
OPA374	Click here	Click here	Click here	Click here	Click here
OPA2374	Click here	Click here	Click here	Click here	Click here
OPA4374	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2373AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	AYO	Samples
OPA2373AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	AYO	Samples
OPA2373AIDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2373AIDRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2373AIDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCEQ	Samples
OPA2374AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A	Samples
OPA2374AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ATP	Samples
OPA2374AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2374A	Samples
OPA2374AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2374A	Samples
OPA2374AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2374A	Samples
OPA373AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA373AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A75	Samples
OPA373AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA373AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 373A	Samples
OPA374AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A76	Samples
OPA374AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA374AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 374A	Samples
OPA4374AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4374A	Samples
OPA4374AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples
OPA4374AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4374AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples
OPA4374AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4374A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

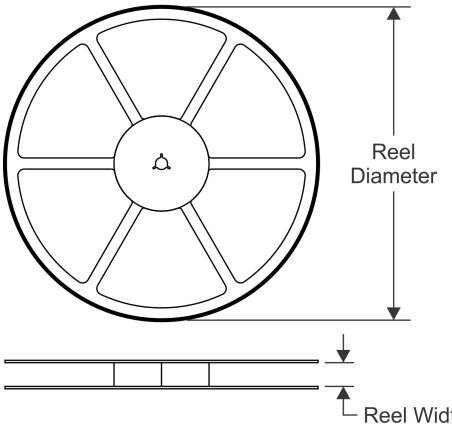
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

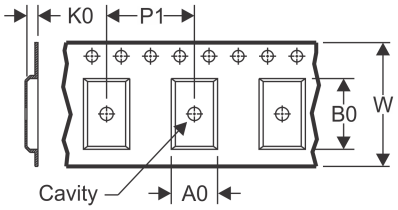
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

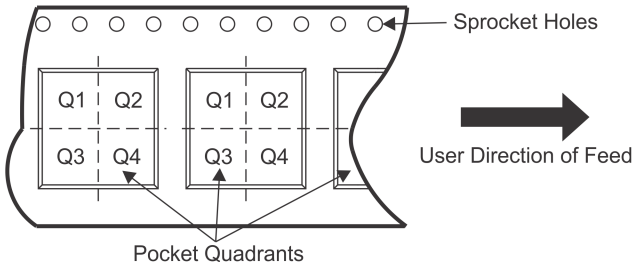


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

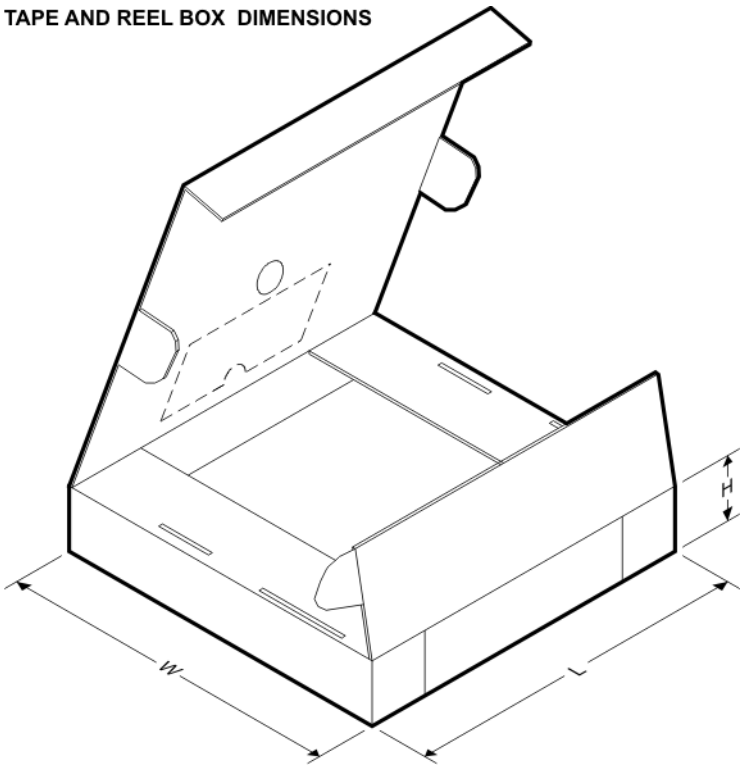
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2373AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2373AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2373AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2373AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA373AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA374AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA374AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4374AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4374AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4374AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

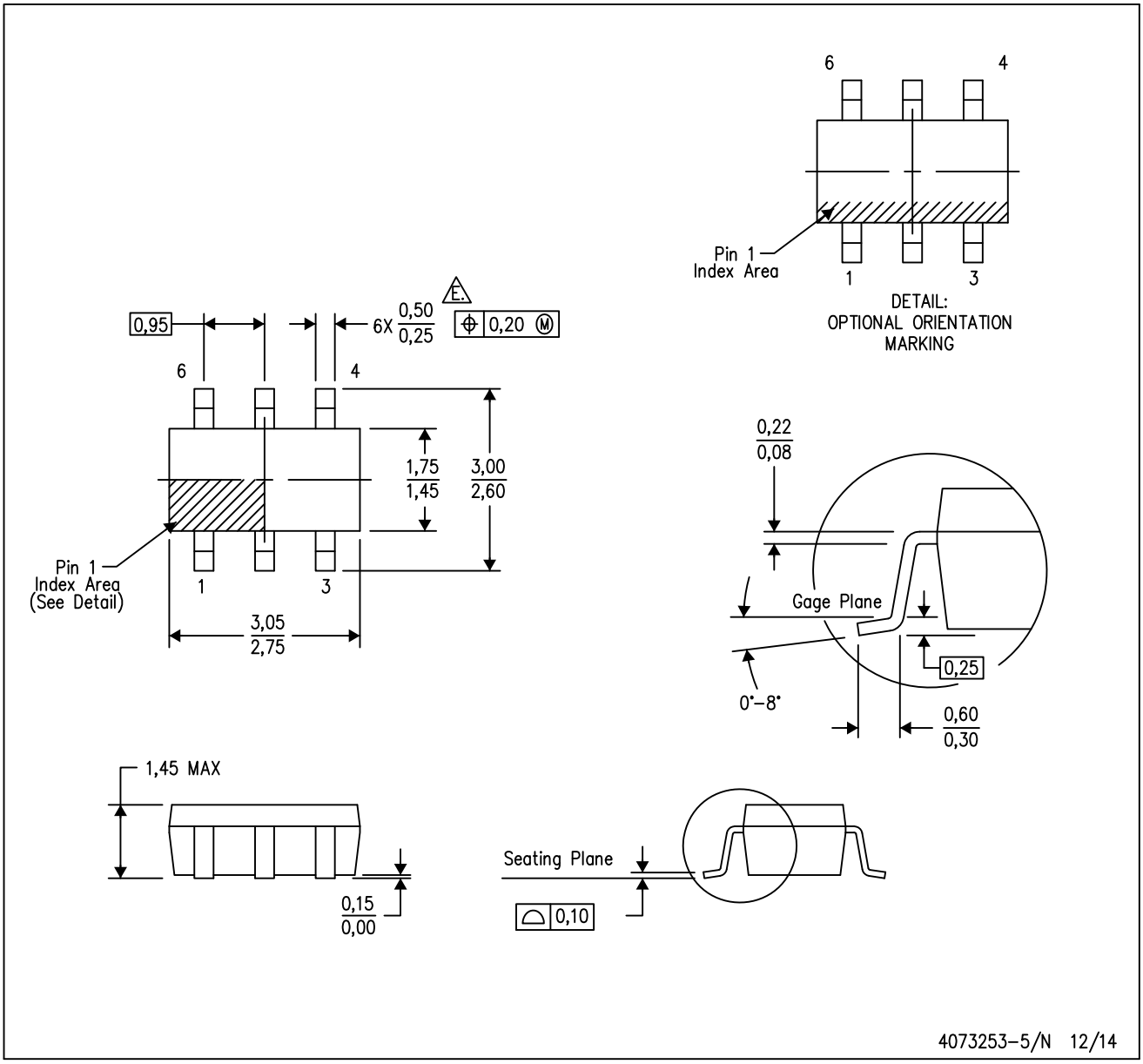
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

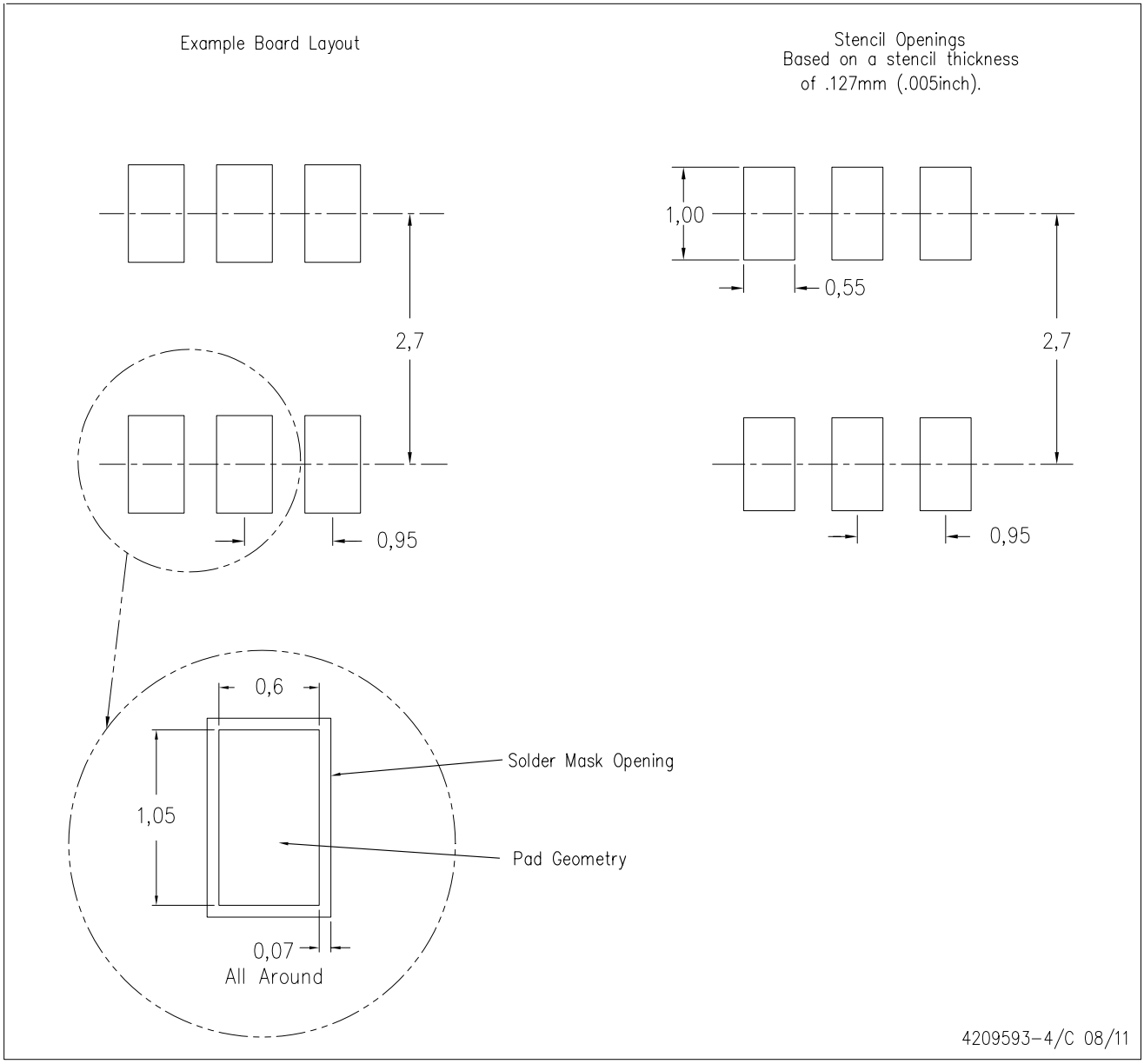
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2373AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2373AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2373AIDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
OPA2373AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0
OPA2374AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA373AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA374AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA374AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA374AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4374AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4374AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4374AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



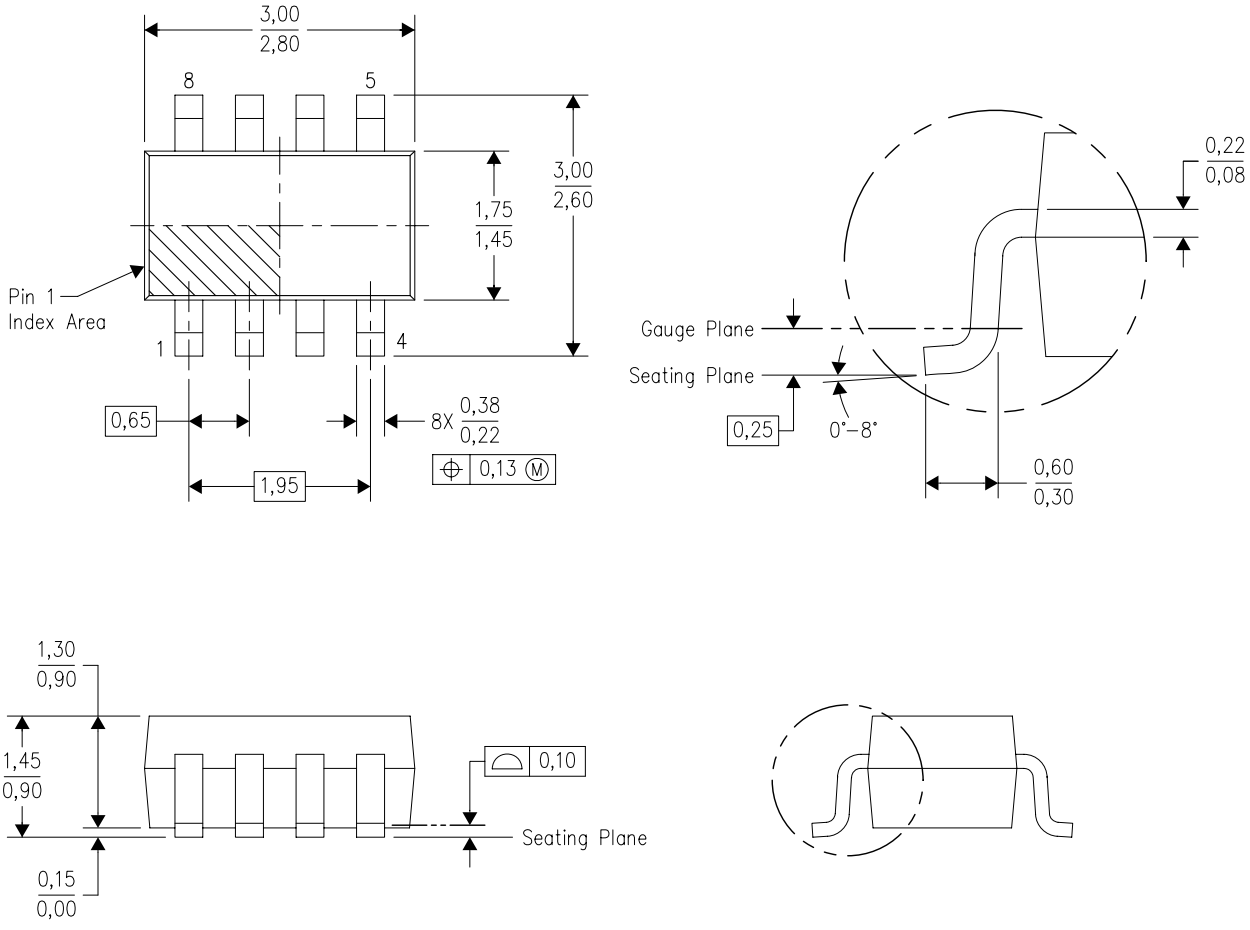
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



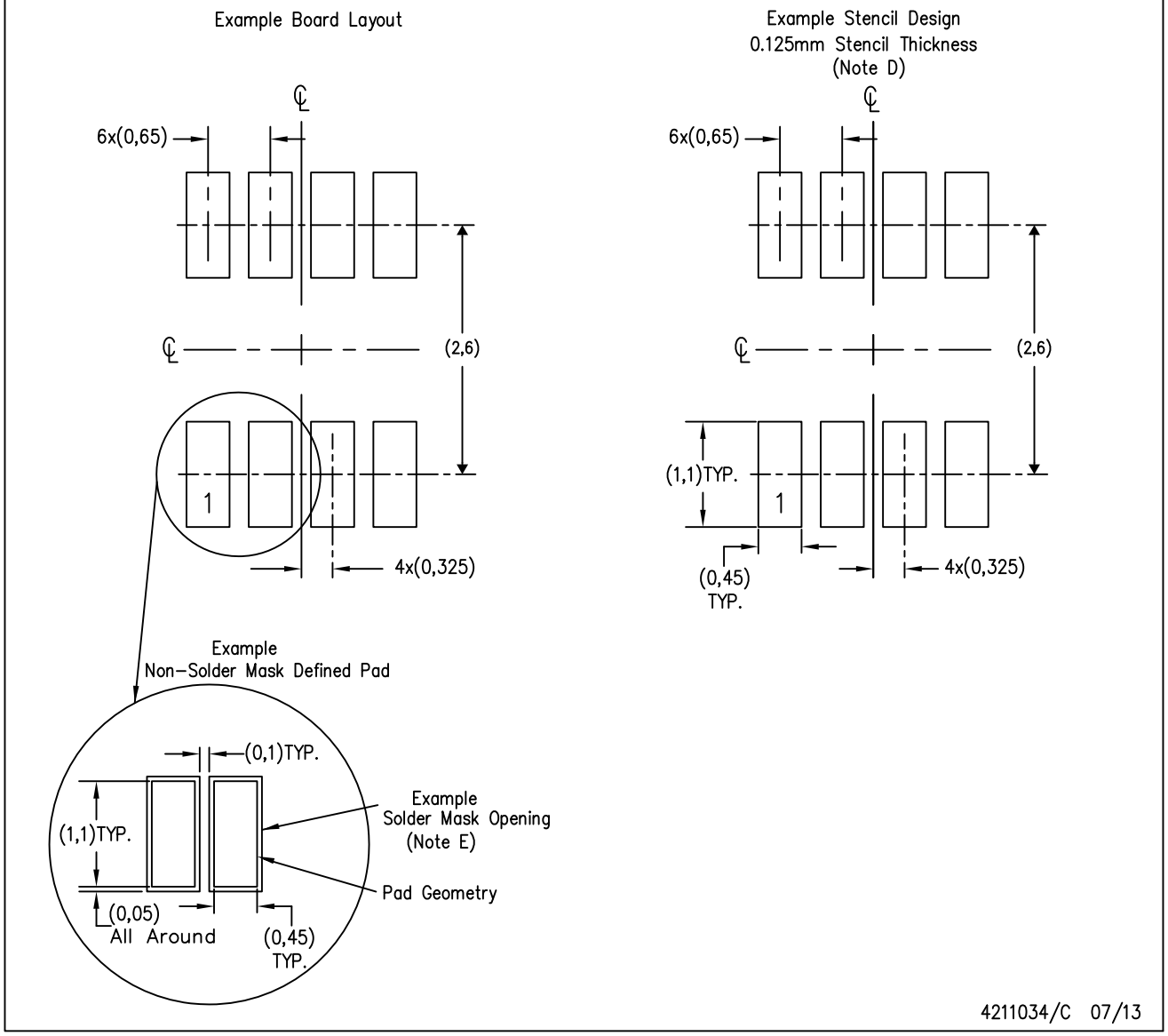
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



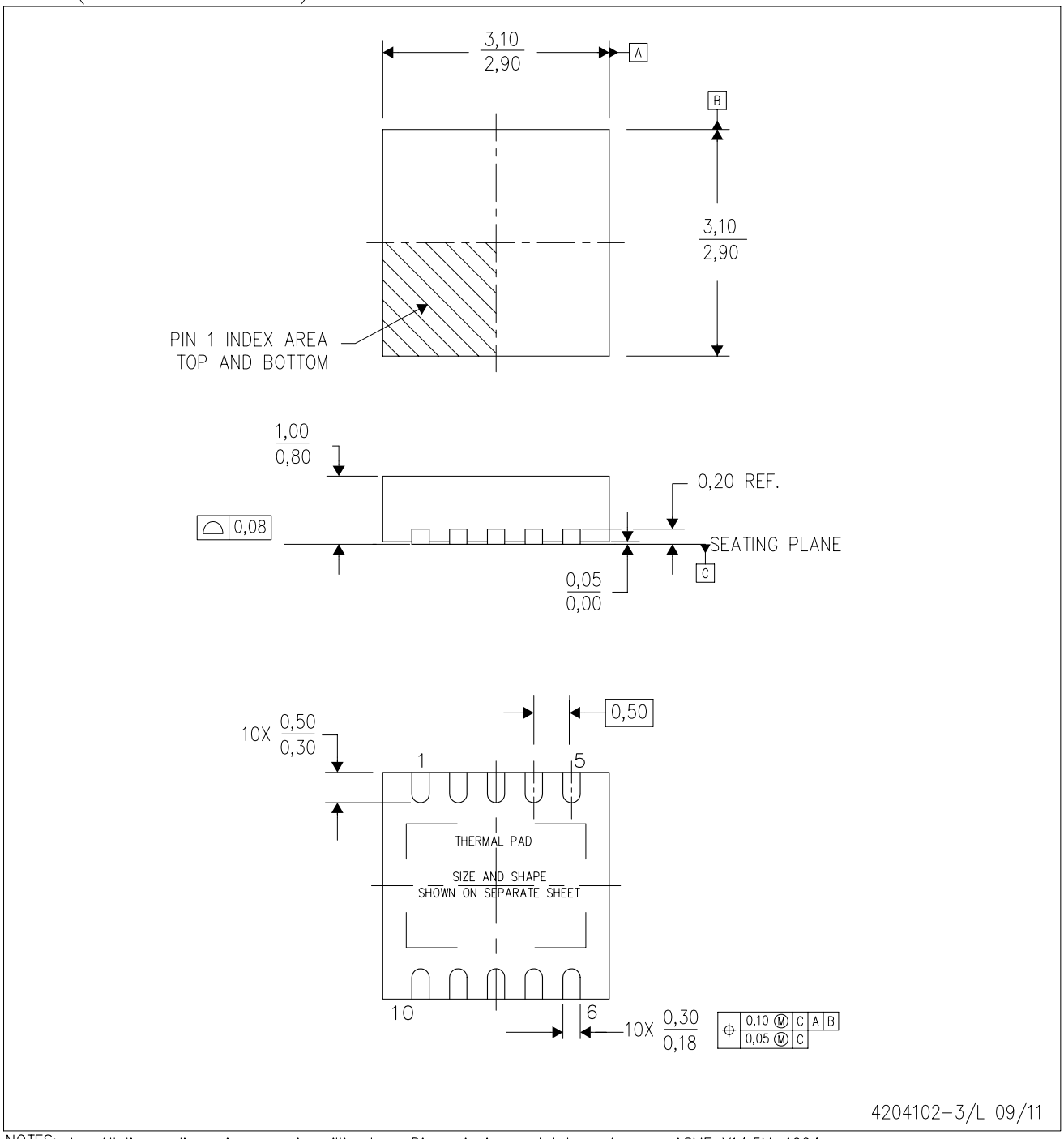
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

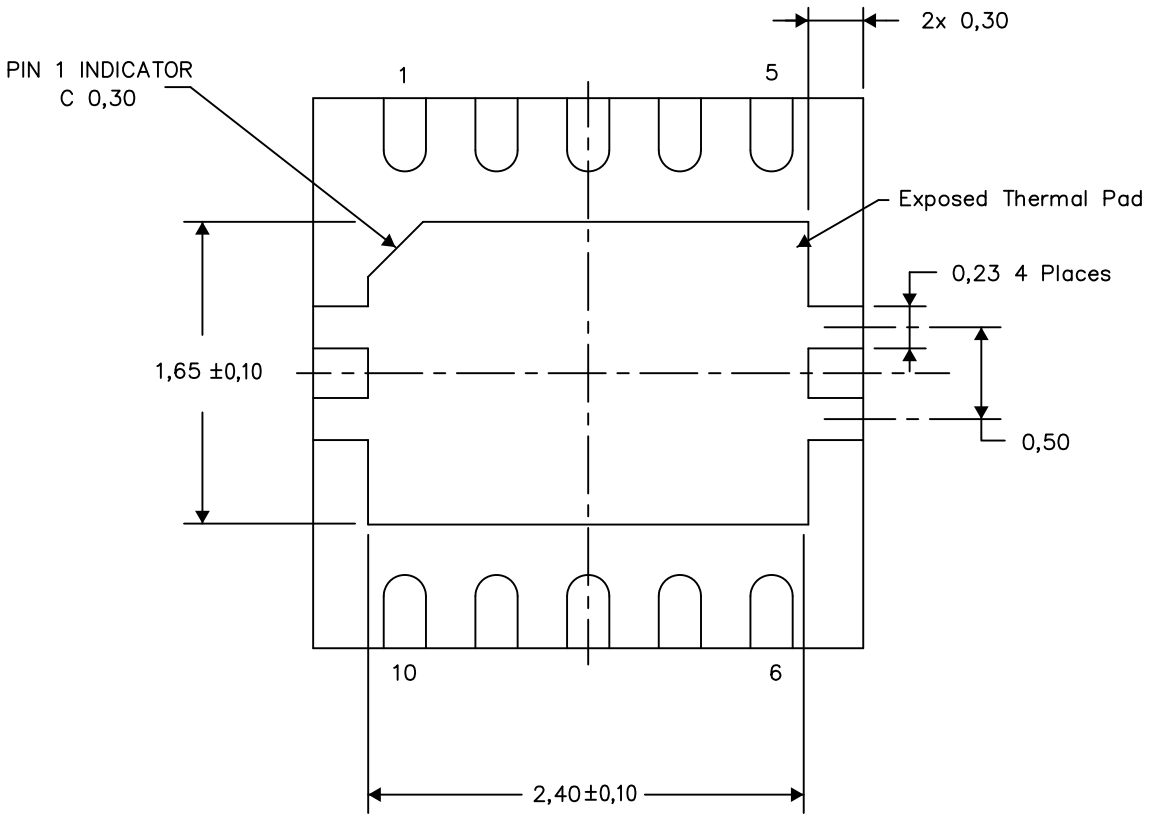
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



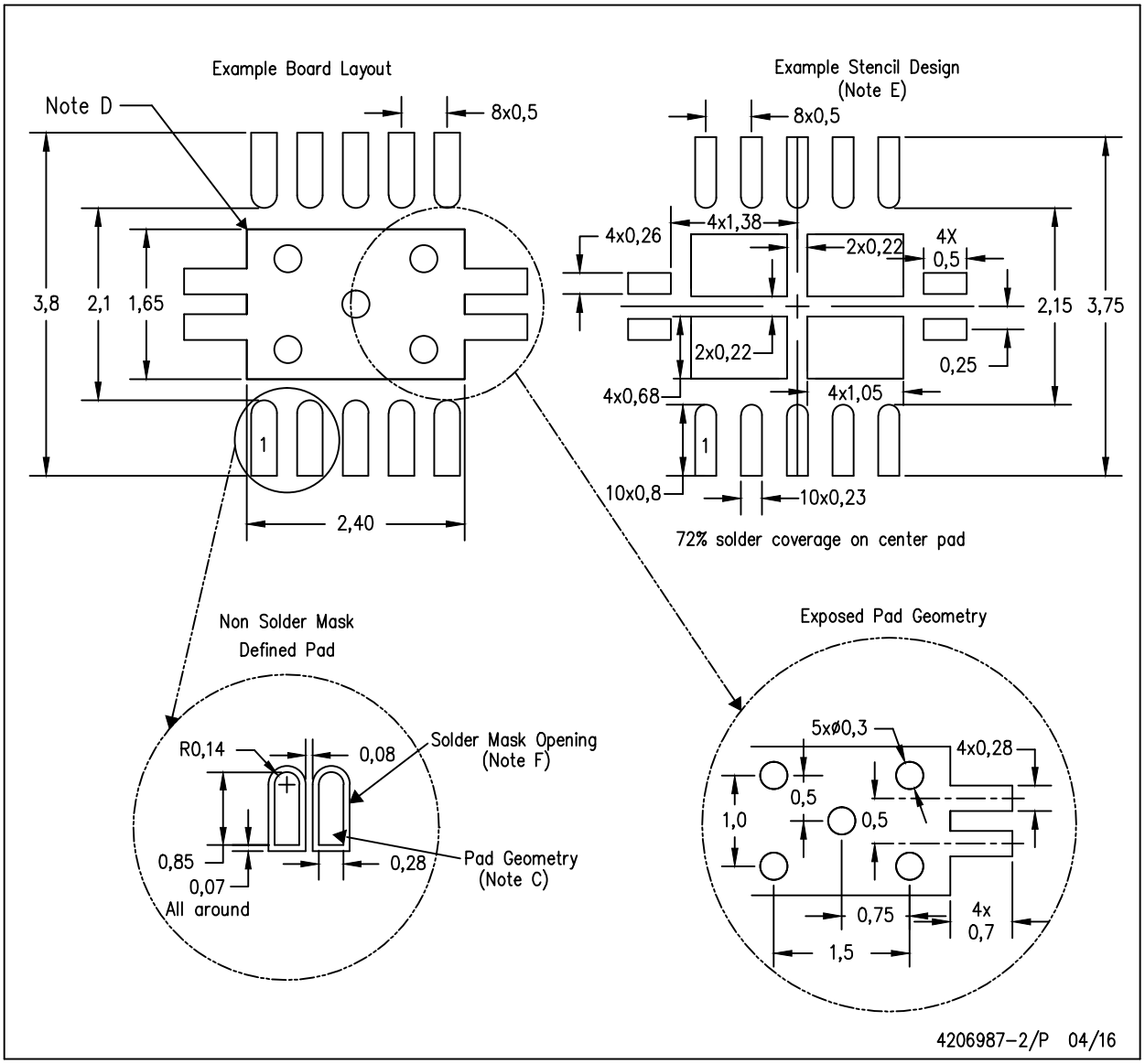
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

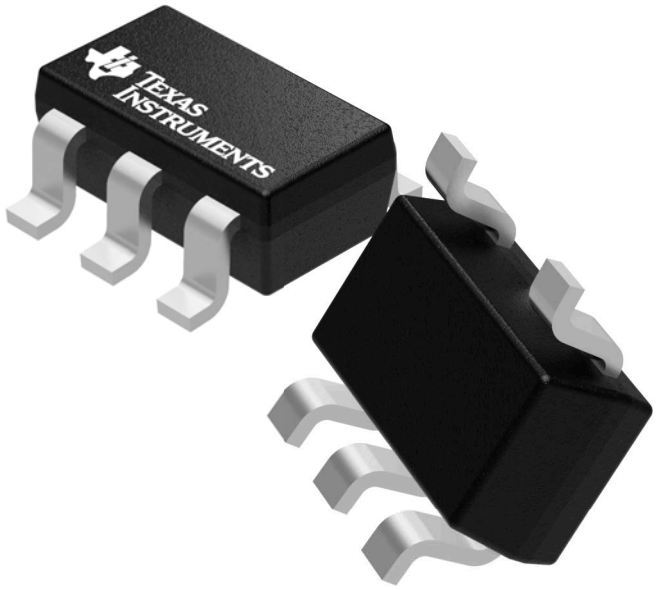
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



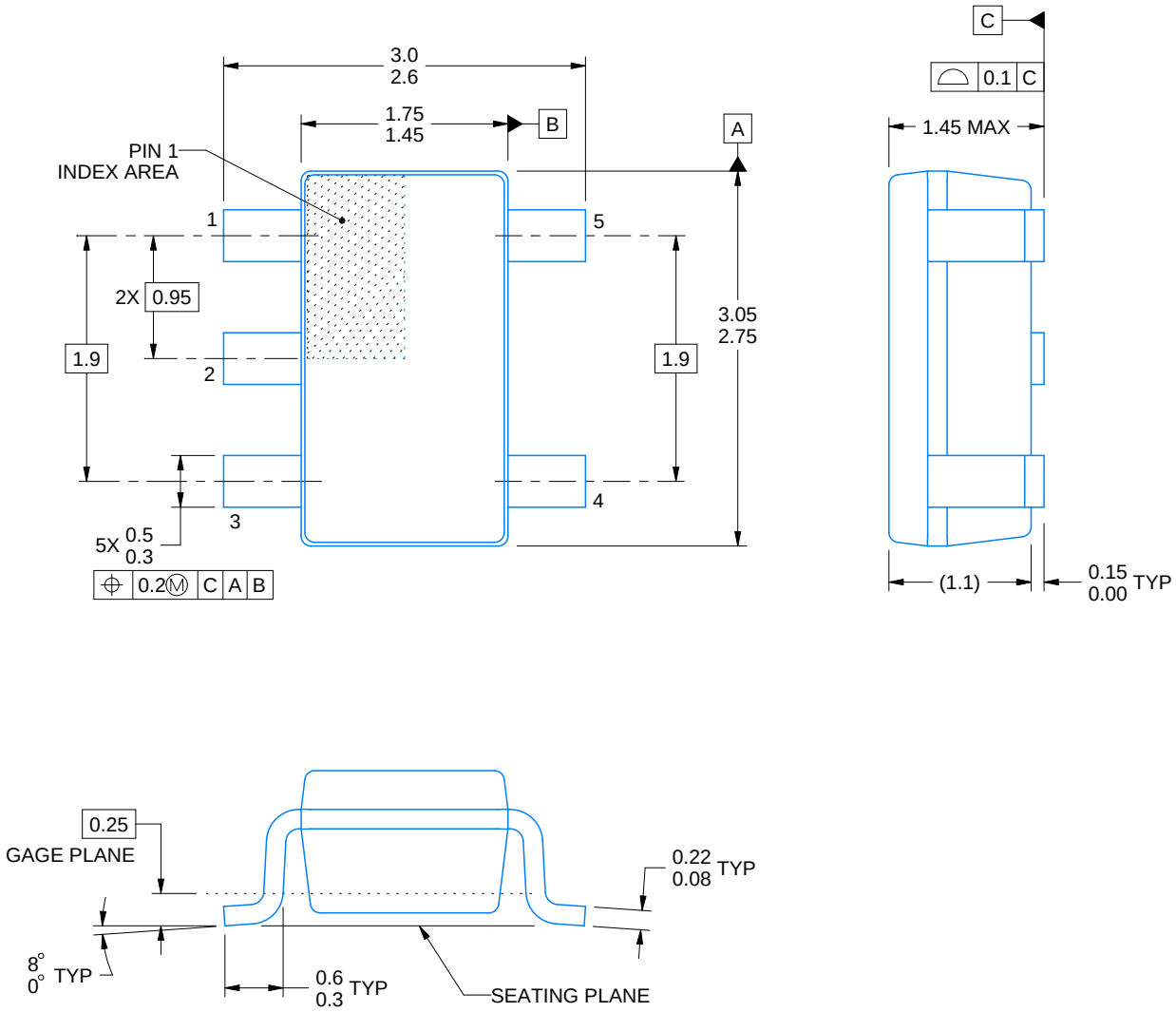
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

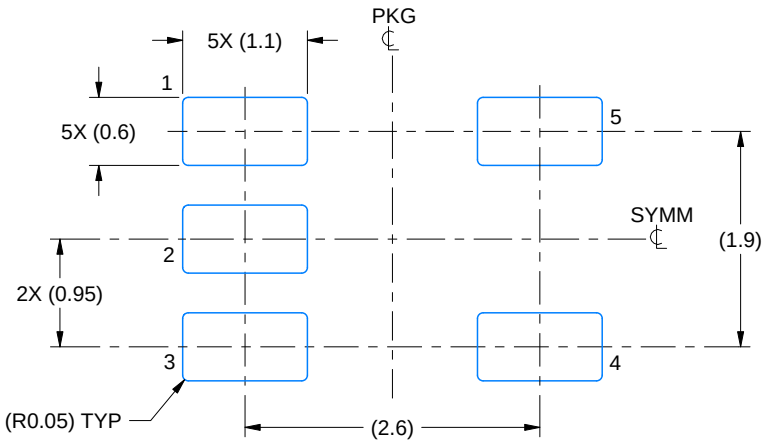
SMALL OUTLINE TRANSISTOR



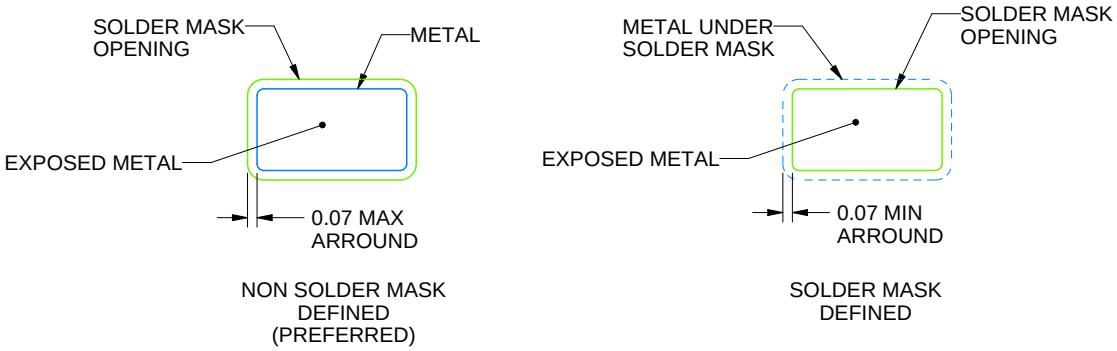
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

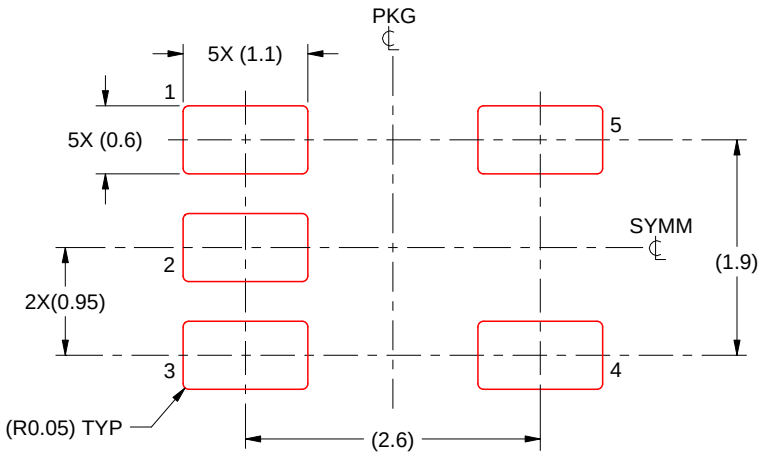


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



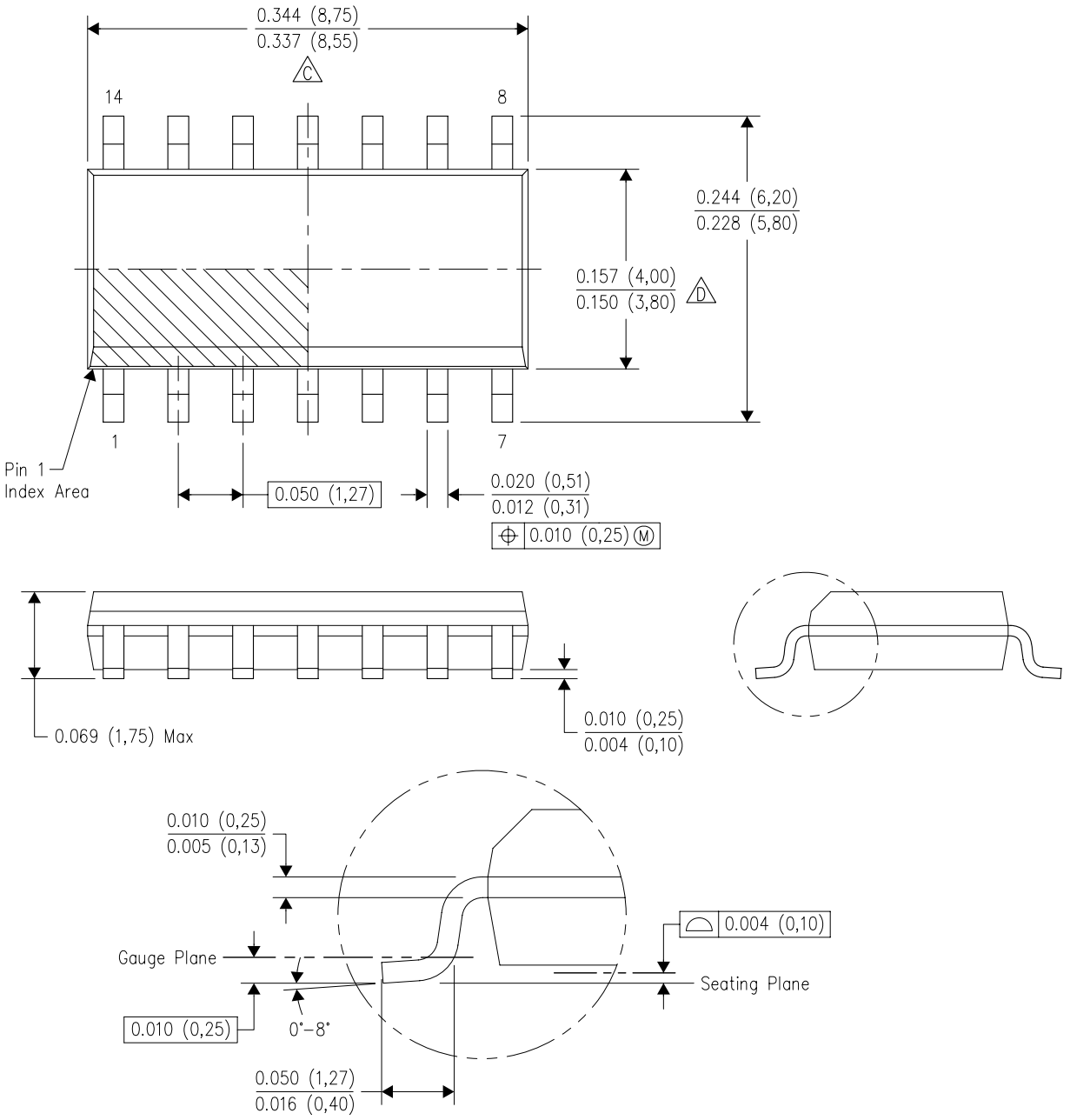
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

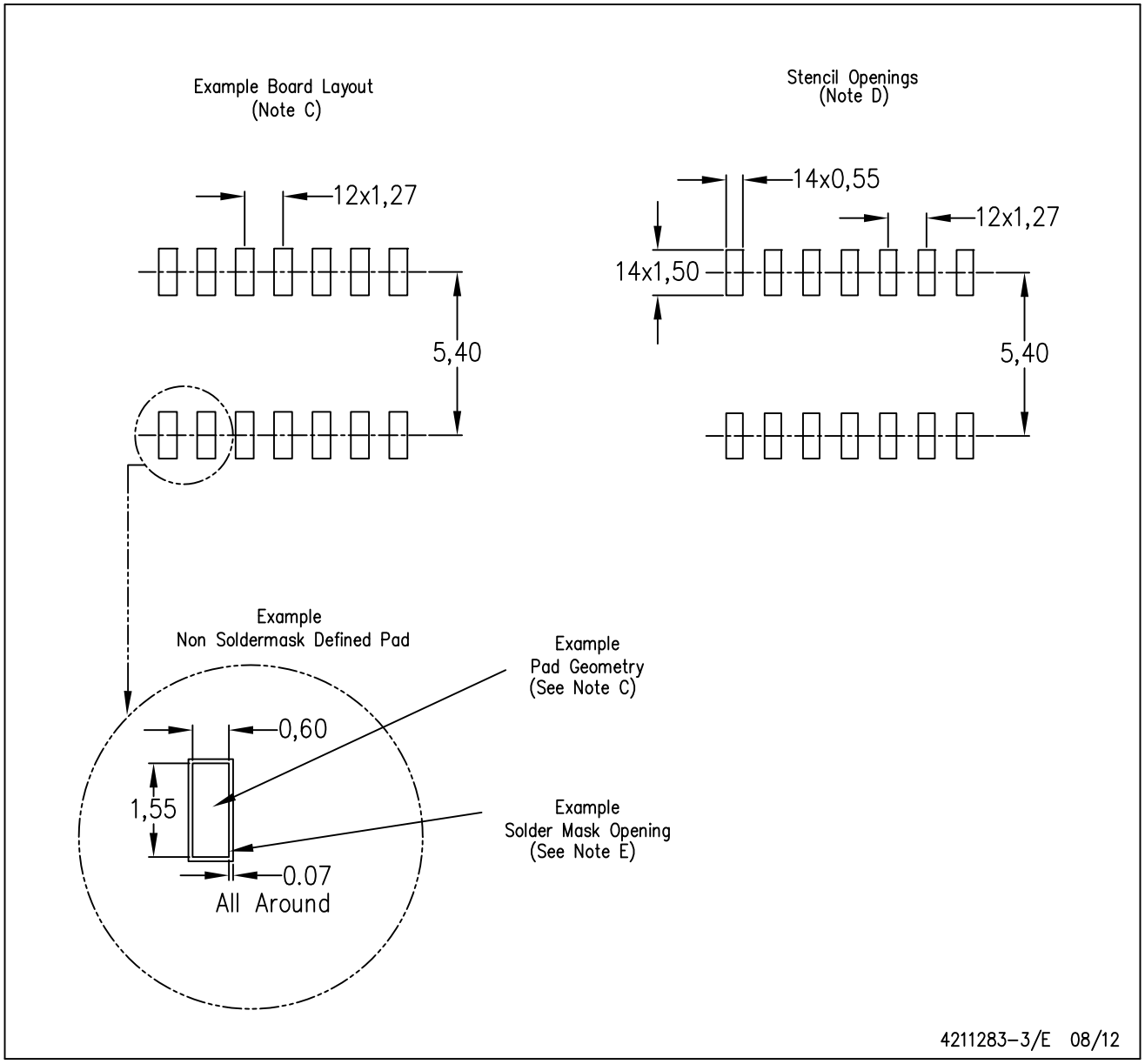
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

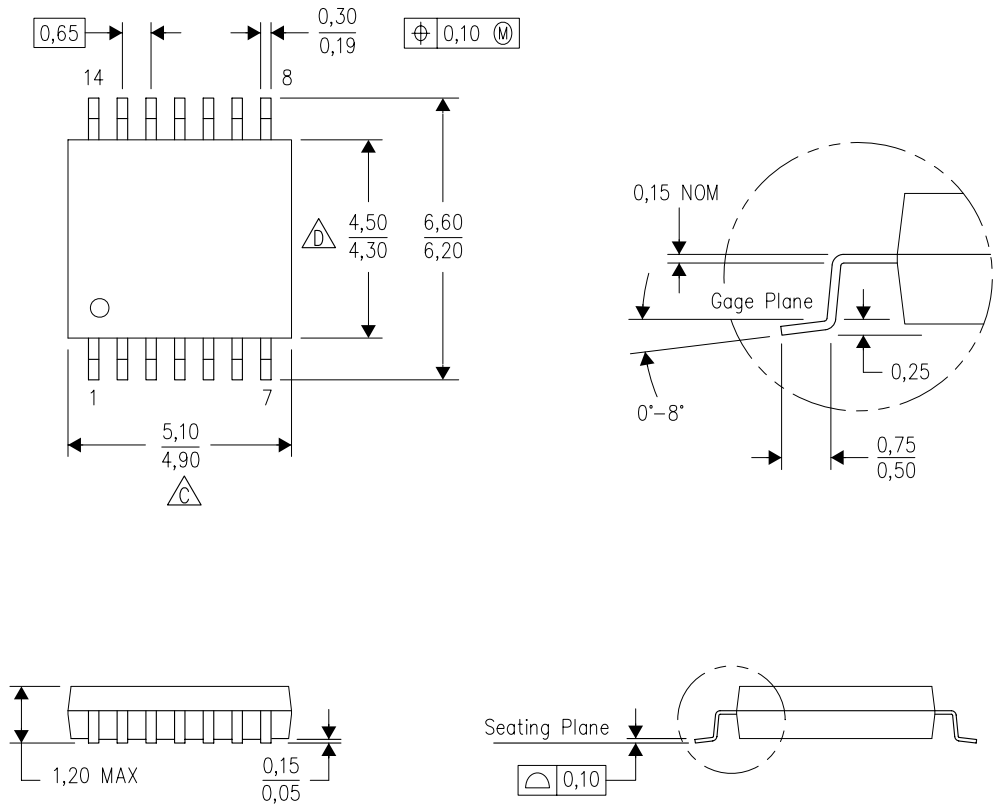
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

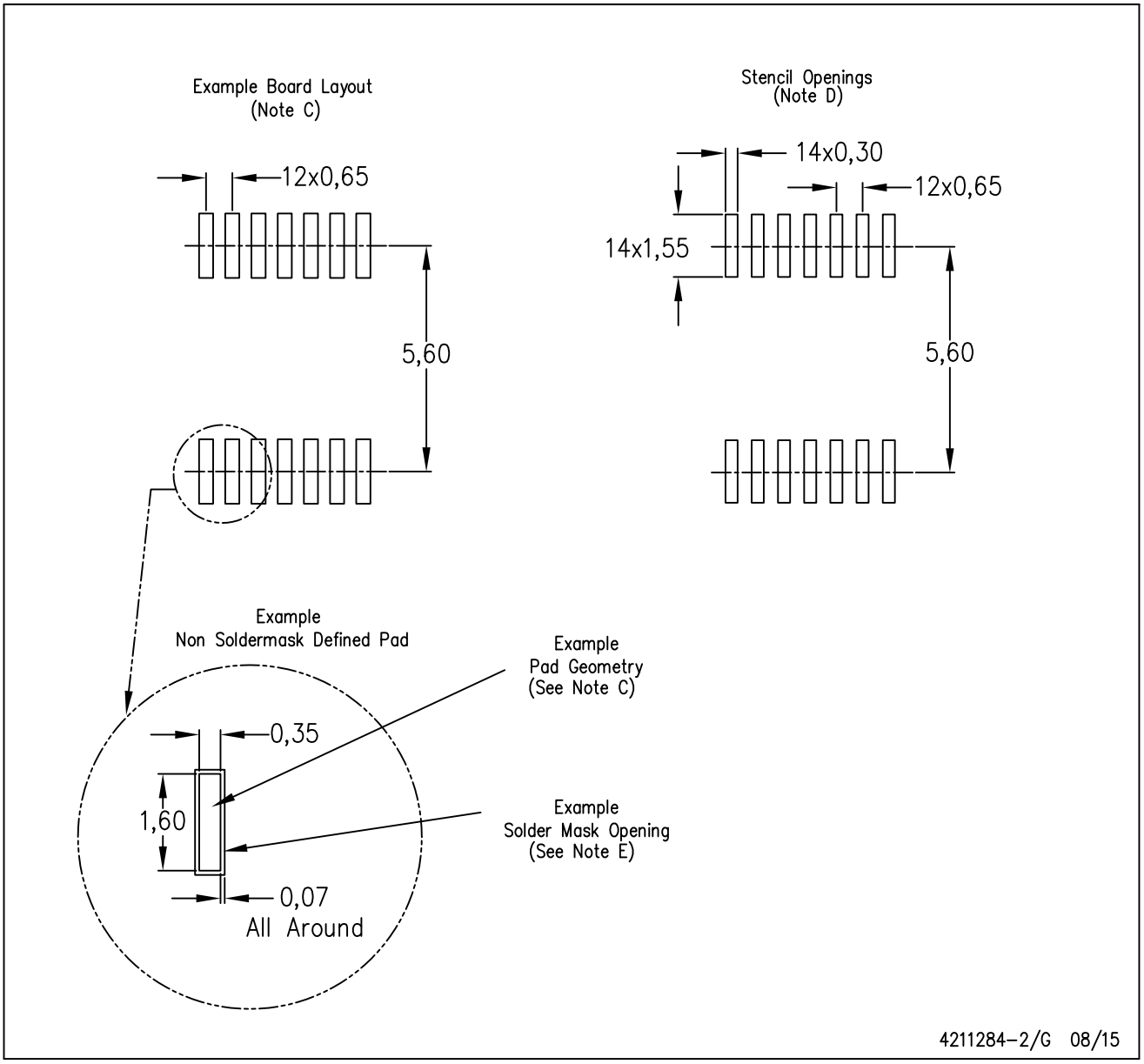
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

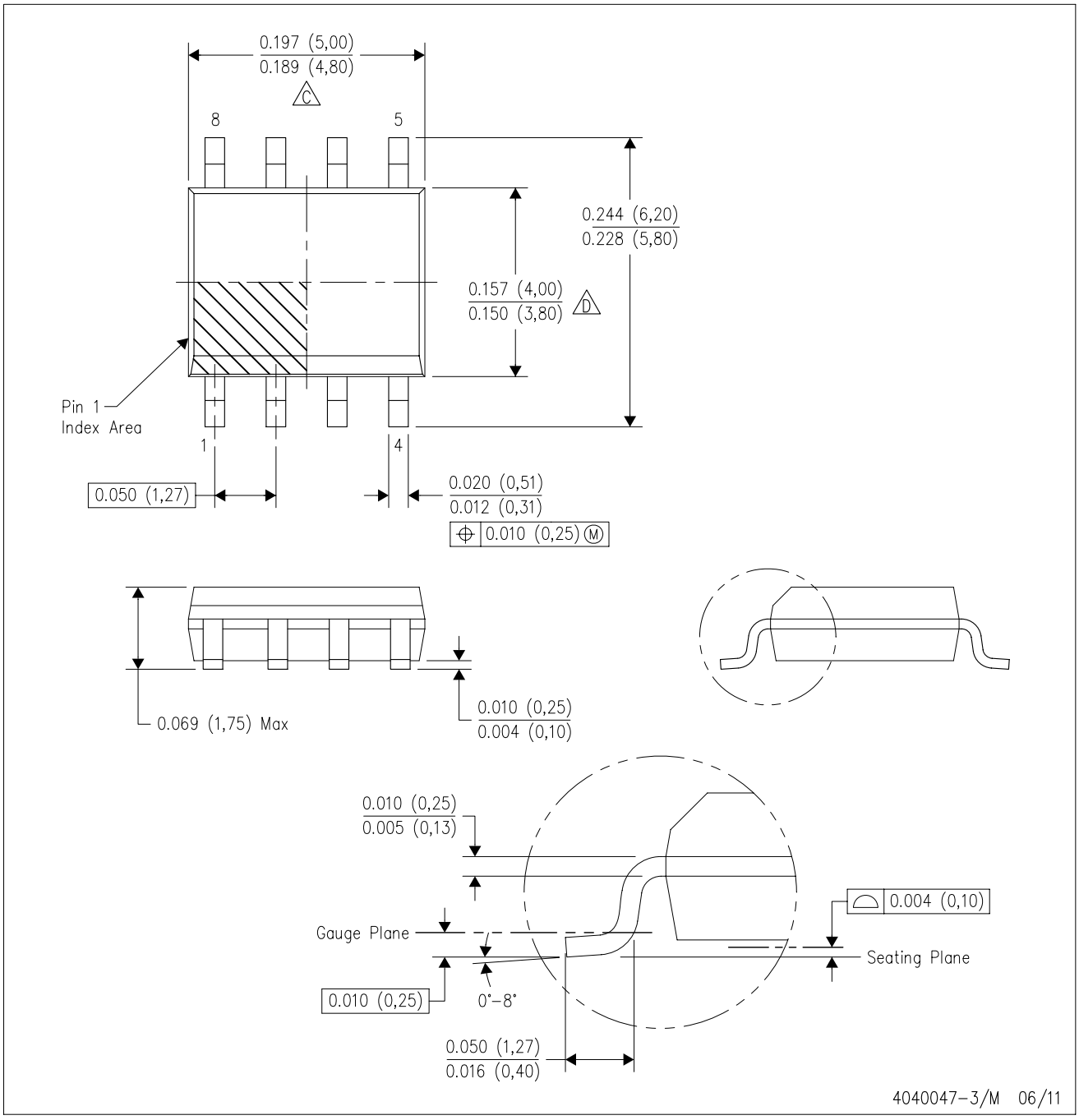
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



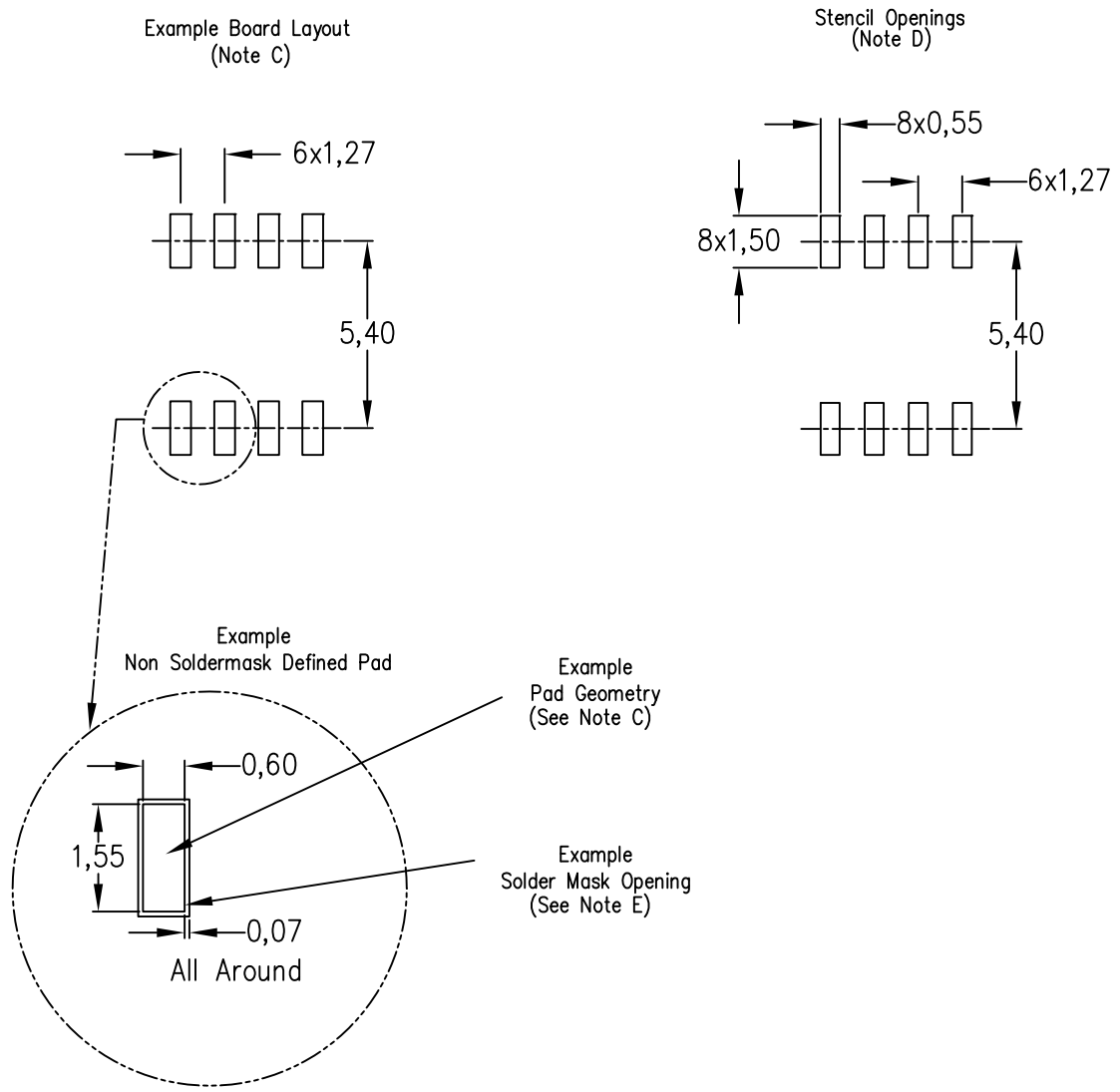
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



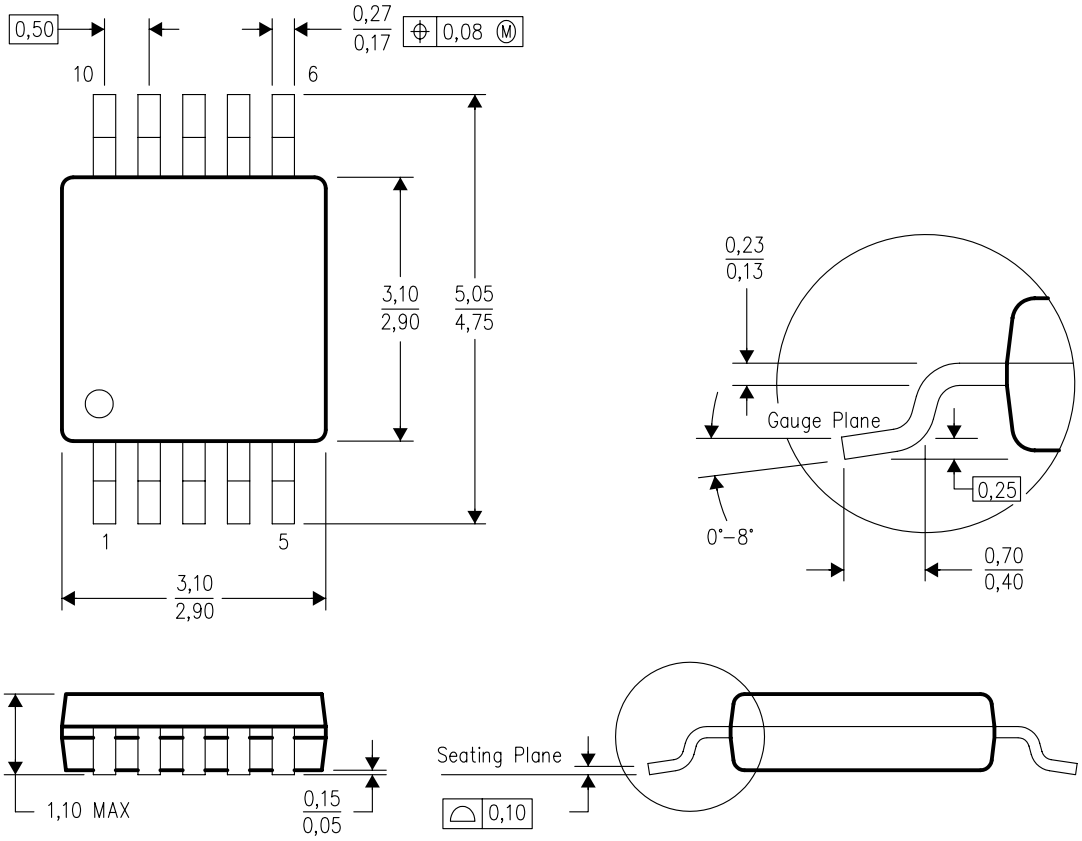
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

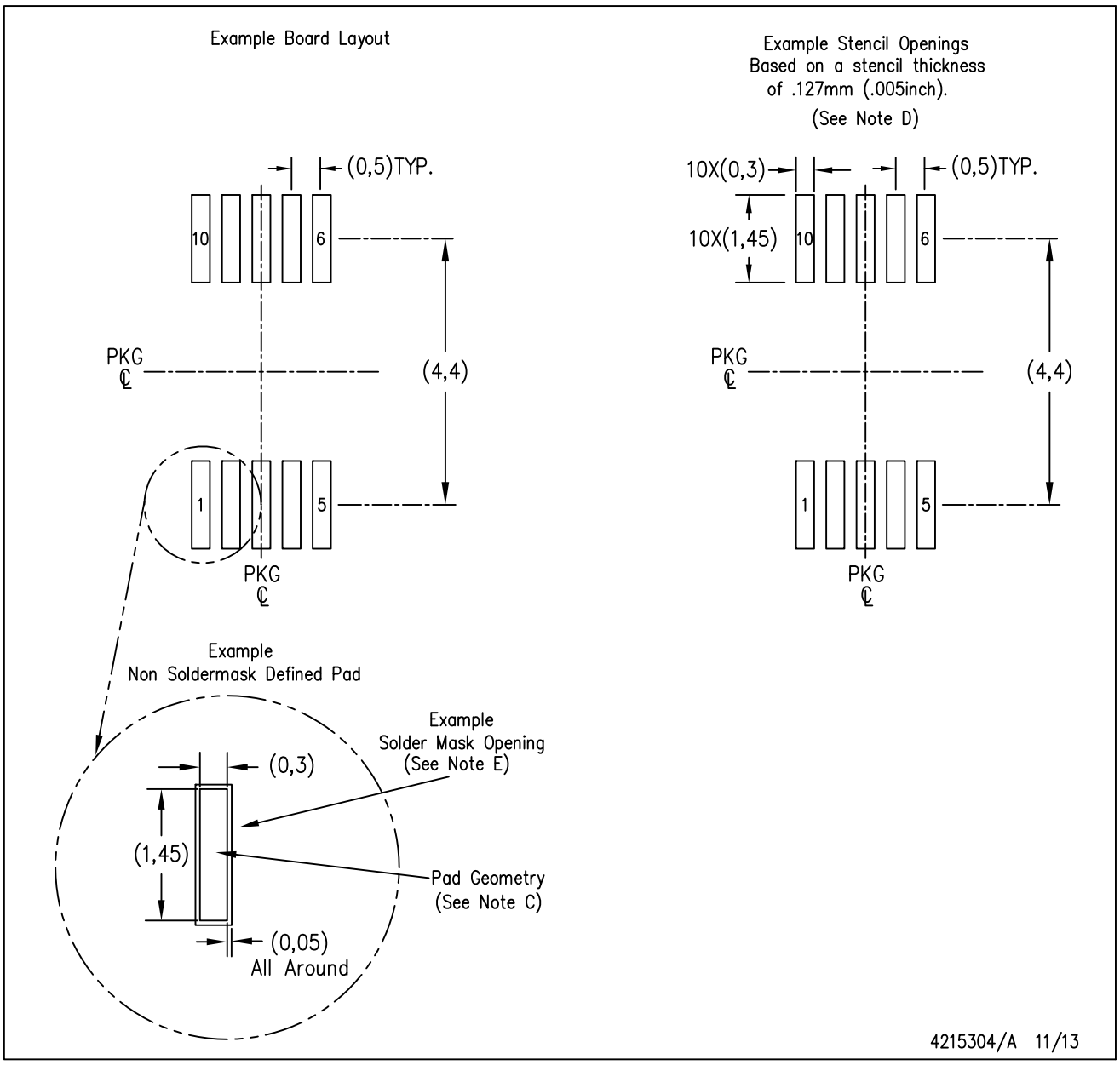
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265