PCM1794A 24-Bit, 192-kHz Sampling, Advanced Segment, Audio Stereo Digital-to-Analog Converter

1 Features

- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range:
    - 132 dB (9 V RMS, Mono)
    - 129 dB (4.5 V RMS, Stereo)
    - 127 dB (2 V RMS, Stereo)
  - THD+N: 0.0004%
- Differential Current Output: 7.8 mA p-p
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –130 dB
  - Pass-Band Ripple: ±0.00001 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect
- Accepts 16-Bit and 24-Bit Audio Data
- PCM Data Formats: Standard, I^2S, and Left-Justified
- Optional Interface Available to External Digital Filter or DSP
- Digital De-Emphasis
- Digital Filter Rolloff: Sharp or Slow
- Soft Mute
- Zero Flag
- Dual-Supply Operation: 5-V Analog, 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small 28-Pin SSOP Package

2 Applications

- A/V Receivers
- DVD Players
- Musical Instruments
- Car Audio Systems
- Other Applications Requiring 24-Bit Audio

3 Description

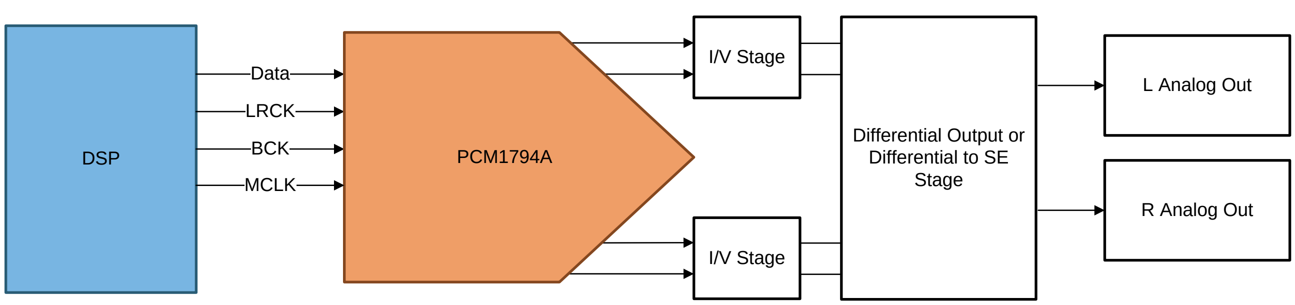
The PCM1794A device is a monolithic, CMOS-integrated circuit that includes stereo digital-to-analog converters (DACs) and support circuitry in a small 28-pin SSOP package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1794A device provides balanced current outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1794A	SSOP (28)	10.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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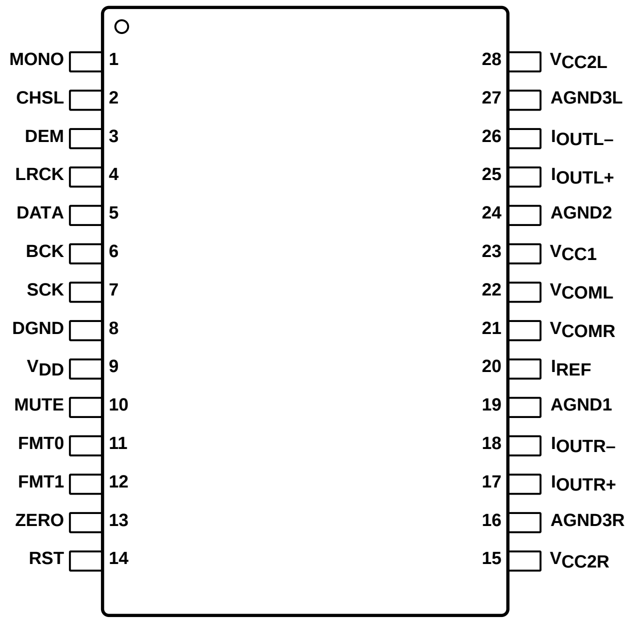
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2006) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

DB Package
28-Pin SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MONO	I	Monaural mode enable[1]
2	CHSL	I	L-channel, R-channel select[1]
3	DEM	I	De-emphasis enable[1]
4	LRCK	I	Left and right clock (f_S) input[1]
5	DATA	I	Serial audio data input[1]
6	BCK	I	Bit clock input[1]
7	SCK	I	System clock input[1]
8	DGND	—	Digital ground
9	V_{DD}	—	Digital power supply, 3.3 V
10	MUTE	I	Mute control[1]
11	FMT0	I	Audio data format select[1]
12	FMT1	I	Audio data format select[1]
13	ZERO	O	Zero flag
14	$\overline{\text{RST}}$	I	Reset[1]
15	V_{CC}2R	—	Analog power supply (R-channel DAC), 5 V
16	AGND3R	—	Analog ground (R-channel DAC)
17	I_{OUT}R+	O	R-channel analog current output +
18	I_{OUT}R–	O	R-channel analog current output –
19	AGND1	—	Analog ground (internal bias)
20	I_{REF}	—	Output current reference bias pin
21	V_{COM}R	—	R-channel internal bias decoupling pin
22	V_{COM}L	—	L-channel internal bias decoupling pin

(1) Schmitt-trigger input, 5-V tolerant.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
23	$V_{CC}1$	—	Analog power supply, 5 V
24	AGND2	—	Analog ground (internal bias)
25	$I_{OUT}L+$	O	L-channel analog current output +
26	$I_{OUT}L–$	O	L-channel analog current output –
27	AGND3L	—	Analog ground (L-channel DAC)
28	$V_{CC}2L$	—	Analog power supply (L-channel DAC), 5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	–0.3	6.5	V
	V_{DD}	–0.3	4	
Supply voltage differences: $V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$			±0.1	V
Ground voltage differences: AGND1, AGND2, AGND3L, AGND3R, DGND			±0.1	V
Digital input voltage	LRCK, DATA, BCK, SCK, FMT1, FMT0, MONO, CHSL, DEM, MUTE, $\overline{RST}$	–0.3	6.5	V
	ZERO	–0.3	(V_{DD} + 0.3 V) < 4	
Analog input voltage		–0.3	(V_{CC} + 0.3 V) < 6.5	V
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature			150	°C
Lead temperature (soldering, 5 s)			260	°C
Package temperature (IR reflow, peak)			250	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	V_{DD}	3	3.3	3.6	VDC
		$V_{CC}1$ $V_{CC}2L$ $V_{CC}2R$	4.75	5	5.25	VDC
T_J	Operation temperature		—25		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		PCM1794A DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA FORMAT						
f_S	Sampling frequency		10		200	kHz
	System clock frequency		128, 192, 256, 384, 512, 768			f_S
DIGITAL INPUT/OUTPUT						
	Logic family		TTL compatible			
V_{IH}	Input logic level high		2			VDC
V_{IL}	Input logic level low				0.8	VDC
I_{IH}	Input logic current high	V_{IN} = V_{DD}			10	µA
I_{IL}	Input logic current low	V_{IN} = 0 V			–10	µA
V_{OH}	Output logic level high	I_{OH} = –2 mA	2.4			VDC
V_{OL}	Output logic level low	I_{OL} = 2 mA			0.4	VDC
DYNAMIC PERFORMANCE (2-V RMS OUTPUT)(1)(2)						
	THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%	0.0008%	
		f_S = 96 kHz		0.0008%		
		f_S = 192 kHz		0.0015%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
		EIAJ, A-weighted, f_S = 96 kHz		127		
		EIAJ, A-weighted, f_S = 192 kHz		127		

(1) Filter condition:
(a) THD+N: 20-Hz HPF, 20-kHz apogee LPF
(b) Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
(c) Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
(d) Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
(e) Analog performance specifications are measured using the System Two Cascade audio measurement system by Audio Precision™ in the averaging mode.
(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 25.

Electrical Characteristics (continued)

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
	EIAJ, A-weighted, f_S = 96 kHz		127		
	EIAJ, A-weighted, f_S = 192 kHz		127		
Channel separation	f_S = 44.1 kHz	120	123		dB
	f_S = 96 kHz		122		
	f_S = 192 kHz		120		
Level linearity error	V_{OUT} = –120 dB		±1		dB
DYNAMIC PERFORMANCE (4.5-V RMS Output) (1) (3)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
	EIAJ, A-weighted, f_S = 96 kHz		129		
	EIAJ, A-weighted, f_S = 192 kHz		129		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
	EIAJ, A-weighted, f_S = 96 kHz		129		
	EIAJ, A-weighted, f_S = 192 kHz		129		
Channel separation	f_S = 44.1 kHz		124		dB
	f_S = 96 kHz		123		
	f_S = 192 kHz		121		
DYNAMIC PERFORMANCE (MONO MODE) (1) (3)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		
ANALOG OUTPUT					
Gain error		–6	±2	6	% of FSR
Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
Bipolar zero error	At BPZ	–2	±0.5	2	% of FSR
Output current	Full scale (0 dB)		7.8		mA p-p
Center current	At BPZ		–6.2		mA
DIGITAL FILTER PERFORMANCE					
De-emphasis error				±0.004	dB
FILTER CHARACTERISTICS-1: SHARP ROLLOFF					
Pass band	±0.00001 dB			0.454 f_S	
	–3 dB			0.49 f_S	
Stop band		0.546 f_S			
Pass-band ripple				±0.00001	dB
Stop-band attenuation	Stop band = 0.546 f_S	–130			dB
Delay time			55/f_S		s
FILTER CHARACTERISTICS-2: SLOW ROLLOFF					
Pass band	±0.04 dB			0.254 f_S	
	–3 dB			0.46 f_S	

(3) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 26.

Electrical Characteristics (continued)

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Stop band		0.732 f_S			
	Pass-band ripple				±0.001	dB
	Stop-band attenuation	Stop band = 0.732 f_S	–100			dB
	Delay time			18 / f_S		s
POWER SUPPLY REQUIREMENTS						
I_{DD}	Digital supply current(4)	f_S = 44.1 kHz		12	15	mA
		f_S = 96 kHz		23		
		f_S = 192 kHz		45		
I_{CC}	Analog supply current(4)	f_S = 44.1 kHz		33	40	mA
		f_S = 96 kHz		35		
		f_S = 192 kHz		37		
	Power dissipation(4)	f_S = 44.1 kHz		205	250	mW
		f_S = 96 kHz		250		
		f_S = 192 kHz		335		

(4) Input is BPZ data.

6.6 Timing Requirements

		MIN	MAX	UNIT
SYSTEM CLOCK INPUT TIMING (see Figure 1)				
$t_{(SCY)}$	System-clock pulse-cycle time	13		ns
$t_{(SCKH)}$	System-clock pulse duration, HIGH	0.4 × $t_{(SCY)}$		ns
$t_{(SCKL)}$	System-clock pulse duration, LOW	0.4 × $t_{(SCY)}$		ns
EXTERNAL RESET TIMING (see Figure 2)				
$t_{(RST)}$	Reset pulse duration, LOW	20		ns
AUDIO INTERFACE TIMING (see Figure 3)				
$t_{(BCY)}$	BCK pulse-cycle time	70		ns
$t_{(BCL)}$	BCK pulse duration, LOW	30		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	30		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns
	LRCK clock duty	50% ± 2-bit clocks		

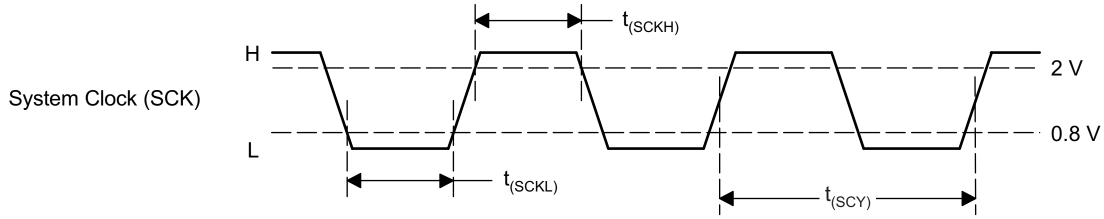


Figure 1. System Clock Input Timing

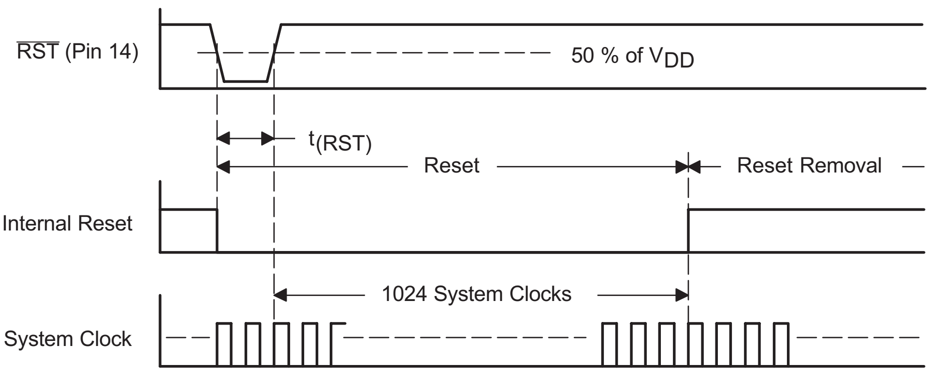


Figure 2. External Reset Timing

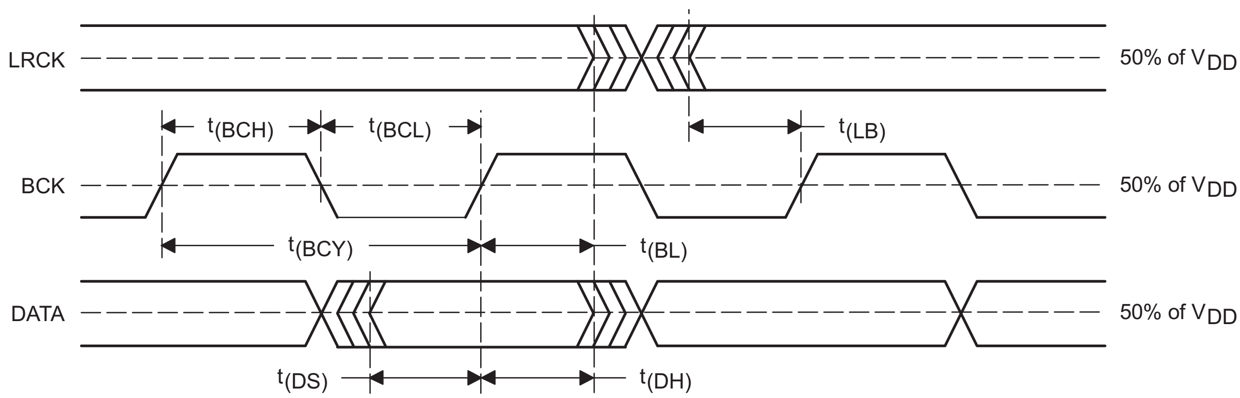


Figure 3. Timing of Audio Interface

6.7 Typical Characteristics

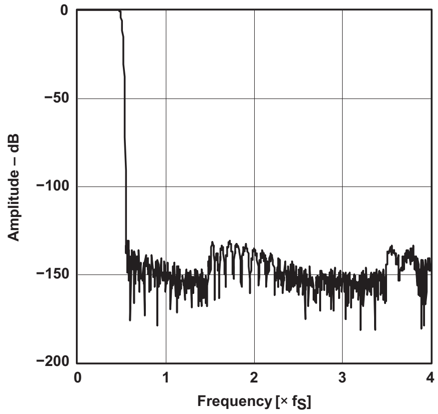


Figure 4. Amplitude vs Frequency Frequency Response, Sharp Rolloff

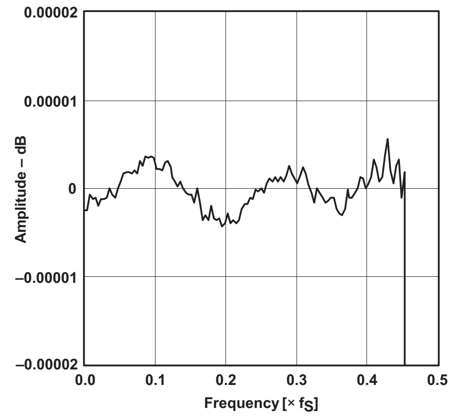


Figure 5. Amplitude vs Frequency Pass-Band Ripple, Sharp Rolloff

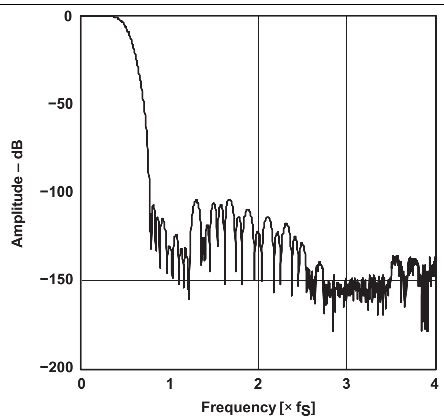


Figure 6. Amplitude vs Frequency Frequency Response, Slow Rolloff

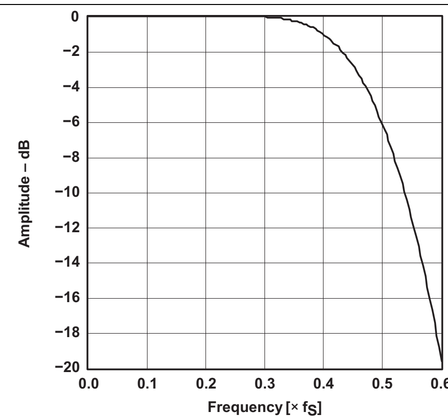
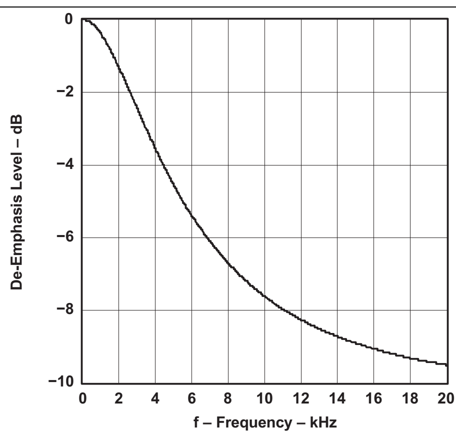
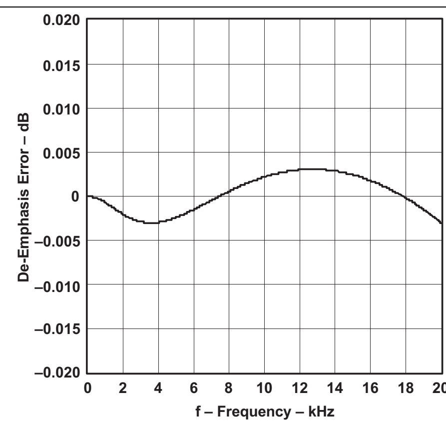


Figure 7. Amplitude vs Frequency Transition Characteristics, Slow Rolloff



f_S = 44.1 kHz

Figure 8. De-Emphasis Level vs Frequency



f_S = 44.1 kHz

Figure 9. De-Emphasis Error vs Frequency

Typical Characteristics (continued)

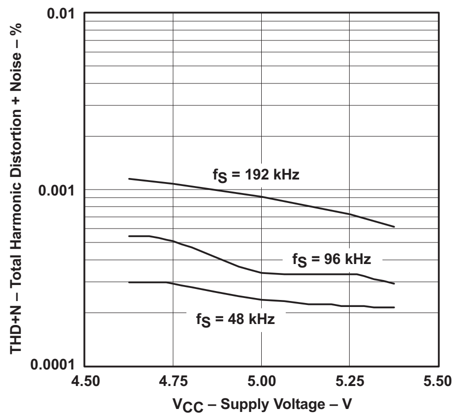


Figure 10. Total Harmonic Distortion + Noise vs Supply Voltage

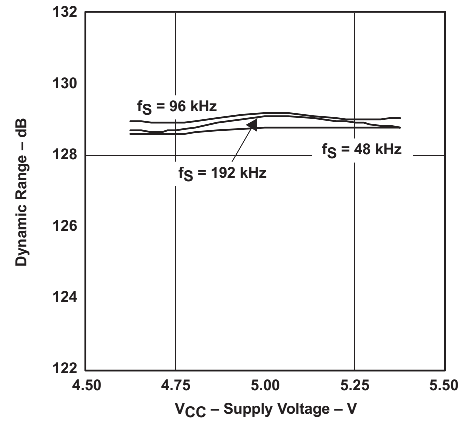
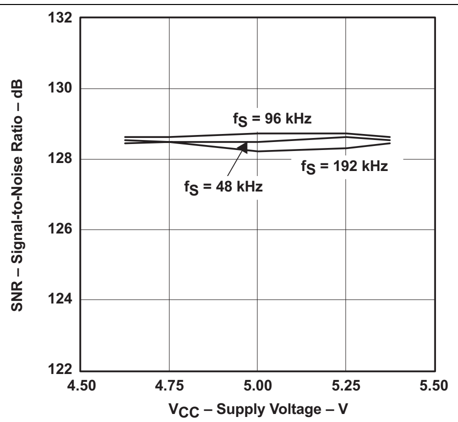


Figure 11. Dynamic Range vs Supply Voltage



T_A = 25°C V_{OUT} = 4.5 V_{RMS}
V_{DD} = 3.3 V Measurement circuit is Figure 26

Figure 12. Signal-to-Noise Ratio vs Supply Voltage

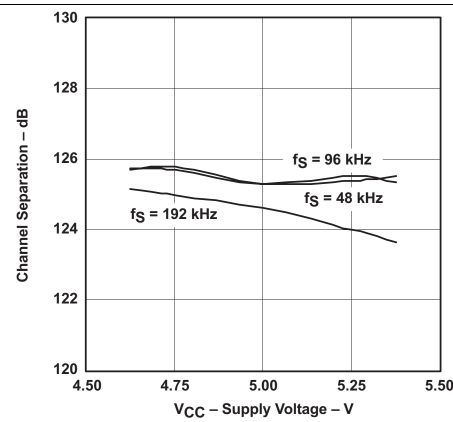


Figure 13. Channel Separation vs Supply Voltage

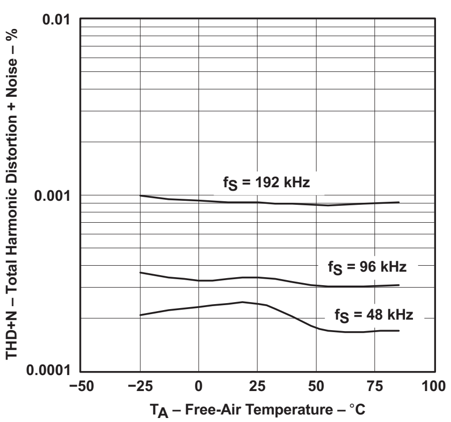


Figure 14. Total Harmonic Distortion + Noise vs Free-Air Temperature

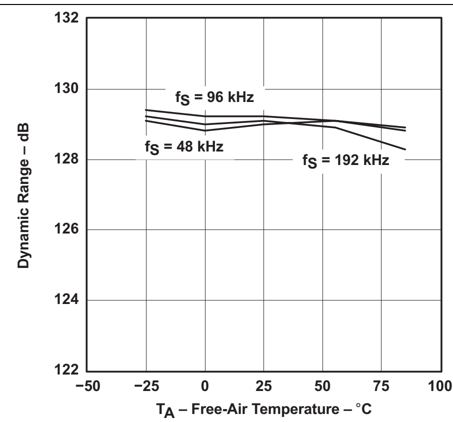
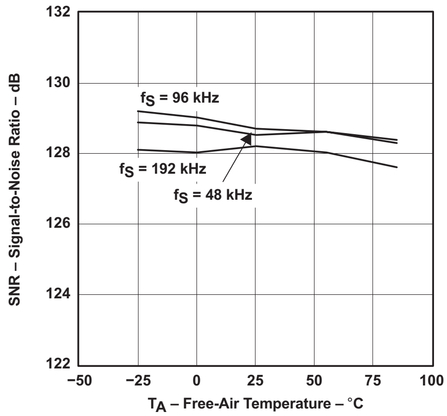


Figure 15. Dynamic Range vs Free-Air Temperature

Typical Characteristics (continued)



V_{CC} = 5 V
V_{DD} = 3.3 V
V_{OUT} = 4.5 V_{RMS}
Measurement circuit is Figure 26.

Figure 16. Signal-to-Noise Ratio vs Free-Air Temperature

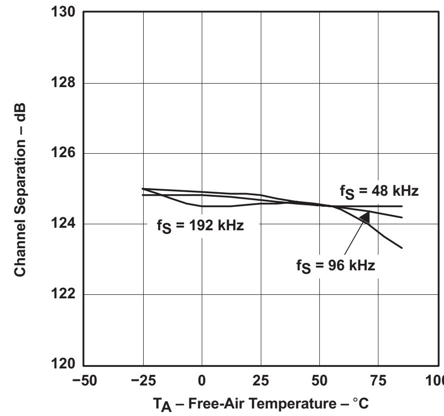
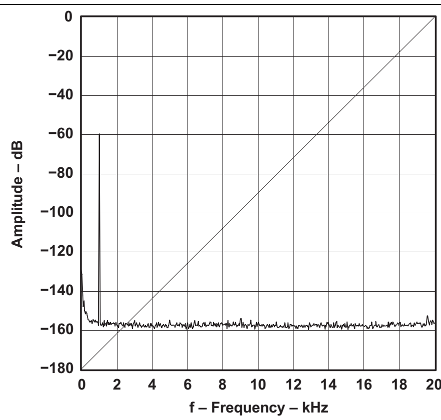
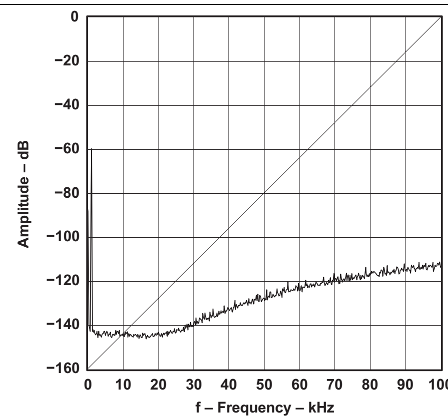


Figure 17. Channel Separation vs Free-Air Temperature



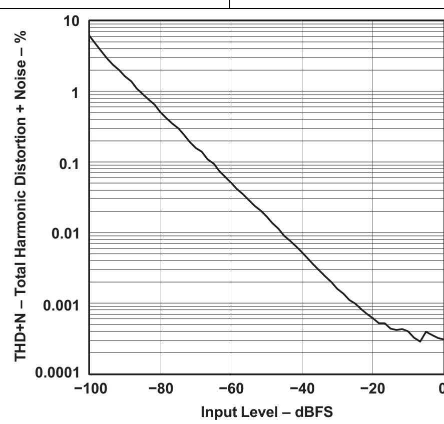
V_{CC} = 5 V
T_A = 25°C
V_{DD} = 3.3 V
Measurement circuit is Figure 26
f_S = 48 kHz, 32768 point 8 average

Figure 18. Amplitude vs Frequency
–60-db Output Spectrum, BW = 20 kHz



V_{CC} = 5 V
T_A = 25°C
V_{DD} = 3.3 V
Measurement circuit is Figure 26
f_S = 48 kHz, 32768 point 8 average

Figure 19. Amplitude vs Frequency
–60-db Output Spectrum, BW = 100 kHz



V_{CC} = 5 V
V_{DD} = 3.3 V
Measurement circuit is Figure 26
f_S = 48 kHz, T_A = 25°C

Figure 20. Total Harmonic Distortion + Noise vs Input Level

7 Detailed Description

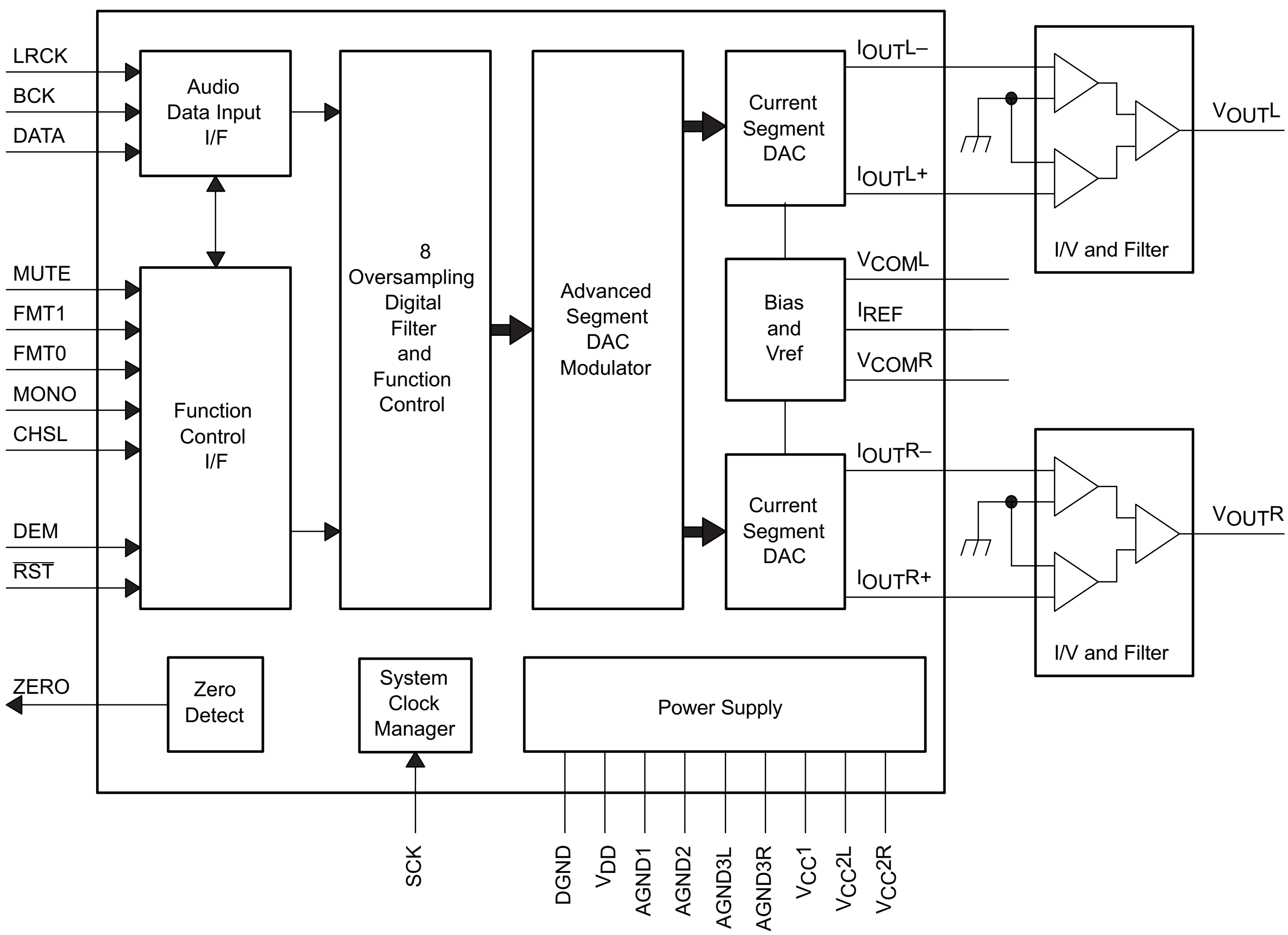
7.1 Overview

The PCM1794A device is a 24-bit, 192-kHz, differential-current, output digital-to-analog converter (DAC) that comes in a 28-pin SSOP package. The PCM1794AA device is hardware controlled and uses the advanced-segment DAC architecture from TI to perform with a Stereo Dynamic Range of 129 dB (132 dB Mono) and with a THD of 0.0004% at 44.1 kHz. The PCM1794AA device uses the SCK input as the system clock and automatically detects the sampling rate of the Digital Audio input when valid BCK and LRCK clocks are supplied. To bypass the internal filter, use an external digital filter.

Table 1. Device Features

FEATURE	DESCRIPTION
Resolution	24 bits
Audio data interface format	Standard, I^2S, left justified
Audio data bit length	16-bit, 24-bit selectable
Audio data format	MSB first, two's complement

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 System Clock Input

The PCM1794A device requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1794A device has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 2 shows examples of system clock frequencies for common audio-sampling rates.

The *Timing Requirements* table lists and Figure 1 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low-phase jitter and noise. One of the Texas Instruments PLL1700 family of multiclock generators is an excellent selection for providing the PCM1794A system clock.

Table 2. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	See (1)	See (1)

(1) This system clock rate is not supported for the given sampling frequency.

7.3.2 Power-On and External Reset Functions

The PCM1794A device includes a power-on reset function. Figure 21 shows the operation of this function. With V_{DD} > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V.

The PCM1794A device also includes an external reset capability using the $\overline{RST}$ input (pin 14), which allows an external controller or master reset circuit to force the PCM1794A device to initialize to its default reset state.

The *Timing Requirements* table lists and Figure 2 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state to start the initialization sequence, which requires 1024 system clock periods. The external reset is useful in applications with a delay between the PCM1794A power-up and system clock activation.

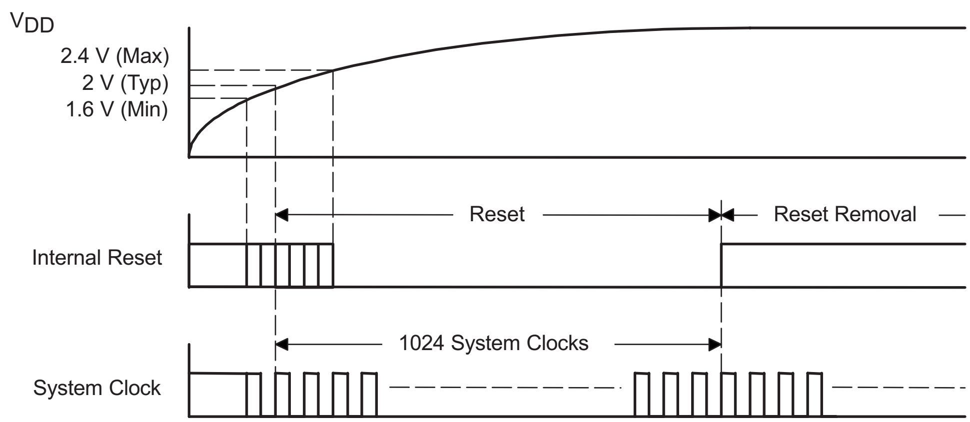


Figure 21. Power-On Reset Timing

7.3.3 Audio Data Interface

7.3.3.1 Audio Serial Interface

The audio interface port is a 3-wire serial port that includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1794A device on the rising edge of BCK. LRCK is the serial audio left/right word clock.

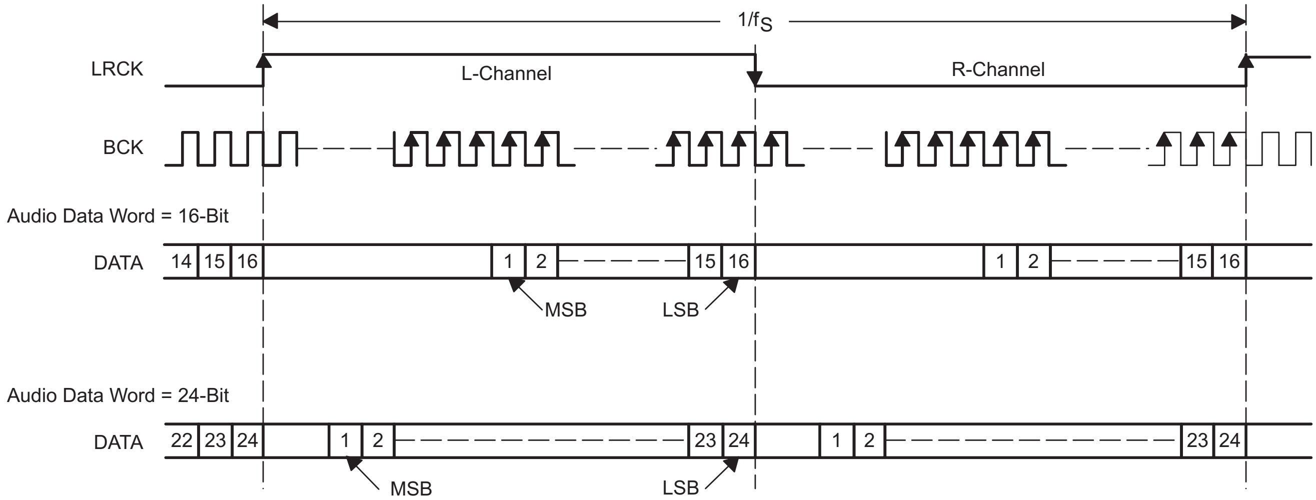
The PCM1794A device requires the synchronization of LRCK and the system clock, but does not require a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ±6 BCK, internal operation is initialized within $1/f_S$, and the analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

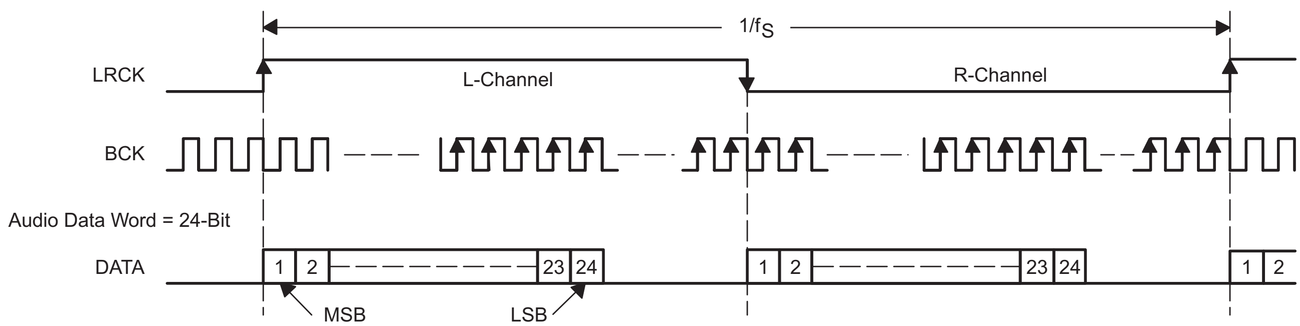
7.3.3.2 PCM Audio Data Formats and Timing

The PCM1794A device supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 22. Data formats are selected using the format bits, FMT1 (pin 12), and FMT0 (pin 11) as shown in Table 3. All formats require binary twos-complement, MSB-first audio data. The *Timing Requirements* table lists and Figure 3 shows a detailed timing diagram for the serial audio interface.

(1) Standard Data Format (Right Justified); L-Channel = HIGH, R-Channel = LOW



(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(3) I 2S Data Format; L-Channel = LOW, R-Channel = HIGH

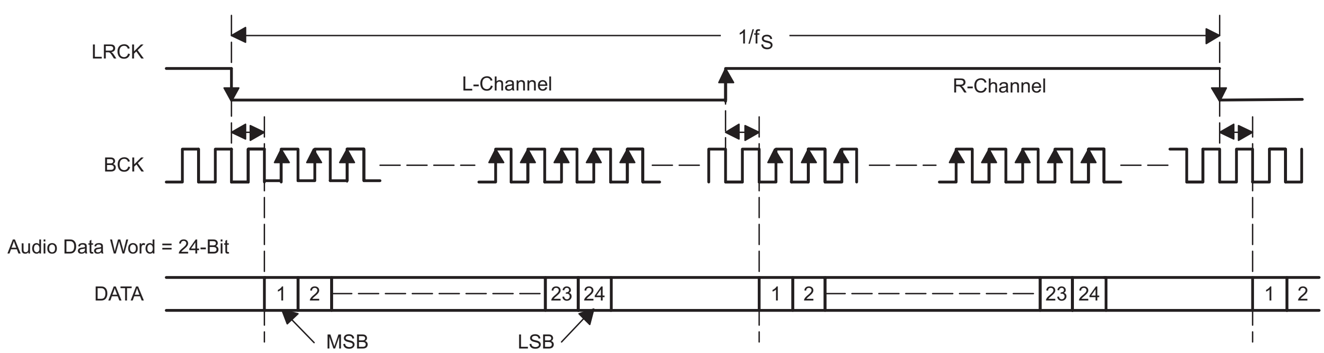


Figure 22. Audio Data Input Formats

7.3.4 Audio Data Format

Audio format is selected using FMT0 (pin 11) and FMT1 (pin 12). The PCM1794A device also supports monaural mode and DF bypass mode using MONO (pin 1) and CHSL (pin 2). The PCM1794A device can select the DF rolloff characteristics.

Table 3. Audio Data Format Select

MONO	CHSL	FMT1	GMT0	FORMAT	STEREO/MONO	DF ROLLOFF
0	0	0	0	I^2S	Stereo	Sharp
0	0	0	1	Left-justified format	Stereo	Sharp
0	0	1	0	Standard, 16-bit	Stereo	Sharp
0	0	1	1	Standard, 24-bit	Stereo	Sharp
0	1	0	0	I^2S	Stereo	Slow
0	1	0	1	Left-justified format	Stereo	Slow
0	1	1	0	Standard, 16-bit	Stereo	Slow
0	1	1	1	Digital filter bypass	Mono	—
1	0	0	0	I^2S	Mono, L-channel	Sharp
1	0	0	1	Left-justified format	Mono, L-channel	Sharp
1	0	1	0	Standard, 16-bit	Mono, L-channel	Sharp
1	0	1	1	Standard, 24-bit	Mono, L-channel	Sharp
1	1	0	0	I^2S	Mono, R-channel	Sharp
1	1	0	1	Left-justified format	Mono, R-channel	Sharp
1	1	1	0	Standard, 16-bit	Mono, R-channel	Sharp
1	1	1	1	Standard, 24-bit	Mono, R-channel	Sharp

7.3.5 Soft Mute

The PCM1794A device supports mute operation. When MUTE (pin 10) is set to HIGH, both analog outputs transition to the bipolar zero level in –0.5-dB steps with a transition speed of $1/f_S$ per step. The mute operation system provides pop-free muting of the DAC output.

7.3.6 De-Emphasis

The PCM1794A device has a de-emphasis filter for the sampling frequency of 44.1 kHz. The de-emphasis filter is controlled using DEM (pin 3).

7.3.7 Zero Detect

When the PCM1794A device detects that the audio input data in the L-channel and the R-channel is continuously zero for 1024 LRCKs in the PCM mode, or that the audio input data is continuously zero for 1024 WDCKs in the external filter mode, the PCM1794A device sets ZERO (pin 13) to HIGH.

7.3.8 Advanced Segment DAC

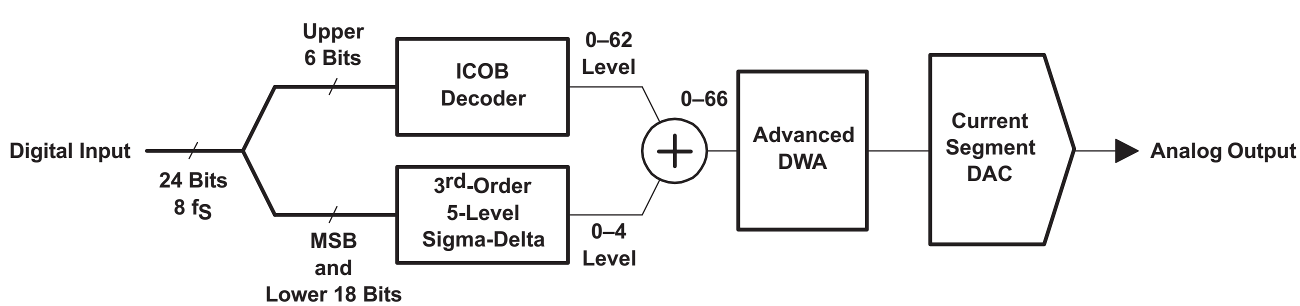


Figure 23. Advanced Segment DAC

The PCM1794A device uses TI’s advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1794A device provides balanced current outputs.

Digital input data using the digital filter is separated into 6 upper bits and 18 lower bits. The 6 upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level, third-order delta-sigma modulator operated at 64 f_S by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to create an up-to-66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing, and also achieves excellent dynamic performance.

7.3.9 Analog Output

Table 4 and Figure 24 show the relationship between the digital input code and analog output.

Table 4. Digital Input Code and Analog Output

	800000 (–FS)	000000 (BPZ)	7FFFFF (+FS)
$I_{OUT}N$ [mA]	–2.3	–6.2	–10.1
$I_{OUT}P$ [mA]	–10.1	–6.2	–2.3
$V_{OUT}N$ [V](1)	–1.725	–4.65	–7.575
$V_{OUT}P$ [V](1)	–7.575	–4.65	–1.725
V_{OUT} [V](1)	–2.821	0	2.821

(1) $V_{OUT}N$ is the output of U1, $V_{OUT}P$ is the output of U2, and V_{OUT} is the output of U3 in the measurement circuit of Figure 25.

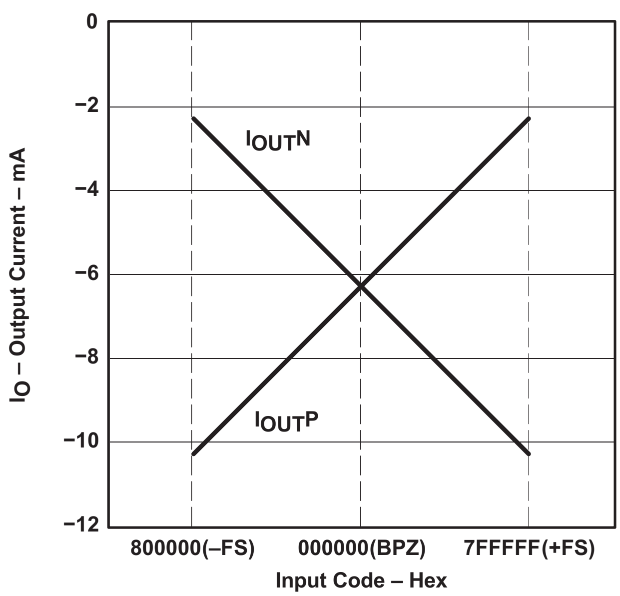


Figure 24. Relationship Between Digital Input and Analog Output

7.4 Device Functional Modes

7.4.1 Device Control

The PCM1794A device is a hardware controlled by external pins. These pins can be tied high or low directly to GND or to V_{DD}. These pins can also be controlled by the GPIO of a host controller.

7.4.2 Audio Input Modes

The PCM1794A device accepts PCM audio in I2S, Right justified (standard), or Left justified formats. The PCM1794 device has an internal digital filter that has the option of a slow or sharp roll off. Use an external digital filter to bypass the internal digital filter. External filter mode is explained more in the *Interfacing With an External Digital Filter* section.

7.4.3 Audio Output Modes

With the use of the MONO pin, the PCM1794A can output either differential stereo audio, or differential mono audio. Figure 25 shows an example of stereo output. Figure 27 shows an example of mono mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The design of the application circuit lets the user realize the high signal-to-noise (S/N) ratio of the PCM1794A device, as noise and distortion generated in an application circuit are not negligible.

In the circuit of Figure 25, the output level is 2-V_{RMS}, and 127-dB S/N is achieved. The circuit of Figure 26 should result in the highest performance. In this case the output level is set to 4.5-V_{RMS}, and 129-dB S/N is achieved (stereo mode). In monaural mode, if the output of the L-channel and R-channel is used as a balanced output, 132-dB S/N is achieved (see Figure 27).

Application Information (continued)

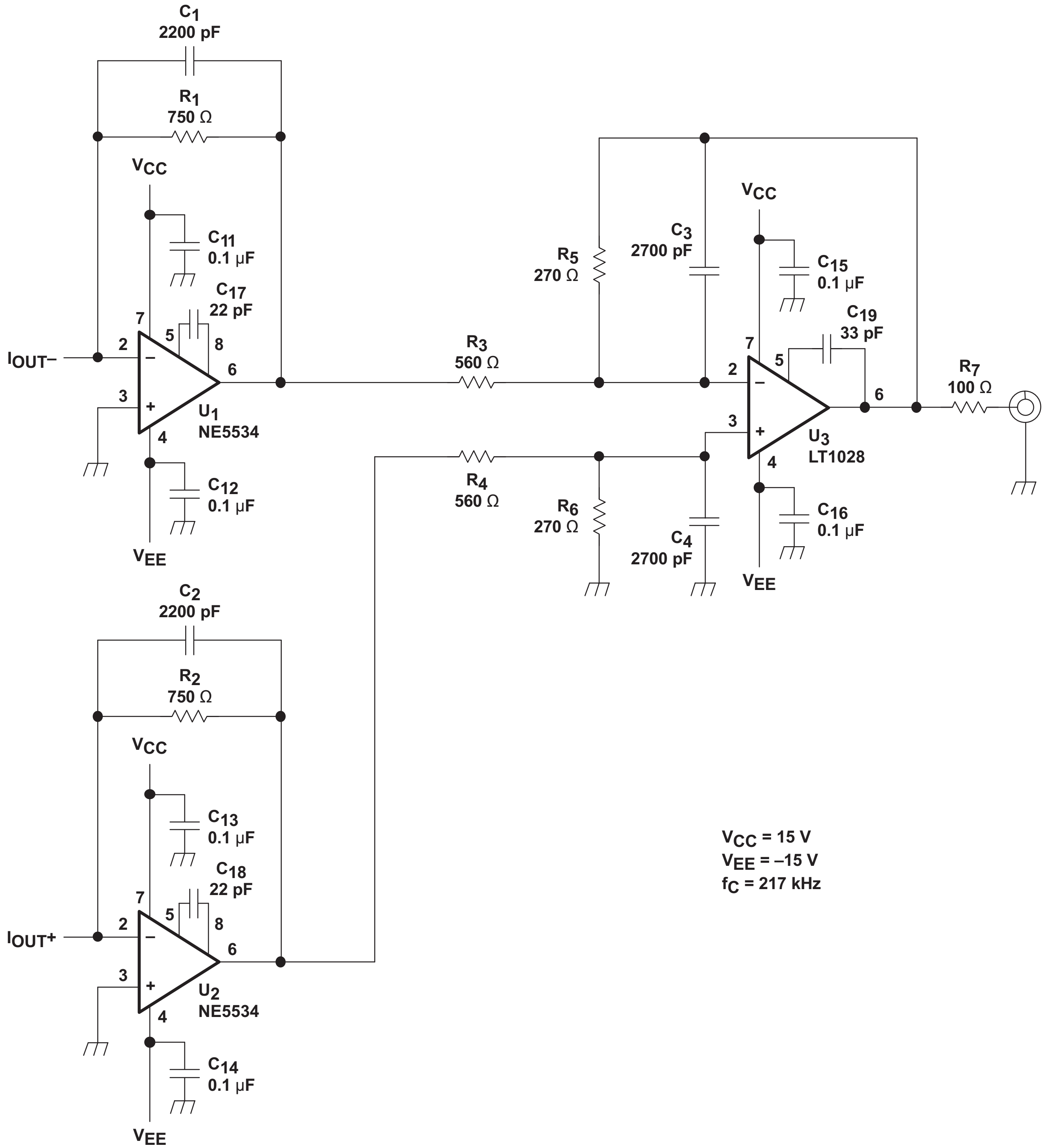


Figure 25. Measurement Circuit, V_{OUT} = 2-V_{RMS}

Application Information (continued)

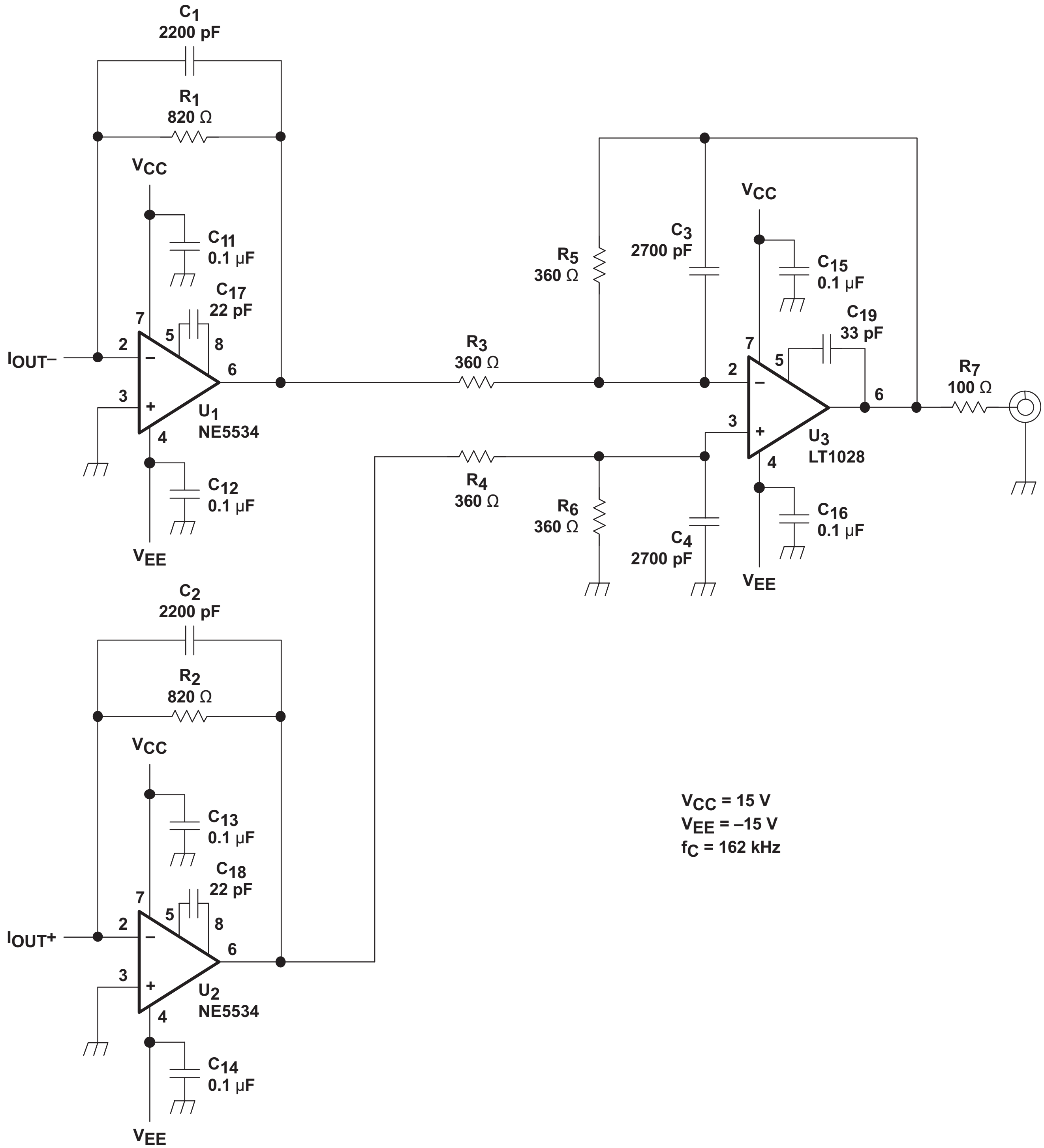


Figure 26. Measurement Circuit, V_{OUT} = 4.5-V_{RMS}

Application Information (continued)

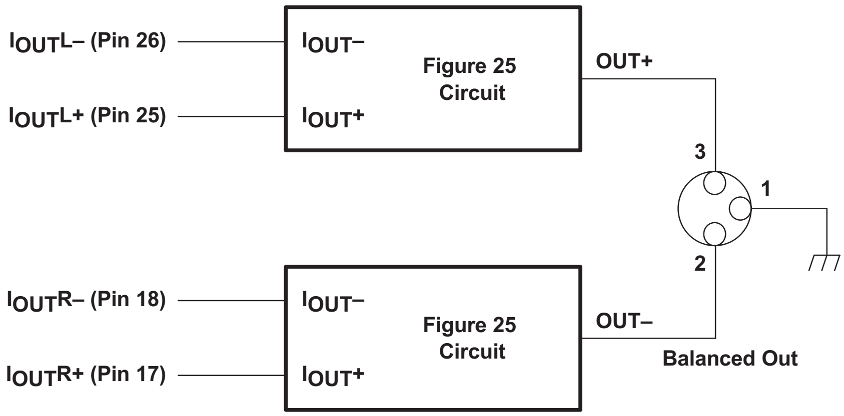


Figure 27. Measurement Circuit for Monaural Mode

8.1.1 I/V Section

The current of the PCM1794A device on each of the output pins ($I_{OUT}L+$, $I_{OUT}L–$, $I_{OUT}R+$, $I_{OUT}R–$) is 7.8 mA p-p at 0 dB (full scale). Use Equation 1 to calculate the voltage output level of the I/V converter (Vi).

$$Vi = 7.8\text{ mA p–p} \times R_f$$

where

- R_f is the feedback resistance of I/V converter (1)

An NE5534 operational amplifier is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

8.1.2 Differential Section

The PCM1794A voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the differential circuit is the Linear Technology LT1028, because the input noise is low.

8.1.3 Interfacing With an External Digital Filter

For some applications, using a programmable digital signal processor as an external digital filter to perform the interpolation function may be necessary. The following pin settings enable the external digital filter application mode:

- MONO (pin 1) = LOW
- CHSL (pin 2) = HIGH
- FMT0 (pin 11) = HIGH
- FMT1 (pin 12) = HIGH

The pins that provide the serial interface for the external digital filter are shown in the connection diagram of Figure 28. The word clock (WDCK) must be operated at 8× or 4× the desired sampling frequency, f_S.

Application Information (continued)

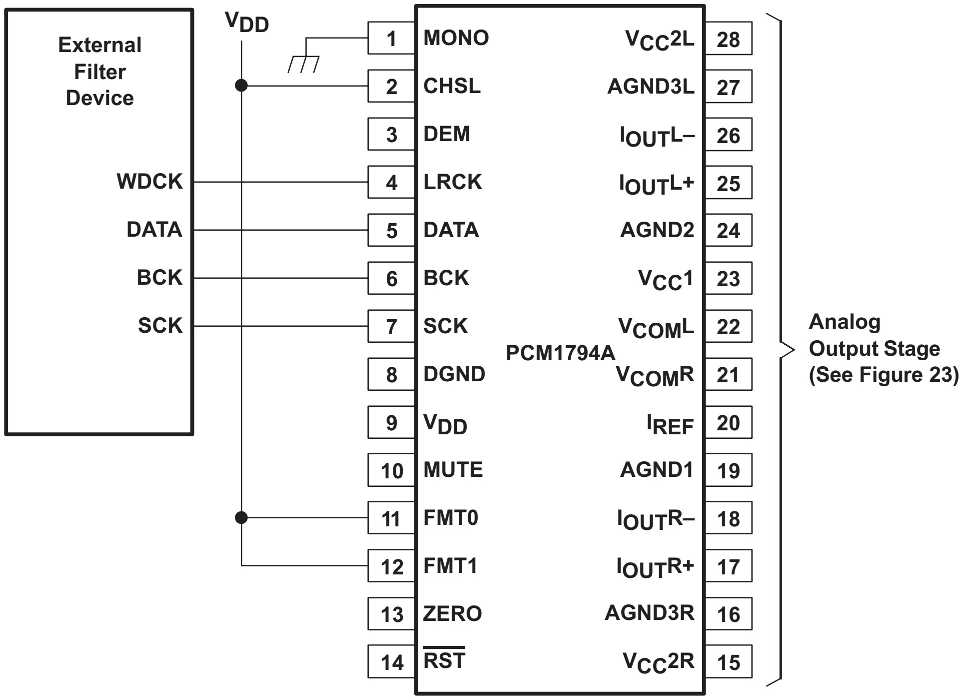


Figure 28. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application

8.1.3.1 System Clock (SCK) and Interface Timing

In an application using an external digital filter, the PCM1794A device requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, and DATA is shown in Figure 29.

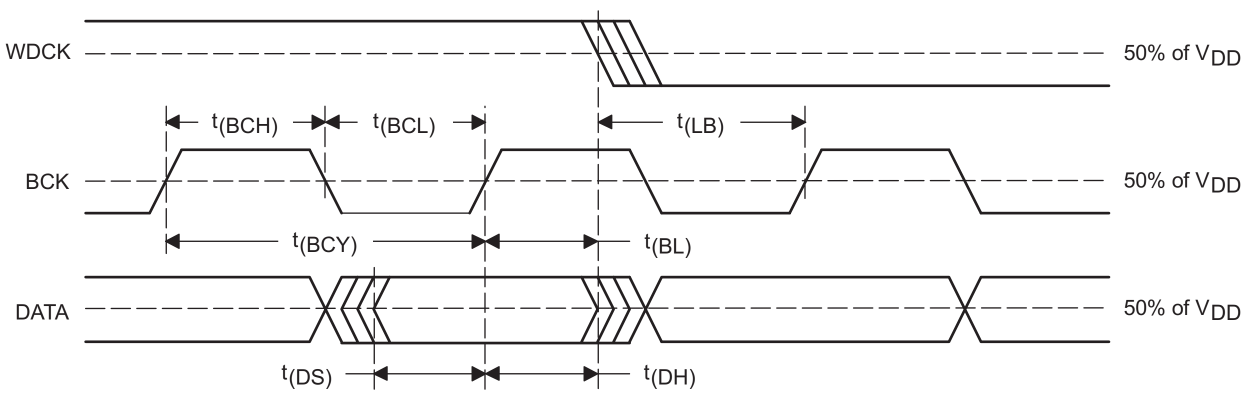


Figure 29. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Table 5 shows the timing requirements for an application using an external digital filter in internal DF bypass mode.

Application Information (continued)

Table 5. External Digital Filter Application Timing Requirements

		MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse-cycle time	20		ns
$t_{(BCL)}$	BCK pulse duration, LOW	7		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA setup time	5		ns
$t_{(DH)}$	DATA hold time	5		ns

8.1.3.2 Audio Format

The PCM1794A device in the external digital filter interface mode supports right-justified audio formats, including 24-bit audio data, as shown in Figure 30.

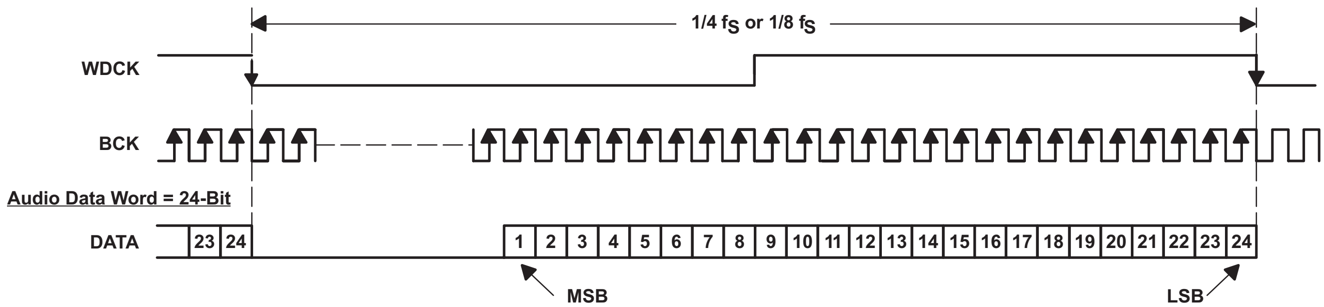


Figure 30. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application

8.2 Typical Application

This application is using the GPIO of a host controller to manipulate the hardware control pins. A PCM audio source is supplying digital audio and the output is single-ended stereo audio.

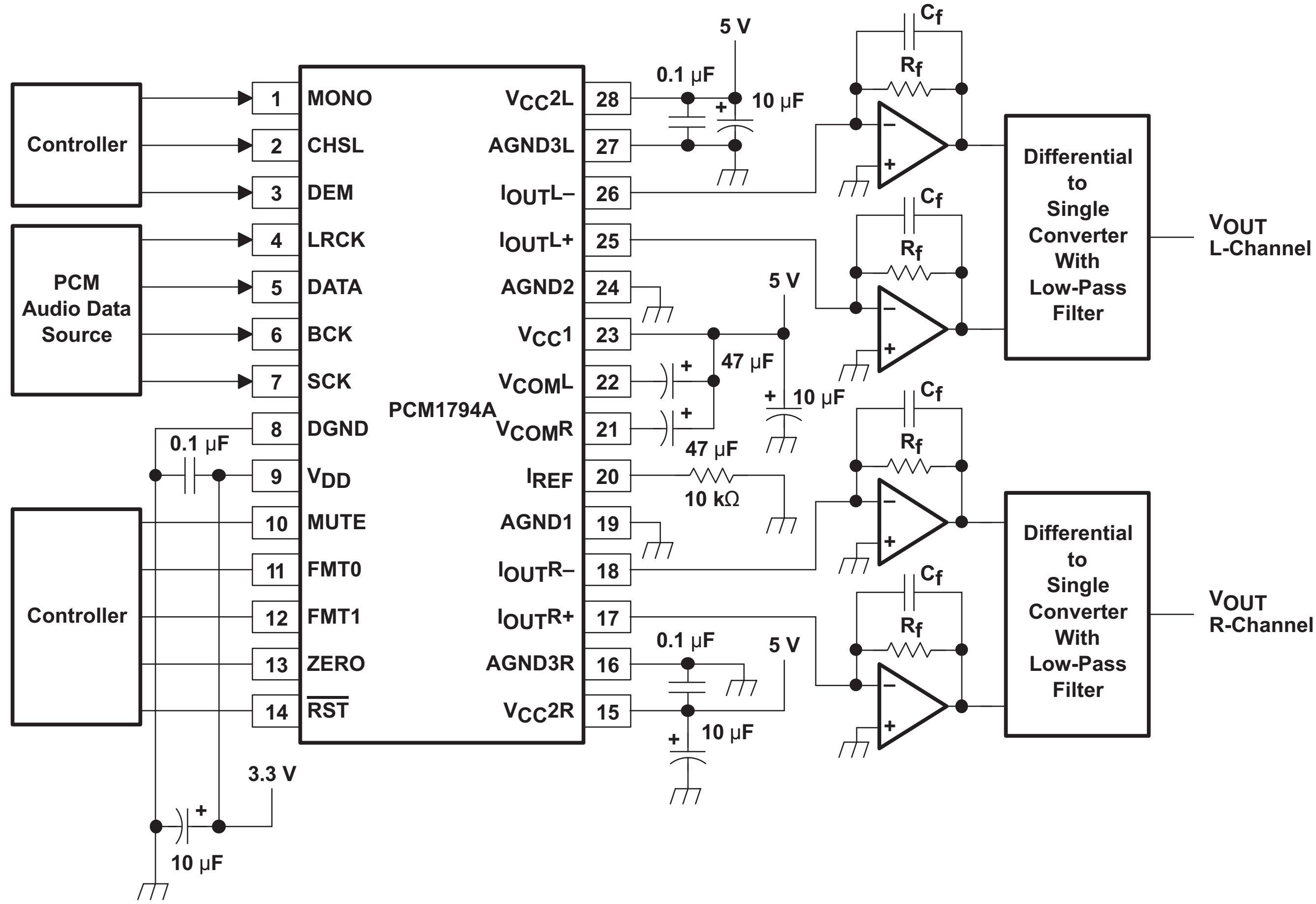


Figure 31. Typical Application Circuit

8.2.1 Design Requirements

For the typical application example, use the parameters listed in Table 6.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE
Audio Input	Digital PCM
Audio Output	Single-Ended Stereo Analog
Control	Host GPIO
Filter	Internal Filter

8.2.2 Detailed Design Procedure

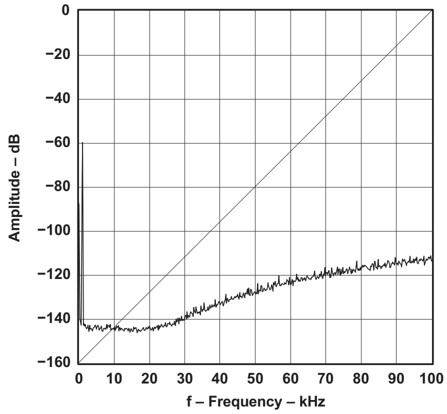
8.2.2.1 Audio Input or Output

In this application, a PCM audio source is supplied to the device. A current output is produced and then converted to a voltage output in the I/V stage. The next stage in the output is a differential to single-ended amplifier stage with a low pass filter to reduce out of band noise. The f_c of the example circuits (Figure 26 and Figure 27) are shown in the example figures. Use Equation 2 to calculate the value of f_c.

$$f_c = 1 / (2 \times \pi \times R_f \times C_f) \quad (2)$$

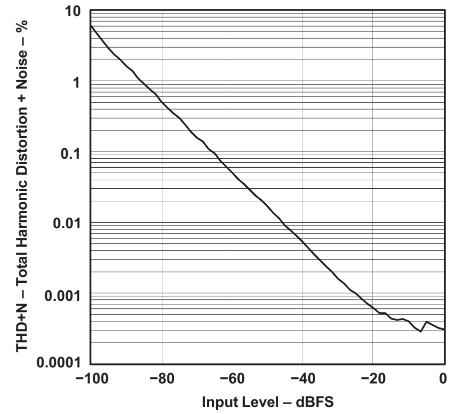
Typical Application (continued)

8.2.3 Application Curves



V_{CC} = 5 V
T_A = 25°C
V_{DD} = 3.3 V
Measurement circuit is Figure 26
f_S = 48 kHz, 32768 point 8 average
–60-db Output Spectrum, BW = 100 kHz

Figure 32. Amplitude vs Frequency



V_{CC} = 5 V
V_{DD} = 3.3 V
Measurement circuit is Figure 26
f_S = 48 kHz, T_A = 25°C

Figure 33. Total Harmonic Distortion + Noise vs Input Level

9 Power Supply Recommendations

The PCM1794A device requires 5-V (nominal) supplies. A 5-V supply is required for the analog circuitry powered by the VCC1, VCC2L, and VCC2R pins. A second 5-V supply is for the digital circuitry powered by the V_{DD} pin. These pins can be powered by the same 5-V rail but separating the supplies can assist with getting the target SNR and THD in some cases. Place the decoupling capacitors for the power supplies close to the device terminals.

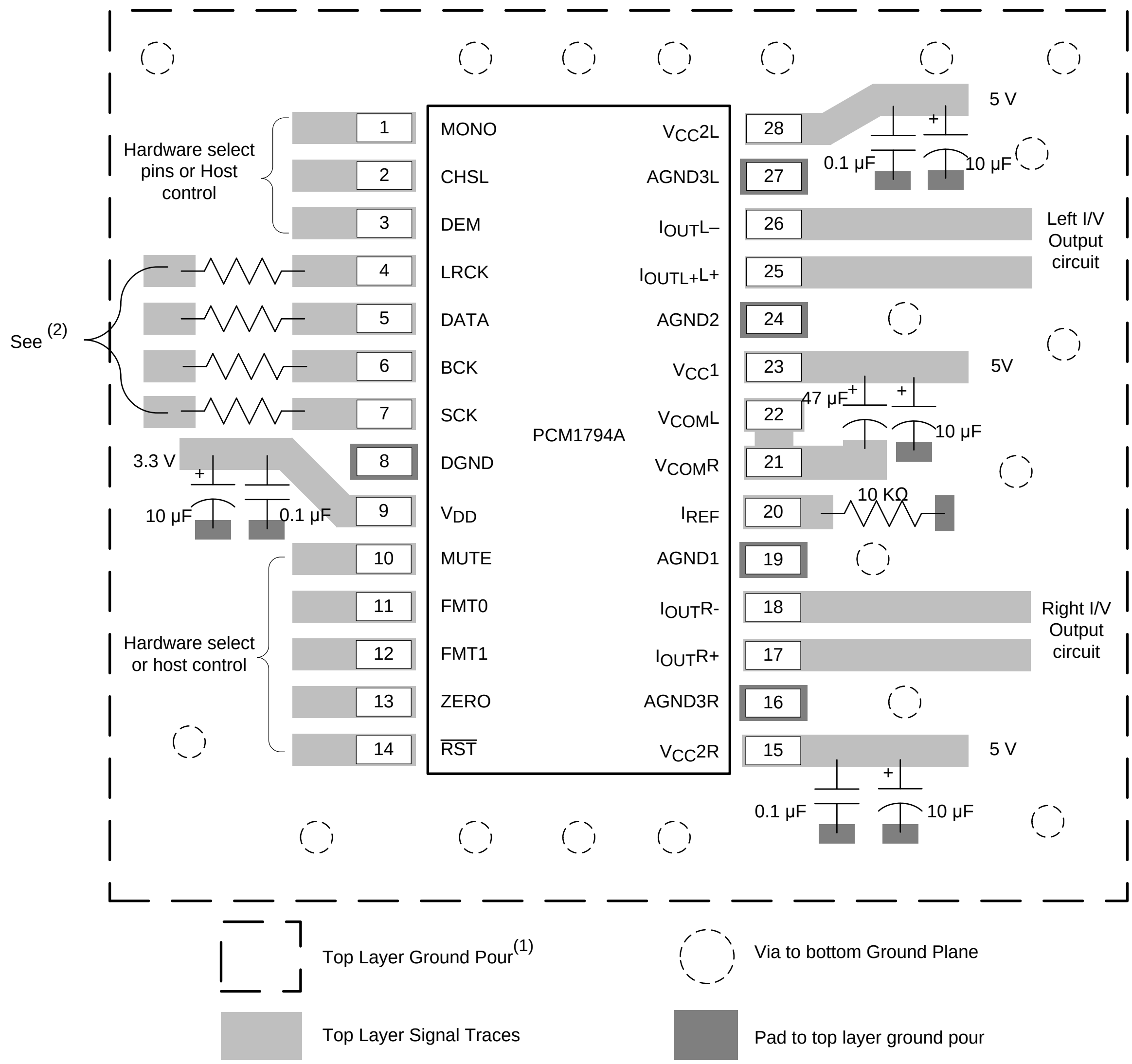
10 Layout

10.1 Layout Guidelines

TI recommends using the same ground between AGND and DGND to avoid any potential voltage difference between them. Ensure the return currents for digital signals avoid the AGND pin or the input signals to the I/V stage. Avoid running high frequency clock and control signals near AGND, or any of the I_{OUT} pins where possible. The pin layout of the PCM1794A partitions into two parts: an analog section and a digital section. If the system is partitioned in such a way that digital signals are routed away from the analog sections, then no digital return currents (for example, clocks) should be generated in the analog circuitry.

Place the decoupling capacitors as close to the Vcc1, V_{CC}2L, V_{CC}2R, V_{COM}L, V_{COM}R, and V_{DD} pins as possible. See Figure 34 for additional guidelines.

10.2 Layout Example



(1) TI recommends to place a top layer ground pour for shielding around device and connect it to the lower main PCB ground plane with multiple vias.

(2) These resistors help prevent overshoot and reduce coupling. Begin with a value of 10 Ω for the MCLK resistor and 27 Ω for the other resistors.

Figure 34. PCM1794A Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *A Low Noise, Low Distortion Design for Antialiasing and Anti-imaging Filters*, SBAA001
- *THD+N Versus Frequency Characteristics and Spectra of the PCM1717/18/19/20/23/27*, SBAA020
- *DEM-PCM1792, DEM-DSD1792, DEM-PCM1794, DEM-DSD1794, EVM Board*, SLEU037
- *NE5534x, SA5534x Low-Noise Operational Amplifiers*, SLOS070
- PLL1700 *Multi-Clock Generator*, SBOS096

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
Audio Precision is a trademark of Audio Precision.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1794ADB	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1794 A	Samples
PCM1794ADBG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1794 A	Samples
PCM1794ADBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1794 A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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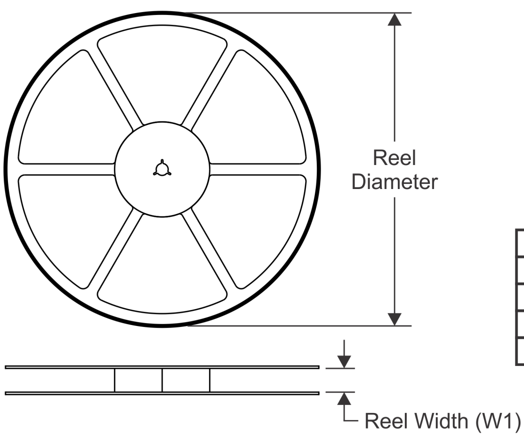
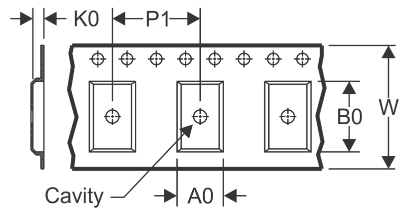
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

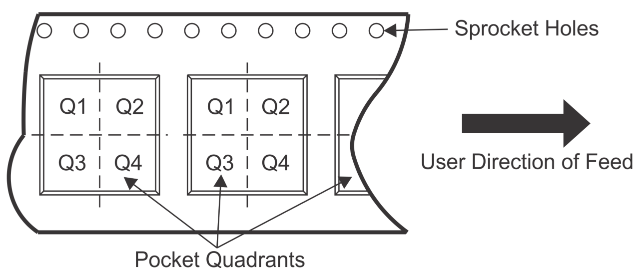


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

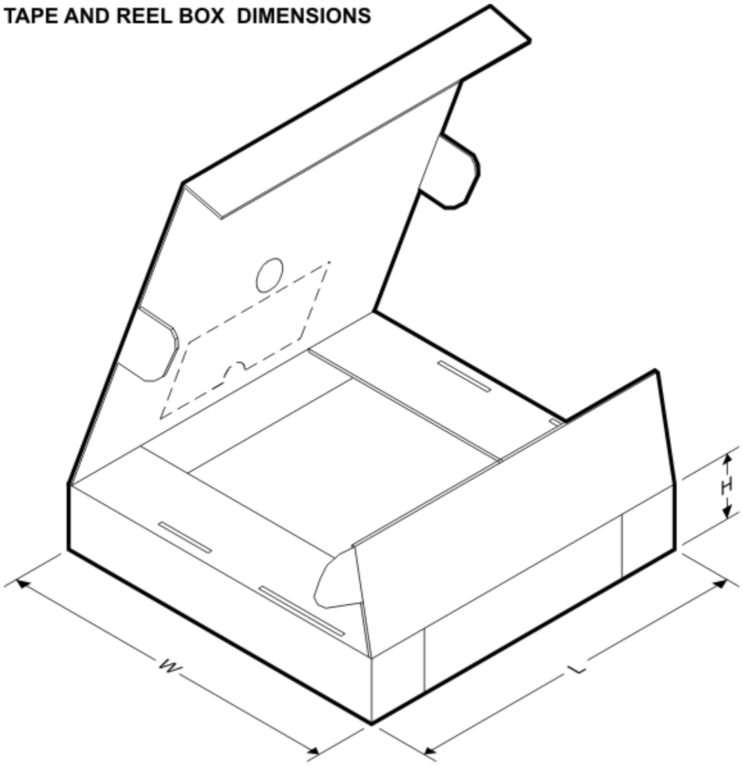
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1794ADBR	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

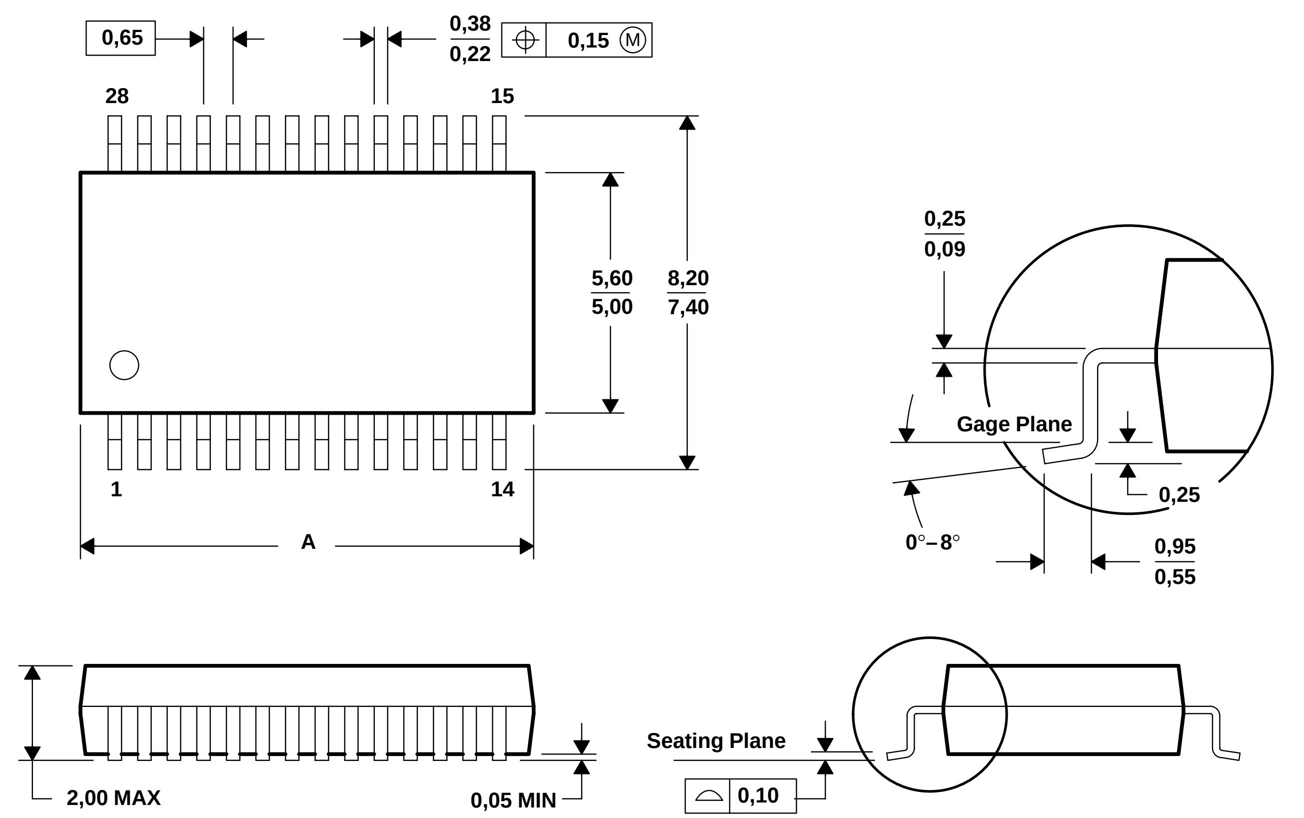


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1794ADBR	SSOP	DB	28	2000	336.6	336.6	28.6

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150