

Complementary MOSFET Half-Bridge (N- and P-Channel)

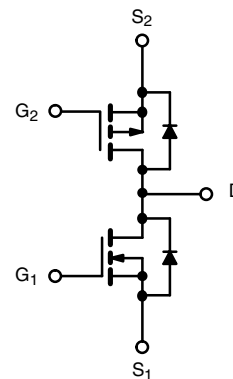
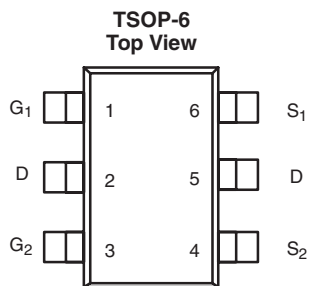
PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.300 at $V_{GS} = 4.5$ V	1.4
		0.410 at $V_{GS} = 3.0$ V	1.2
P-Channel	-20	0.640 at $V_{GS} = -4.5$ V	-0.96
		0.980 at $V_{GS} = -3.0$ V	-0.78

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si3850ADV-T1-E3 (Lead (Pb)-free)
Si3850ADV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C)	$T_A = 25$ °C	1.4	-0.96	A
	$T_A = 70$ °C	1.1	-0.77	
Pulsed Drain Current	I_{DM}	3.5	-2.0	
Continuous Source Current (Diode Conduction) ^a	I_S	0.9	-0.9	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	$T_A = 25$ °C	1.08		W
	$T_A = 70$ °C	0.70		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, $\pm \leq 10$ s)	R_{thJA}	115	°C/W

Note:
Maximum under Steady State condition is 150 °C/W.

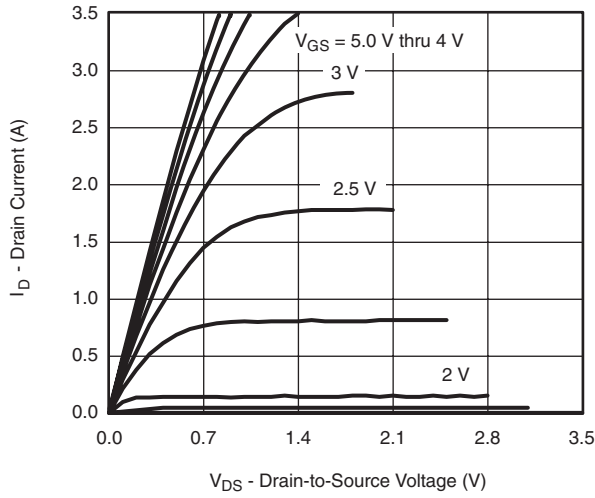
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	3.0			A
		$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-1.5			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$	N-Ch		0.240	0.300	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.510	0.640	
		$V_{GS} = 3.0\text{ V}, I_D = 0.5\text{ A}$	N-Ch		0.325	0.410	
		$V_{GS} = -3.0\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.780	0.980	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 1\text{ A}$	N-Ch		1.8		S
		$V_{DS} = -10\text{ V}, I_D = -1\text{ A}$	P-Ch		1.1		
Diode Forward Voltage ^b	V_{SD}	$I_S = 0.9\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.87	1.2	V
		$I_S = -0.8\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-1.0	-1.3	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$	N-Ch		0.95	1.4	nC
Gate-Source Charge	Q_{gs}		P-Ch		1.10	1.7	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$	N-Ch		0.22		nC
			P-Ch		0.28		
Gate Resistance	R_g		N-Ch		3.5	5.3	Ω
			P-Ch		10.5	16	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 0.9\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		8	14	ns
Rise Time	t_r		P-Ch		13	20	
		Turn-Off Delay Time	$t_{d(off)}$	N-Ch		16	
P-Ch				34	50		
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -0.9\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		20	30	
			P-Ch		18	30	
Body Diode Reverse Recovery Tme	t_{rr}	$I_F = 0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	N-Ch		20	30	
		$I_F = -0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	P-Ch		25	40	
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F = 0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	N-Ch		9	15	nC
		$I_F = -0.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	P-Ch		9	15	

Notes:

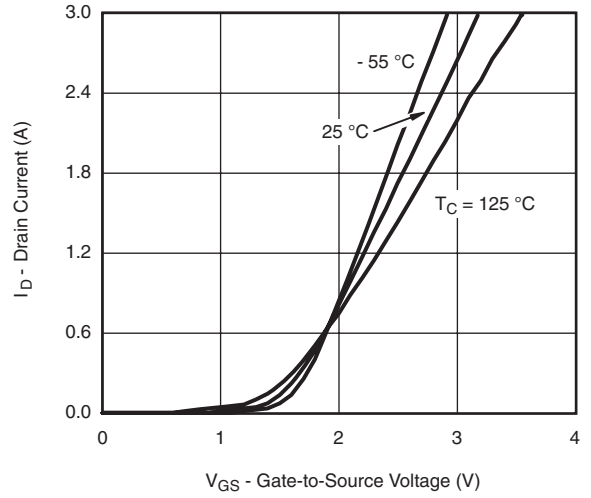
- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

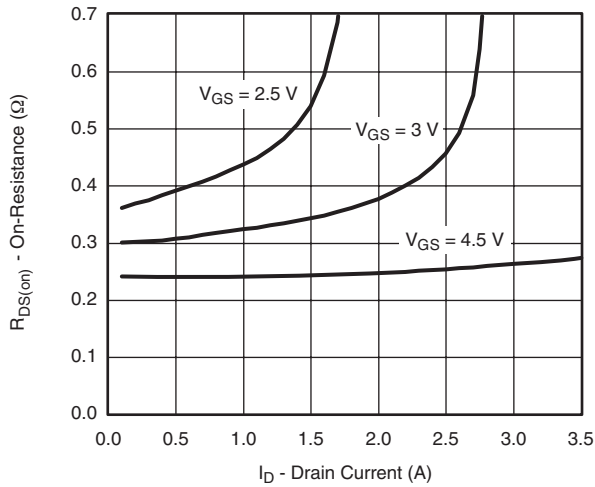
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



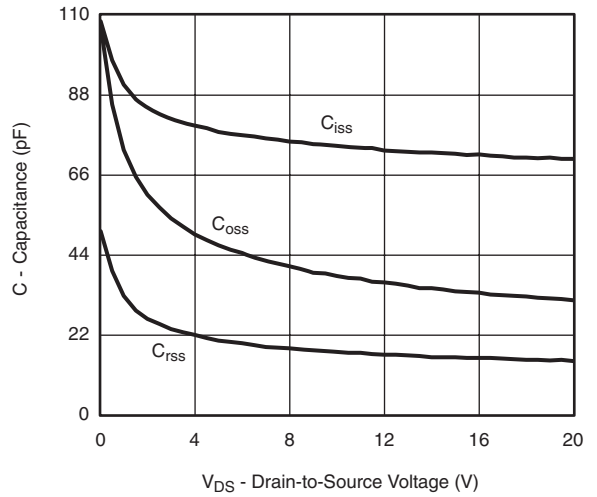
Output Characteristics



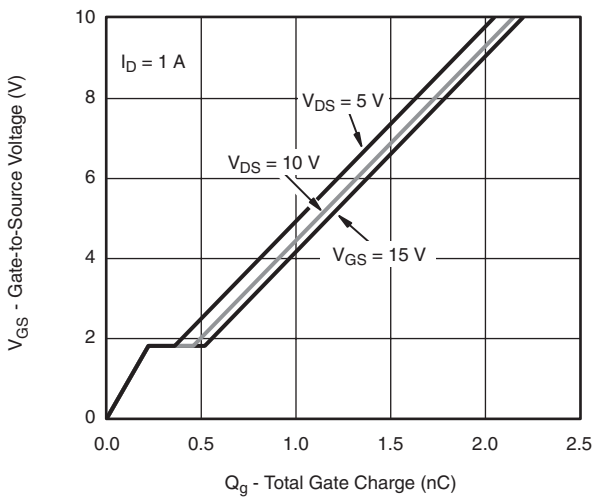
Transfer Characteristics



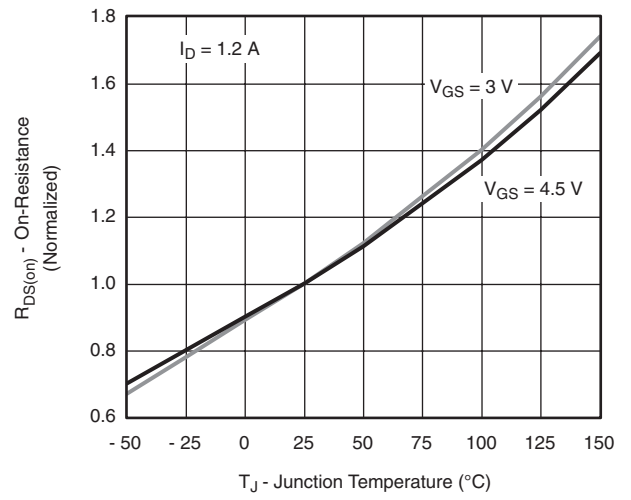
On-Resistance vs. Drain Current



Capacitance

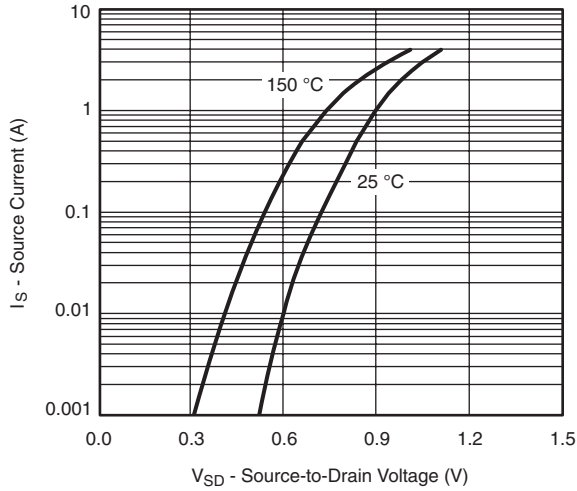


Gate Charge

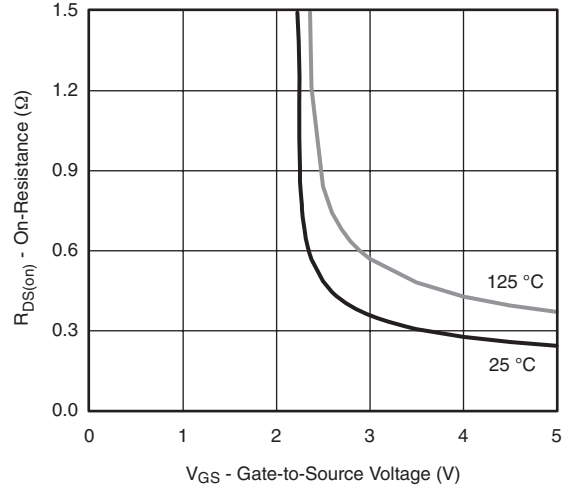


On-Resistance vs. Junction Temperature

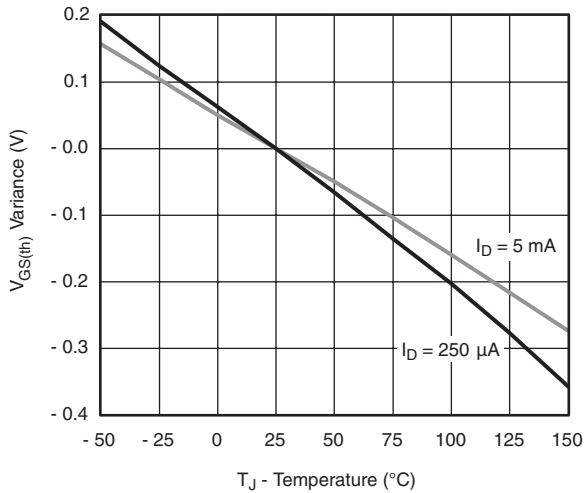
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



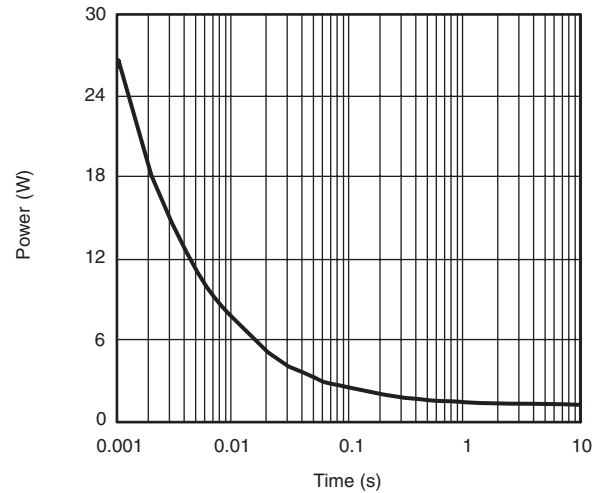
Source-Drain Diode Forward Voltage



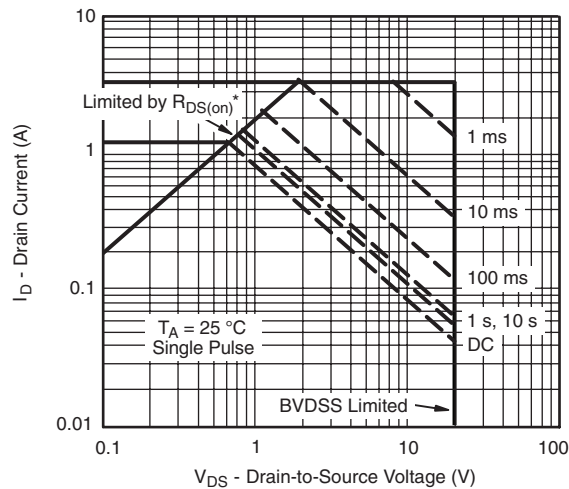
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

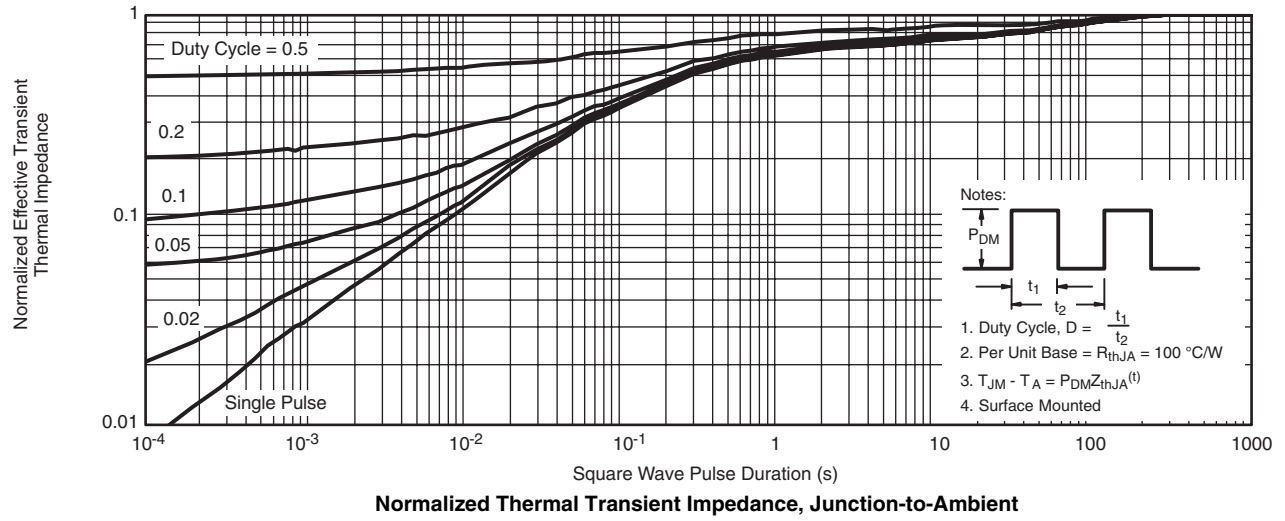


Single Pulse Power

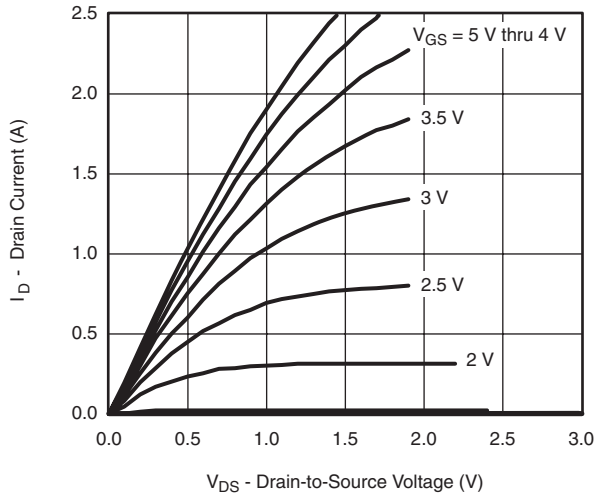


Safe Operating Area

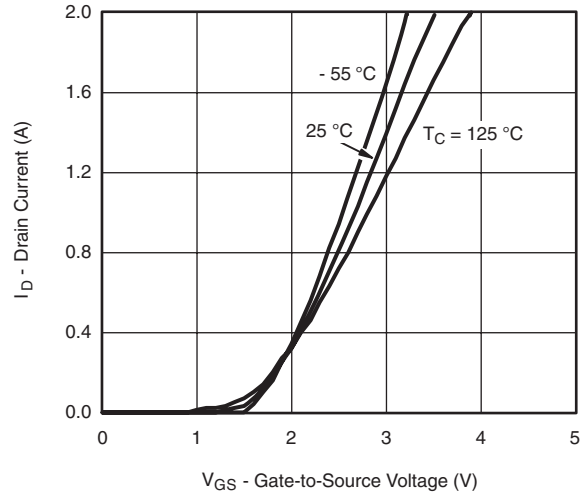
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



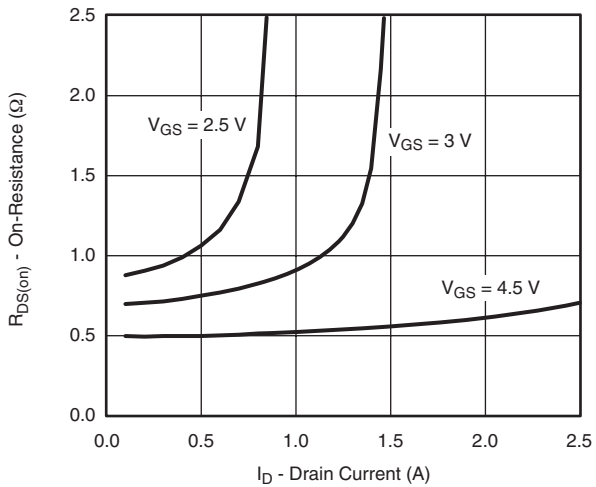
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



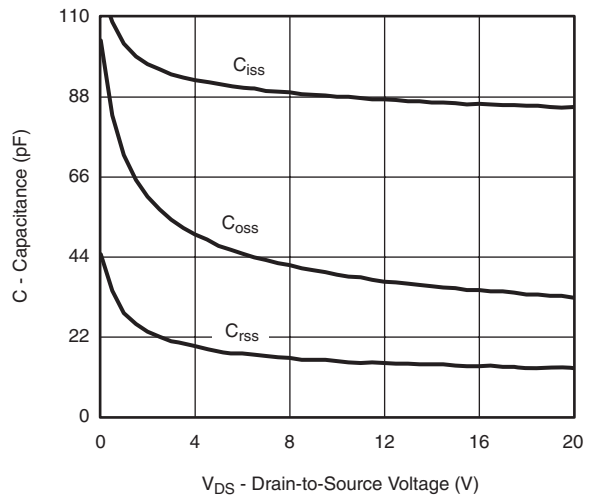
Output Characteristics



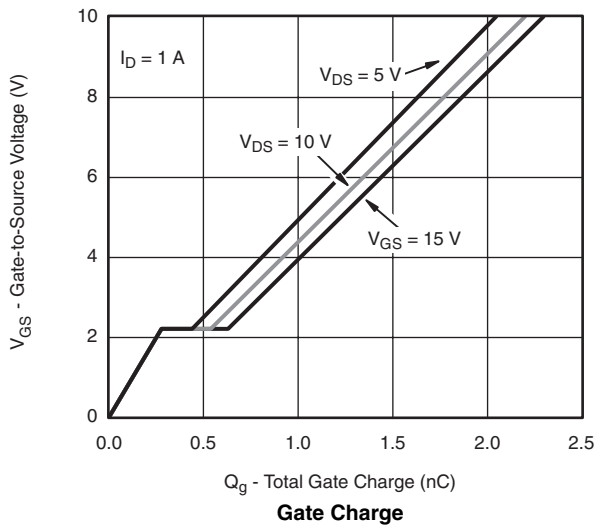
Transfer Characteristics



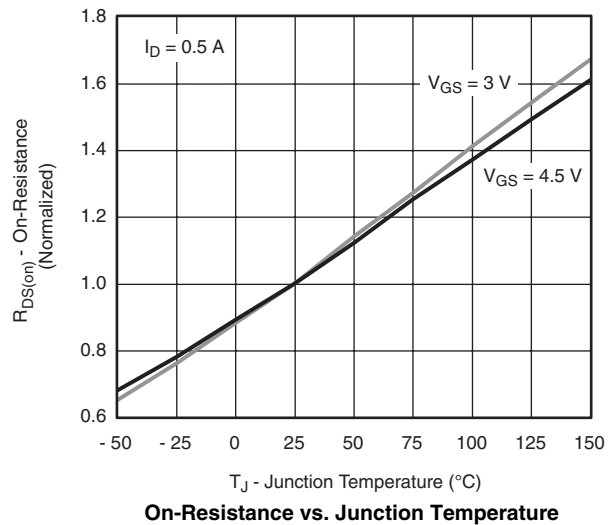
On-Resistance vs. Drain Current



Capacitance

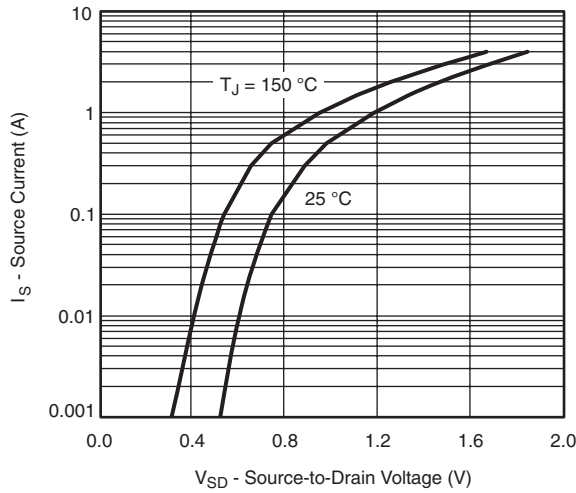


Gate Charge

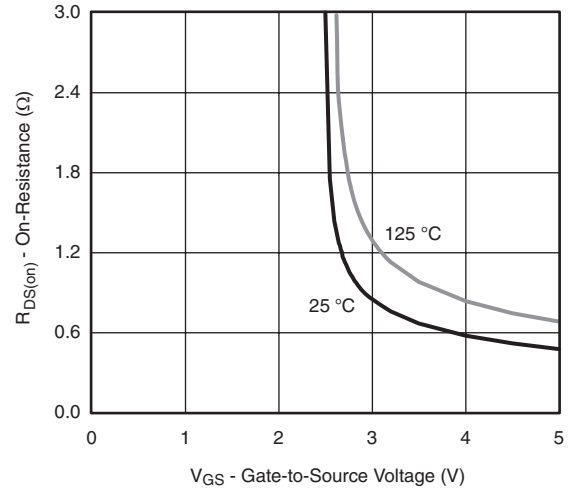


On-Resistance vs. Junction Temperature

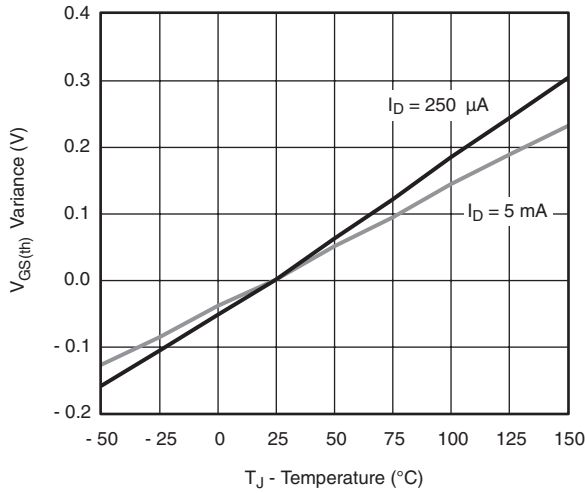
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



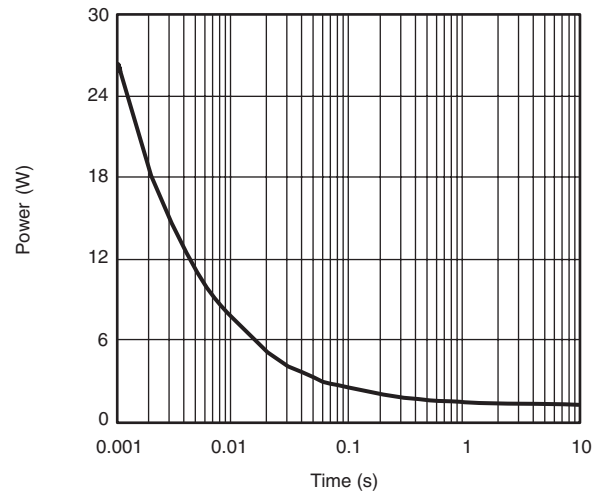
Source-Drain Diode Forward Voltage



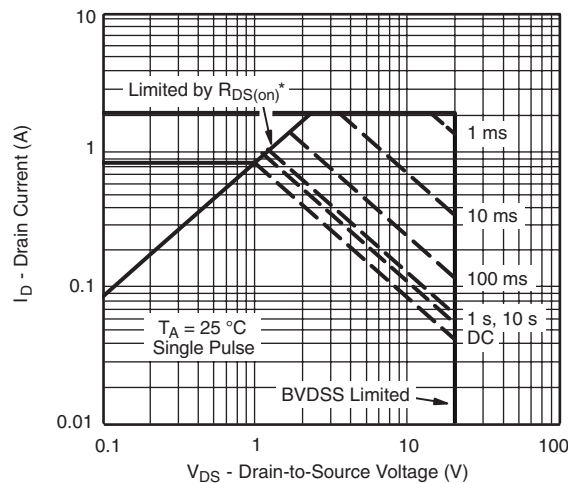
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



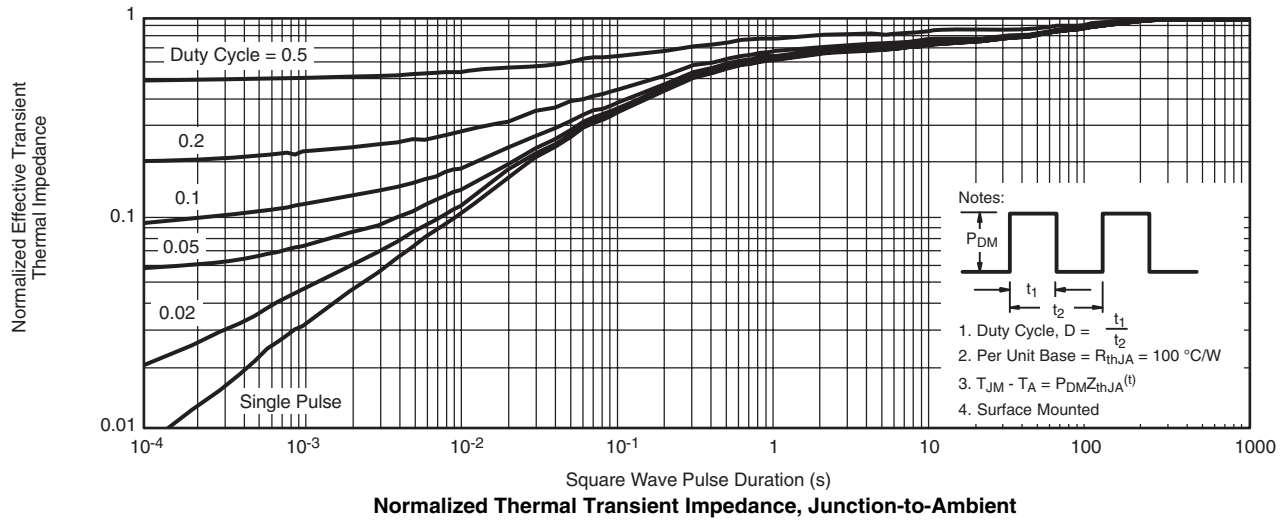
Single Pulse Power vs. Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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